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https://doi.org/10.15017/1961327

出版情報：Proceedings of International Exchange and Innovation Conference on Engineering & Sciences (IEICES). 4, pp.149-150, 2018-10-18. 九州大学大学院総合理工学府
バージョン：
権利関係：

Low-temperature fabrication and electric properties of Ge MOS capacitors

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Abstract: *Ge is of great interest in MOSFET applications due to its high carrier mobilities. Many research of Ge metal-oxide-semiconductor field effect transistor (MOSFET) have been studied to achieve More Moore. However, its potential of spintronics and flexible electronics have not been researched. We fabricated Ge MOS capacitors (CAPs) under 250°C, and investigated the electrical properties. The MOSCAPs fabricated under 250°C shows typical C-V curves with small hysteresis, and the breakdown voltage is well suppressed. The quality of MOSCAPs fabricated at low temperature is similar to those fabricated at higher temperatures. Density of interface trap (D_{it}) it is only slightly higher in the upper half of the bandgap. Therefore, Ge has potential to be applied to spintronics and flexible electronics.*

Keywords: Ge MOS capacitor

1. INTRODUCTION

In the semiconductor industry, Si has met the limitation on scaling. As a high channel mobility material, Ge is considered as one of beyond-Si materials. Many issues have been solved, and high mobility Ge MOSFETs have been reported. [1,2] Another possible application ways of Ge are spintronics (spin-FET) and flexible electronics (high mobility TFT on polymer substrate). [3,4] For these applications, a low temperature fabrication process is necessary because of the low thermal stability of spin-source/drain or polymer substrate. However, no one has focused on fabrication of high quality Ge MOS capacitor at low temperature yet. In this study, we aim to investigate qualities of Ge MOSCAPs fabricated under low temperatures.

2. EXPERIMENTAL

Both p- and n-type (111) Ge substrate with doping concentration 1.2×10^{16} and 4.0×10^{15} cm^{-3} was used. The reason we used (111) surface is that spin injection/detection electrodes can be formed on (111) surface. [3] After wet cleaning, SiO_2 was deposited by radio frequency (rf) sputtering at 250°C with O_2 flow. As a result, a thin layer of GeO_2 formed between the SiO_2 layer and the Ge substrate. This process is called SiO_2/GeO_2 bilayer passivation (BLP), which we usually conducted at a higher temperature. [5] Then, 10 nm SiO_2 was deposited by rf-sputtering at room temperature, and a post-deposition annealing (PDA) at 250°C in N_2 ambient for 30 minutes was carried out. After TiN deposition by sputtering, Al vacuum evaporation was performed. Next, Al/TiN layers were patterned as electrodes. Finally, a post-metallization annealing (PMA) was performed at 250°C in N_2 ambient for 30 minutes, followed by a back contact formation. The fabrication process and the schematic of sample structure are shown in Fig. 1 (a) and (b), respectively.

In order to compare the performance to the MOSCAPs fabricated at higher temperatures, the other MOSCAPs were fabricated with the same process, but both BLP and PMA temperatures were 300°C. In addition, the PDA temperatures were 300°C, 350°C and 400°C, respectively. Thermal budgets for the processes of all the MOSCAPs are shown in Fig. 2. Both *C-V* and *I-V* characteristics are measured in a black box for film quality evaluation, and D_{it} is evaluated by a double lock-in deep level transient spectroscopy (DLTS).

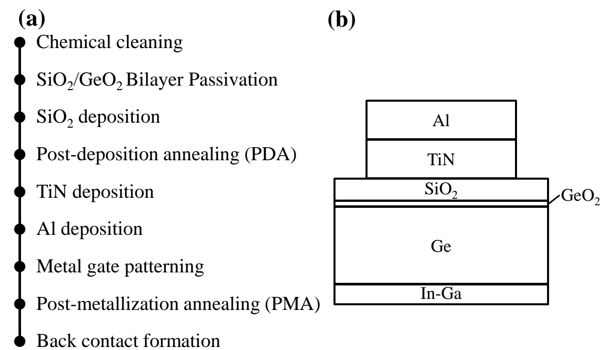

Fig. 1 (a) Fabrication process and (b) sample structure.

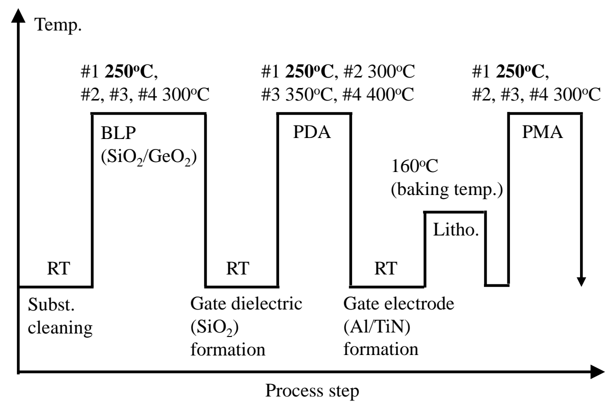

Fig. 2 Thermal budgets.

3. RESULTS AND DISCUSSION

Figure 3 shows the *C-V* characteristics of MOSCAPs fabricated with 250°C-PDA and 300°C-PDA. Typical *C-V* curves were obtained, and the MOSCAPs fabricated with 250°C-PDA and 400°C-PDA have no difference except for the flat band voltage (V_{FB}). These *C-V* results are not different from those fabricated under other temperatures (not shown).

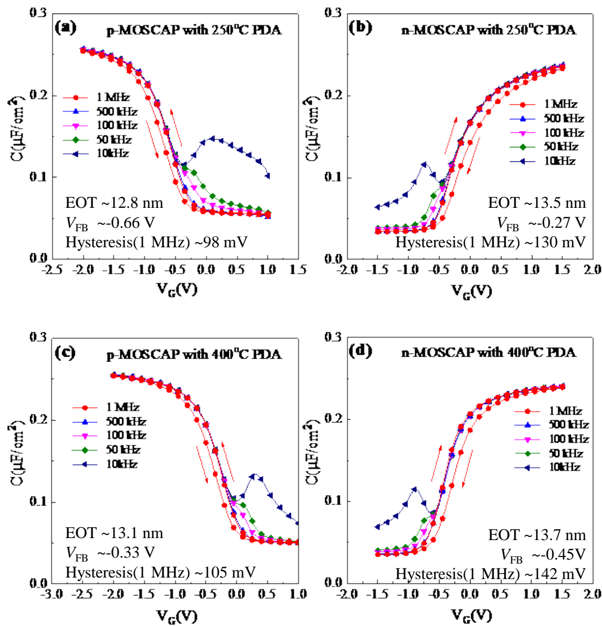

Fig. 3 *C-V* characteristic of (a) p-MOSCAP and (b) n-MOSCAP fabricated under 250°C. *C-V* characteristic of (c) p-MOSCAP and (d) n-MOSCAP fabricated under 400°C.

The V_{FB} and hysteresis of all samples are summarized in figure 4. V_{FB} shift is related to fixed oxide charges in oxide layers. All the V_{FB} here has a negative shift comparing to the ideal case (V_{FB}=0). This indicates that the fixed oxide charges are positive oxide charges. [6] V_{FB} of the p-MOSCAP shows a positive shift, which is close to V_{FB}=0, with increasing PDA temperature. By contrast, V_{FB} of the n-MOSCAP shows a negative shift with increasing PDA temperature. Therefore, with PDA temperature increasing, fixed oxide charges decrease in p-MOSCAPs, but they increase in n-MOSCAPs.
The hysteresis is counterclockwise (as shown in fig. 3), so it results from oxide trapped charges in the oxide layers. As shown in fig. 4, the hysteresis for all samples is small even for the MOSCAPs fabricated under 250°C. This implies the concentration of fixed oxide charges is low, which is important for high mobility MOSFET. Both fixed oxide charges and oxide trapped charges in a MOSCAP are illustrated in figure 5. [6,7]

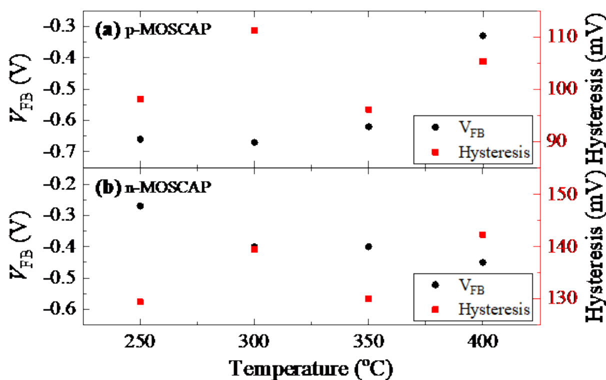

Fig. 4 Dependence of V_{FB} and hysteresis on the PDA temperature for (a) p-MOSCAPs and (b) n-MOSCAP.

Figure 6 shows the D_{it} for all the MOSCAPs. D_{it} in the upper half of the bandgap slightly decreases with increasing temperatures of PDA, but nearly no temperature difference can be seen in the lower half of the band gap. Besides, the high breakdown electric field indicates that the leakage current is well suppressed (figures are not shown). The *C-V* and *I-V* characteristics of all the MOSCAPs will be presented in the conference.

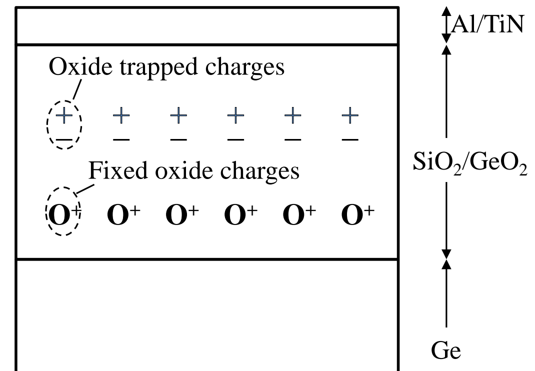

Fig. 5 Charges in oxide layers.

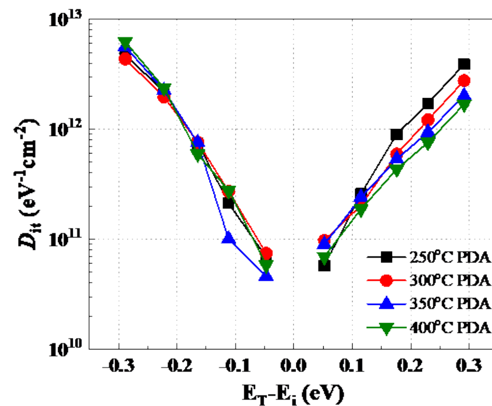

Fig.6 Dit of MOSCAPs.

4. SUMMARY

We successfully fabricated Ge MOSCAPs under 250°C, which is low enough to apply to spin-FET and flexible electronics. Although the performance may need to be improved, it seems Ge has potential for advanced applications.

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