A Multi-Layer Stacked All Sol-Gel Fabrication Technique for Vertical Coupled Waveguide

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https://doi.org/10.5109/1929657

出版情報：Evergreen. 4 (2/3), pp.12-17, 2017-09. Green Asia Education Center
バージョン：

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(Received June 5, 2017; accepted July 6, 2017).

A multi-layer vertically stacked all sol-gel fabrication technique on bulk silicon is proposed to realize vertical coupling from planar waveguides to 3-dimensional structures. The all sol-gel fabrication technique realizes the capability to stack ZnO sol-gel core layer and SiO_2 sol-gel cladding and core separation layers. A major issue with sol-gel based fabrication is the appearance of cracks on the sol-gel layer, and these were improved by a slow cooling process of 1°C/min after 500°C temperature annealing in addition to a SiO_2 surface cleaning using photoresist remover. As a result, a multi-layer vertically stacked structure with a ZnO core layer thickness of 300 nm and SiO_2 cladding/core separation layer thickness of 1.5 µm was successfully fabricated on bulk Si.

Keywords: vertical stacking, photonics, sol-gel.

1. Introduction

Space division multiplexing (SDM)[1] is a technique that is proposed as one of the main candidate to address the issue of ever increasing demand for greater data transmission. Multi-core fibers (MCF) are a major component in realizing SDM to improve the capacity of data transmission bandwidth[2]. Issues appear when coupling light into the MCF which has a 3 dimensional core layout at the fiber facet to planar photonic circuits such as optical switches, multiplexers, and waveguides. Several schemes have been proposed for interfacing such as fan-in/fan-out device[3], vertical silicon waveguides[4], vertical MMIs[5], compact lens coupling[6] and vertical coupled waveguides[7]. Among them, an all sol-gel multi-layer fabrication is attractive because of the capability to stack materials with different refractive index and the ability to control the thickness of the layers. In this work, we propose stacked multi-layer all sol-gel fabrication technique to enable the realization of a vertical coupled waveguide.

Coupling occurs when two parallel core waveguides with a higher refractive index are separated by a core separation layer of a lower refractive index[8]. Figure 1(a) shows an example with a 300 nm core waveguide (refractive index of 1.9) and 1.5 µm core separation (refractive index of 1.4). Beam propagation method simulation was used to simulate the structure and the results are shown in Fig. 1(b).

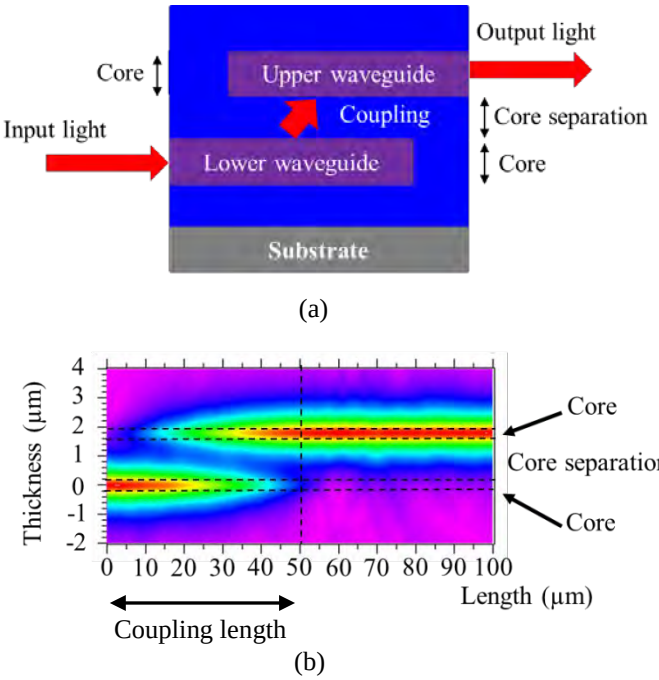


Fig. 1: Vertical coupled waveguide with (a) schematic showing stacked waveguide structure and (b) simulation results of showing core thickness of 300 nm and core separation of 1.5 µm with coupling length of around 50 µm.

The simulation results for the optical power injected into the lower waveguide and coupling to the upper waveguide showed a coupling length of around 50 µm.

In order to fabricate such a vertical coupled waveguide structure, the cladding, core and core separation layers must be stacked on top of one another during the fabrication process. This stacking process requires the ability to control the thickness of the different layers as it directly affects the capability and performance of the vertical coupling.

There are several deposition techniques of multi-layered materials including chemical vapor deposition (CVD)[9], pulsed laser deposition[10], magnetron sputtering[11], and spray pyrolysis[12]. The majority of these fabrication process requires the use of plasma equipment such plasma enhanced chemical vapor deposition (PECVD) or sputtering which increases the complexity and cost of fabricating the device. Alternatively, sol-gel based fabrication has been proposed as a low cost alternative to fabricate optical devices. Examples of sol-gel materials used for photonic applications are SiO_2, ZnO, TiO_2 and GeO_2. The fabrication of sol-gel based optical devices has so far been demonstrated as a single photonic layer deposited on glass[13] and Si substrate[14].

A critical issue that is prevalent when using a sol-gel based fabrication technique is the appearance of deformation on the sol-gel layer. Deformations from sol-gel fabrication can be characterized into cracks, particle inclusion, surface striation and thickness non-uniformity[15], with the most prevalent issue being the appearance of cracks. The appearance of cracks on the sol-gel layer has been studied [16–19], however multi-layer stacking of sol-gel layers requires careful processing throughout the entire fabrication process. Furthermore, the influence of surface treatment can greatly affect fabrication results[20] and in the sol-gel fabrication process, it can also produce cracks. These finding and methods developed to overcome them are further described in the results and discussion section.

In order to fabricate the different layers by using sol-gel method, the compatible materials that have contrasting refractive index for optical confinement and negligible difference in thermal expansion coefficient must be selected. Table 1 shows the refractive index and thermal expansion coefficient of the substrate, Si and cladding layer, SiO_2 and the core layer ZnO.

Table 1: Refractive index and thermal expansion coefficient for Si, SiO_2 and ZnO sol-gel.

Material	Refractive index	Thermal expansion coefficient, α (K^{-1})
Si	3.42	2.6
SiO_2 sol-gel	1.44	0.6
ZnO sol-gel	1.92	0.475

In this work, we make use of SiO_2 sol-gel as the cladding and core separation layers and ZnO sol-gel as the core layers. The optical confinement was calculated to be 37% for the ZnO core and SiO_2 cladding structure.

The thermal expansion coefficient α is defined as:

$$\alpha = \frac{I(T)-I_0}{I_0 \times T} = \frac{\varepsilon_{therm}}{T} \quad (1)$$

where T is the annealing temperature and I_0 is a height of our material at room temperature.

Since we are using an Si substrate and depositing a layer of SiO_2 on top, the expansion of both these materials will differ at the maximum annealing temperature T by some $\Delta I(T)$ or ε_{therm} that is directly proportional to the mismatch in the thermal expansion coefficient and this is given by;

$$\Delta I(T) = I_0 \times \Delta T\left(\alpha_{Si} - \alpha_{SiO_2}\right) \quad (2)$$

$$\varepsilon_{therm} = \Delta T \times \Delta\alpha \quad (3)$$

For a sol-gel SiO_2 layer of 1500 nm on top of the Si substrate, the difference of $\Delta I(T)$ is 1.5. This higher difference forces the SiO_2 layer to contract at a slower rate compared to the Si substrate and this causes cracks to appear.

On the other hand, for the ZnO layer on top of the SiO_2 layer, a $\Delta I(T)$ is 0.38. This low $\Delta I(T)$ may enable the stacking of these two different sol-gel materials without deformation caused by thermal stress due to $\Delta I(T)$.

2. Experimental procedure

Throughout the experimental process, a standard Si substrate was cleaved into 3 cm x 3 cm size samples and cleaned in a diluted BHF solution (NH_4HF 13.1%) for 60 sec in order to make surface cleaning. The SiO_2 sol-gel solution was produced by mixing the following chemicals together; methyltriethoxysilane (MTES): ethyl silicate: ethanol: water: acetic acid in the following concentration 0.2:0.106:0.1:0.118:0.02 by following the work of K. Iwamoto[21]. The SiO_2 sol-gel solution was stirred at 600 rpm and 60°C for 6 hours to obtain a homogenous mixture and was left to cool down for another 6 hours to ensure that all chemical reactions have stabilized before usage.

The schematic of the fabrication process is shown in Fig. 2. The SiO_2 sol-gel solution was firstly spin coated onto the cleaned Si substrate to act as the first bottom cladding layer. The thicknesses of the sol-gel deposited layers are dependent on the rotation speed of the spin coater and the results are discussed further in the results and discussion section. Two heating stages were applied to the sample after spin coating where the first heating stage was for solvent evaporation and the second stage was for layer densification. After spin coating the sample for 60 sec, the sample was firstly heated on a hot plate up to 145°C for 60 mins and was then annealed under vacuum condition up to 500°C for another 60 mins to

fully solidify the layer. Once the sample was fully cooled to room temperature, it was cleaned in varying solutions to minimize cracks before depositing the core layer.

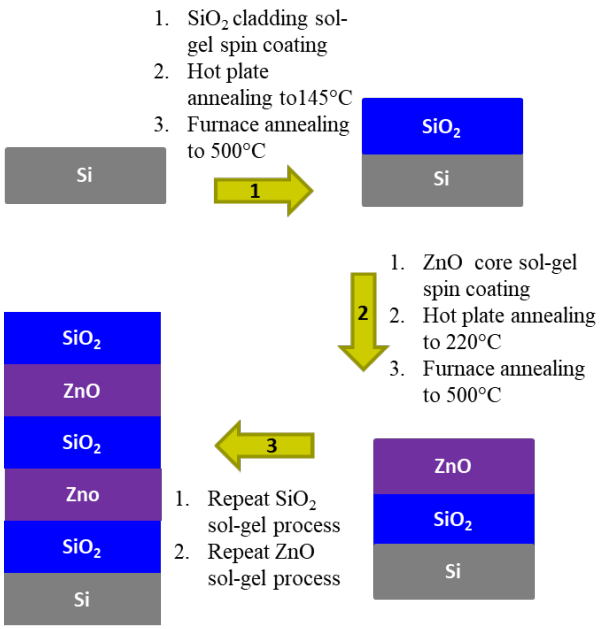


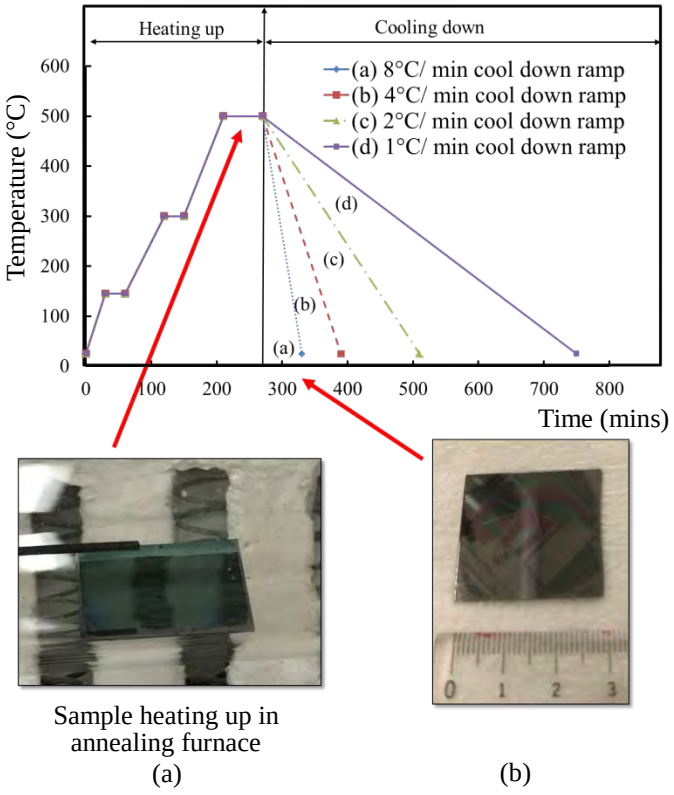
Fig 2: Process flow of the multi-layer stacked all sol-gel fabrication technique.

The core layer consists of ZnO sol-gel (Kojundo Chemical Laboratory). The ZnO sol-gel core layer was deposited as is and was spin coated onto the SiO_2 bottom cladding layer for 60 sec. The ZnO core layer sample was heated on a hot plate up to 220°C for 10 mins and then annealed under vacuum condition up to 500°C for another 60 mins. The same SiO_2 sol-gel spin coating, heating and annealing recipe was again used and deposited on top of the ZnO core layer to form the core separation layer. Similarly, the same recipe for the ZnO core layer was again used and deposited on top of the SiO_2 core separation layer. Finally all of the samples were cleaved and the facet and the surface of the sample were observed under an optical microscope to determine the stacking and thickness of all multiple layers as well as the condition of the surface.

3. Results and discussion

The two main advantages in the all sol-gel fabrication technique are the ability to stack the different sol-gel in a multi-layer structure and the ability to control the thickness of each individual layer. As stated in the introduction section, one critical issue for the sol-gel based fabrication techniques is the appearance of deformation on the sol-gel layer. The most prevalent issue of deformation is the appearance of cracks which are the breaking of the chemical bonds due to stress that appears during the heating stages on the sol-gel surface. In order to solidify the sol-gel solution, there are two heating stages that are applied to the sample after spin coating. The first heating stage involves a low temperature heating of the sample on a hot plate in air in order to evaporate the solvent used in the sol-gel. The second high temperature heating stage uses a thermal annealer where the sample is heated up to 500 °C under vacuum condition in order to condense and densify the sol-gel into a solid layer. Cracks can be categorized into either low temperature failures or high temperature failures[15]. Since we are stacking multiple SiO_2 and ZnO sol-gel layers, the cracks due to stress can occur at any layer during the fabrication process.

Cracks at low temperature are characterized by non-directional cracks that have no preferred orientation. In the SiO_2 sol-gel fabrication process, we make use of an organic modified precursor, MTES to provide stress relief during the low temperature solvent evaporation stage.



Sample heating up in annealing furnace

(a)

(b)

Fig. 3: High temperature annealing profile for SiO_2 heating and cooling down stage with cooling down ramps of 8°C/min, 4°C/min, 2°C/min, and 1°C/min. The bottom left inset (a) is of the sample in the annealing chamber showing no cracks during the heating up stage. The bottom right inset (b) shows cracks on the surface the appearance of cracks on the sample with an 8°C/min cooling down ramp.

The annealing temperature profile for the high temperature annealing stage is shown in Fig. 3. During the heating up stage, the sample undergoes stress due to densification. This thermal stress can lead to cracks especially if the layers have a large difference in thermal

expansion coefficient[22]. The appearance of cracks can lead to delamination and non-uniformity of the sol-gel layer which will hinder the stacking of further sol-gel layers. Therefore, in order to minimize and eliminate the cracks, we have chosen SiO_2 and ZnO sol-gel which has a smaller difference of thermal expansion coefficient. We do not observe any cracks during the heating up stage as shown in left inset of Fig. 3(a). Images of the sample at the maximum heating temperature do not show any evidence of cracks. This is because during the heating up process, the SiO_2 layer is still not fully cured. Therefore, there is no stress on the SiO_2 layer up to the maximum heating up temperature.

Cracks were only observed on the SiO_2 layer when cooling the sample from the maximum annealing temperature down to room temperature. The right inset of Fig. 3(b) shows the appearance of cracks on the sample based on an 8°C cool down ramp. During the cooling down stage, thermal stress that was generated and accumulated in the SiO_2 layer is released, and due to the thermal coefficient difference between SiO_2 and Si gives rise to the formation of cracks. This formation of cracks however can be reduced by controlling the cooling down ramp of the SiO_2 layer. Figure 4 shows the microscope view of the cracks on the SiO_2 surface when the sample was cooled down from maximum heating temperature down to room temperature by different cooling down ramps.

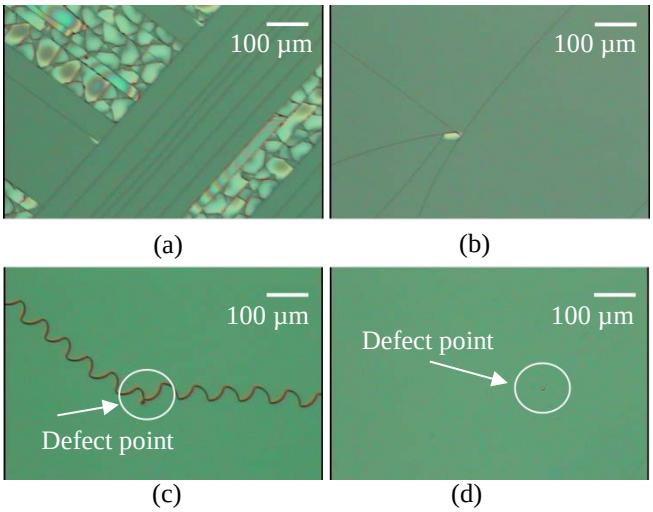


Fig. 4: Cracks on SiO_2 sol-gel surface with cooling down ramp of (a) 8°C/min, (b) 4°C/min, (c) 2°C/min, and (d) 1°C/min; with defect points on the surface circled in white.

Figure 4(a) shows multiple oriented cracks and delamination of the SiO_2 sol-gel layer when cooling down at a rate of 8°C/min which appears over the whole sample. Slowing the cooling rate down to 4°C/min in Fig. 4(b) produces lesser cracks that still occurs over the whole sample but no delamination is observed. Figure 4(c) with a rate of 2°C/min shows only zig-zag cracks that originate from point defects on the SiO_2 surface and is significantly less than in Fig. 4(a) and Fig. 4(b). Finally, Fig. 4(d) with a rate of 1°C/min shows no cracks on the surface even ones originating from point defects. The appearance of the zig-zag cracks as shown in Fig. 4(c) can be attributed to stress that accumulates at the defect point and then propagates through the sample in order to release the stress during the cooling down stage.

When depositing the ZnO sol-gel layer on top of the SiO_2 layer, cracks was still seen on the surface even after cooling the sample using a slow rate of 1°C/min. Therefore, in order to suppress the formation of cracks, a surface cleaning method for the SiO_2 layer was developed prior to depositing the ZnO sol-gel layer. Figure 5(a) shows the cracks on the ZnO layer when it was directly spin coated onto the SiO_2 layer cleaned only by using N_2 gas. The cracks cover the whole sample and originate from the samples edge and from defect points on the surface of the sample. When cleaning the sample using butanone and isopropanol, the number of cracks on increases as shown in Fig. 5(b). This increase can be attributed to butanone and isopropanol residues left on the sample which has a lower evaporation point and when heated can causes the top ZnO layer above to heat unevenly. Figure 5(c) shows minimal cracks on the ZnO surface when the SiO_2 layer was cleaned in a diluted BHF solution for 15 sec. It was observed that the cracks were significantly reduced and only propagates around a distance of 250 µm originating from point defects. It should be noted that the diluted BHF etches the SiO_2 layer slightly and can reduce its thickness. The best crack free surface was obtained by cleaning the SiO_2 surface with a photoresist remover as shown in Fig. 5(d).

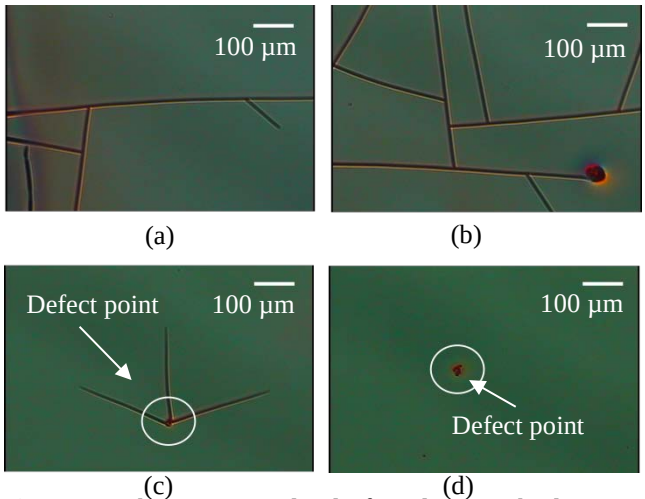
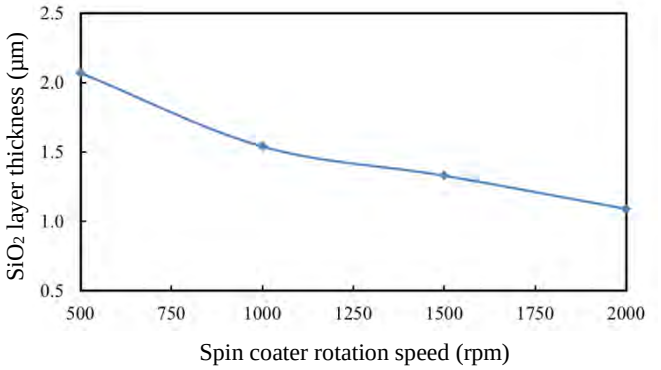


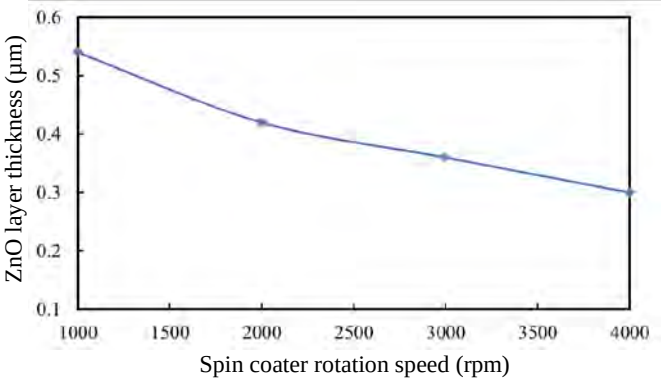
Fig. 5: Cracks on ZnO sol-gel after cleaning the lower SiO_2 surface using (a) N_2 gas blow dry, (b) butanol and isopropanol, (c) diluted BHF, and (d) photoresist remover; with defect points on the surface circled in white.

The photoresist remover is an excellent remover of organic and polymeric compounds and it can be seen that the deposited ZnO layer was crack free even with the presence of point defects.

By using a spin coater to deposit the sol-gel layers, the thickness of each layer can be controlled by optimizing the spin coater rotation speed. Because the sol-gel deposited layers require a thermal annealing process in order to solidify the layer, the thickness of the layers decrease during the annealing process. The thickness of the sol-gel layer will reduce firstly due to solvent evaporation during the first hot plate heating stage and secondly due to densify during the high temperature annealing stage. Therefore, all of the thickness measurements were taken after the high temperature annealing process was completed. As seen in Fig. 6(a), the SiO_2 sol-gel layer thickness varies from 2 µm when using a spin coater rotation speed of 500 rpm to 1 µm when using a spin coater rotation speed of 2000 rpm. Similarly, Fig 6(b) shows that the ZnO sol-gel layer thickness varies from 540 nm when using a spin coater rotation speed of 1000 rpm to 300 nm when using a spin coater rotation speed of 4000 rpm. Therefore, by optimizing the spin coater rotation speed, we can determine and accurately control the thickness of the SiO_2 and ZnO layers.



(a)



(b)

Fig. 6: Thickness of (a) SiO_2 and (b) ZnO sol-gel layers vs. spin coater rotation speed (rpm).

Based on the results obtained, a multi-layer SiO_2 cladding and ZnO core layer was successfully fabricated using the all sol-gel fabrication technique as shown in Fig. 7. An optical microscope was used to observe the thickness of each layer and to observe that the layers were crack free. In order to achieve a crack free surface, the SiO_2 layer requires a well-controlled slow 1°C/min cooling down ramp from the annealing temperature of 500°C down to room temperature. Correspondingly, to achieve a crack free ZnO sol-gel core layer, it was found that a surface cleaning preparation procedure consisting of cleaning the SiO_2 layer using a photoresist remover was also required.

The thickness of the SiO_2 layers were designed to be 1.5 µm thick and this was achieved by using a spin coater rotation speed of 1000 rpm. Similarly, ZnO core layer was designed to be 300 nm and this was achieved by using a spin coater rotation speed of 4000 rpm.

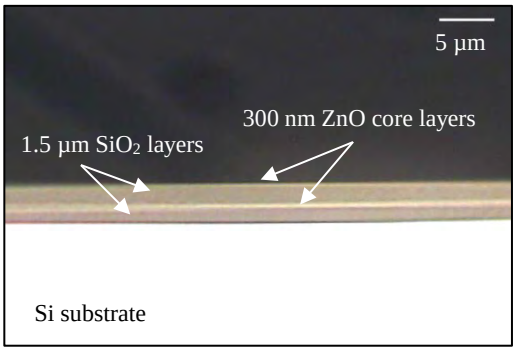


Fig 7: Multi-layer ZnO core and SiO_2 cladding and core separation layer for vertical coupling waveguide.

4. Conclusion

The main objective of this work is to demonstrate the capability to stack different refractive index materials on top of one another as well as to control the thickness of each individual layer in order to facilitate fabrication of photonic devices such as the vertical coupler. The use of sol-gel deposition as in our work provides a simple, effective method to fabricate these layers. We have demonstrated a novel fabrication technique by using an all sol-gel method on bulk Si to create a multi-layer structure. The novel fabrication technique enables the stacking of different refractive index sol-gel materials to realize a vertical coupling waveguide. To obtain a 1.5 µm thick SiO_2 layer, a spin coater rotation speed of 1000 rpm was used. Similarly, to obtain a 300 nm thick ZnO core layer, a spin coater rotation speed of 4000 rpm was used.

Similarly, the issues of cracks were resolved through a slow cooling down ramp of 1°C/min after annealing and the use of photoresist remover as a surface cleaning treatment. Further fabrication and measurement for the vertical coupler waveguide will be reported later.

The simplicity of the processes and the capability to control the device parameters suggests that the method described in this paper are promising for large scale fabrication of integrated photonic circuits.

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