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Zang, Chengjie
System LSI Research Center

Ishihara, Tohru
System LSI Research Center

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An Implementation of Energy Efficient Multi-performance Processor for Real-Time Applications

Chengjie Zang
System LSI Research Center,
Kyushu University, 3-8-33, Momochihama,
Sawara-ku, Fukuoka,814-0001 JAPAN
Email: zang@slrc.kyushu-u.ac.jp

Tohru Ishihara
System LSI Research Center,
Kyushu University, 3-8-33, Momochihama,
Sawara-ku, Fukuoka,814-0001 JAPAN

***Abstract*— Multi-performance processor reduces the energy consumption by using lower supply voltage in CPU core and reducing the number of cache ways activated when applications do not need the peak performance of the processor. In this paper, the design results of a multi-performance processor is presented, which has two processing elements, PE-H and PE-M. The design flow of finding minimum V_{DD} for PE-M is shown. The processor is implemented by commercially available 0.18 μm process technology. PE-H and PE-M are synthesized using cell libraries characterized with 1.8V and 1.0V, respectively. Post-layout simulation is performed to evaluate energy consumption and performance of the processor. The experimental results show that a PE with 1.0V supply voltage takes more than 50% smaller energy consumption and longer execution time compared with those of a PE with 1.8V supply voltage. The experiments also demonstrate that the selective-way instruction cache contributes for saving the energy consumption. The results show that lower associative cache consumes lower energy while takes larger execution time. The energy efficiency of the selective-way cache technology depends on the type of benchmark program. At last, the paper shows the specifications of the processor. The processor with two PEs can save the energy consumption without losing peak performance of the processor. The area overhead for having two PE cores is only 6.88% of the total chip area.**

I. Introduction

Dynamic voltage and frequency scaling (DVFS) is one of the most popular approaches for reducing the energy consumption of microprocessors [5], which dynamically changes the supply voltage to the lowest value for saving the dynamic power consumption while it ensures a correct operation of the microprocessors. The DVFS technology usually uses a delay chain or a look-up table to determine the lowest voltage for an error-free operation at a particular frequency. In past years, a lot of DVFS processor architectures have been proposed [6][7]. However, only a few of them are used in real-time systems. One major reason is the large overhead for dynamically changing the supply voltage and the clock frequency. Reliability issue is also very serious for DVFS processors in the latest process technology like 65nm process. In our group, a new processor architecture which can be used as a design alternative for the DVFS processors is proposed [1]. We refer to the processor as a multi-performance processor. The processor consists of multiple same-ISA PE-cores and resizable set-associative cache memories as presented in [2]. The cache memories are shared by the PE-cores. Clock speeds and energy consumptions of PE-cores are different from each other. Only a single PE-core is selected to run at a time and the other PE-cores are deactivated by clock gating and signal gating. In this paper, a multi-performance processor is implemented with $0.18\mu m$ CMOS process technology. The change of the active PE-core can be completed within a few microseconds, which is suitable for the real-time applications.

In traditional DVFS processors, a CPU core is designed to correctly work for multiple voltage conditions. In this case, a critical path may be different along supply voltage even in a same chip. This indicates that the traditional DVFS processor chip is not optimally synthesized for each supply voltage. Therefore, it is less power efficient than the dedicated processor core which is optimized for a specific supply voltage. Unlike the conventional DVFS processors, our PE-cores are optimally designed at the pre-silicon design phase for the specific supply voltage at the cost of chip area. As a result, our PE-core is more power efficient. In the proposed processor, PE-cores are functionally equal to each other while run on different supply voltages and different frequencies. The power consumption of the processor can be saved by dynamically selecting the active PE-core and a cache associative value based on the criticality of the task and the proximity of the deadline.

The rest of this paper is organized as follows: Section 2 briefly introduces the architecture of the multi-performance processor, the selective cache way architecture, the level shifter design and the physical implementation flow of multi-V_{DD} processors, including the library characterization and the minimum supply voltage decision method for PE-M. Section 3 shows the experimental results including performance of low-V_{DD} operation, power and energy consumption comparisons for different PE cores, the efficiency of the selective cache way architecture and specifications of the multi-performance processor. The conclusion is described in the last section.

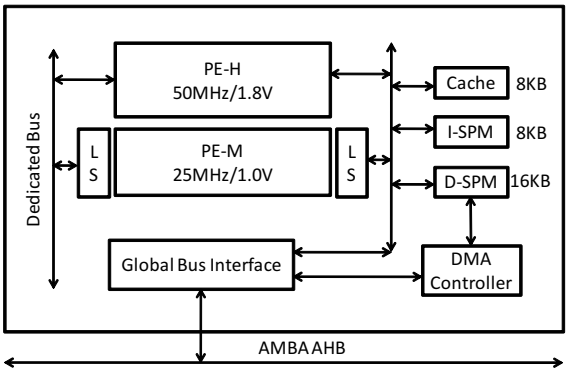

Fig. 1. Block diagram of the dual-PE processor.

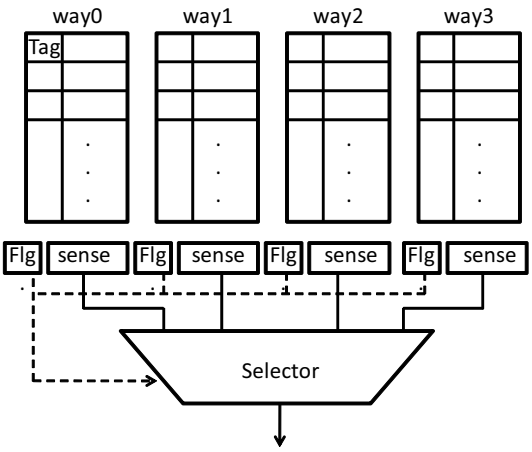

Fig. 2. A four-way set associative cache with selective cache ways.

II. Multi-performance processor design

A. Multi-performance Processor Architecture

The multi-performance processor is designed based on the Media embedded processor (MeP) originally developed by Toshiba [8] and which is modified to include two PEs, PE-H and PE-M, as shown in Fig.1. In the processor, PE-H runs at high clock frequency and is implemented using an original standard cell library which is supposed to use a normal 1.8V voltage supply. PE-M runs at low clock frequency and is implemented with a cell library characterized by lower supply voltage than 1.8V. In the processor, only one PE can be activated for running at a time and the entire clock frequency of the processor is set to be the same frequency with the active PE. A special register is designed in the last address of a data scratchpad memory to specify the active PE-core. Thus programmer can explicitly specify which PE core is activated for running by a store instruction. For switching PE-cores, the data of internal registers are transferred between PEs through a dedicated internal bus or a data scratchpad memory.

A 4-way set-associative instruction cache is designed based on the selective cache way architecture which is proposed in [2]. The selective cache way technology can disable one or more ways of the cache memory when full cache associativity is not required to achieve good performance. The cache memory has extra flag bits to indicate the ways which should be active or not, as shown in Fig.2. For the flag, value 0 means that the corresponding cache way is not active. In this case, the processor does not use the cache way and all the references to that way will result in a cache miss. Value 1 means that the way is active and which is treated as a normal cache for accessing. The values of these flags are stored in a series of registers and therefore, programmer can explicitly specify the cache ways which are activated.

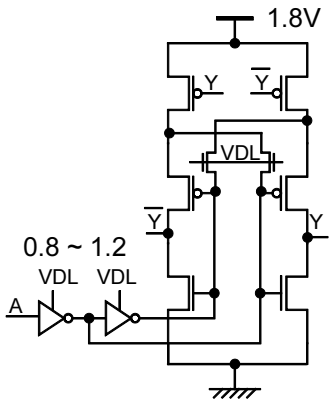

Fig. 3. Schematic of the level shifter circuit.

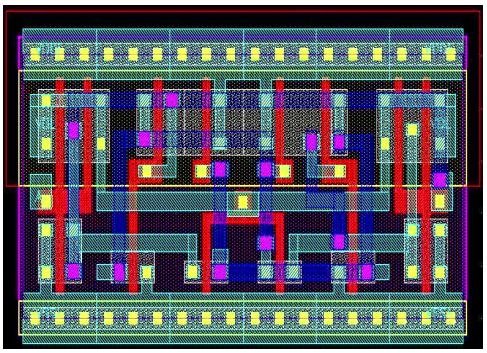

Fig. 4. Layout of the level shifter circuit.

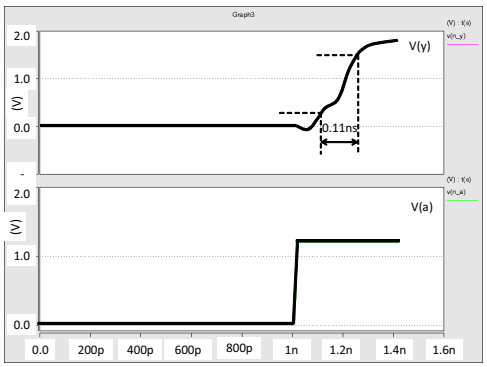

Fig. 5. Rising curve of the level shifter.

B. Level Shifter

In the processor, PE-M uses a low supply voltage, which is different from the other parts. Since SRAM is very sensitive to noise, on-chip caches and scratchpad memories use the highest supply voltage available to preserve the reliability of the processor chip. To correctly make interface from lower voltage block to higher voltage blocks, it is necessary to convert the signal voltage level between low voltage block and conventional voltage blocks. Therefore, in the processor, a level shifter circuit is designed for transporting signals among different voltage blocks. The up-shifter converts a low voltage level in the range of 0.8V∼1.2V up to a high voltage level of about 1.8V. Similarly, the down-shifter converts a high voltage signal to a low voltage signal. The level shifter is designed based on the circuit from work [4]. Fig.3 and Fig.4 show the transistor level circuit and the layout schematic of the level shifter, which has two supply voltages VDL and V_{DD}. V_{DD} is the supply voltage from standard library and VDL is the low supply voltage for PE-M. The circuit can generate 1.8V output Y from 0.8V∼1.2V input A. The area of level shifter is about 5.1 times larger than that of the minimum inverter in 1.8V library. Fig.5 the shows rising curves of the level shifter. In the figure, output Y with 1.8V is generated by an input A with 0.8V∼1.2V. The rising latency of Y is 0.11ns and which is about 3.6 times larger than that of the minimum inverter in 1.8V library.

C. Multi-V_{DD} Processor Design Flow

The processor is implemented using 0.18 μm CMOS technology, which has a set of standard cells with 1.8V supply voltage. In the processor, PE-H is designed using the original standard cells which are characterized with 1.8V. To reduce dynamic and leakage power consumptions, PE-M uses supply voltage which is lower than 1.8V. Thus, PE-M is selected to run at low supply voltage if slack time of task is large enough. The PE-M and PE-H modules are synthesized from the same RTL description. However, the synthesis flows are different from each other. The processor except PE-M runs at 1.8V supply voltage. To find the optimal supply voltage of PE-M, the 0.18 μm cell library is characterized with different supply voltages. The voltage of PE-M is optimized by the following steps:

- **Cell Library Characterization**
  Liberty NCX [3] of SYNOPSYS is used to characterize the 0.18 μm CMOS standard cell library with different supply voltages ranging from 0.6V to 1.6V. PEs are synthesized, placed and routed using the libraries. For each PE synthesized with a library characterized by a specific supply voltage, we find the minimum critical-path delay.
- **Frequency Decision of PE-H**
  At first, both of PE-H and PE-M are synthesized, placed and routed by using 1.8V library. In our design, the maximum clock frequency of the processor working with PE-H is 90 MHz.

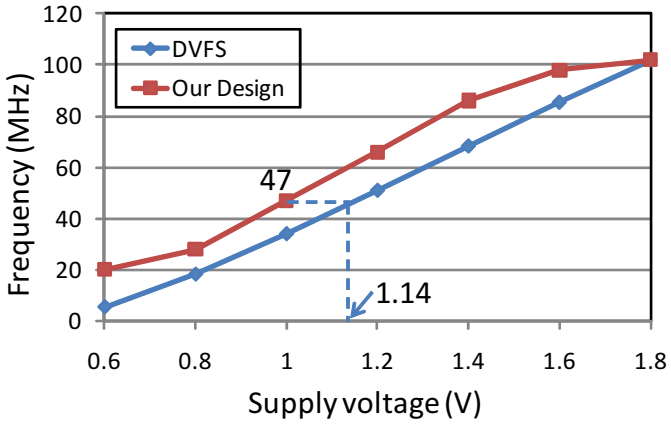

Fig. 6. Performance of low-V_{DD} operations.

- **Frequency Decision of PE-M**
  Set the target clock frequency of the processor working with PE-M as half of PE-H, 45MHz.
- **Voltage Optimization of PE-M**
  Since the target clock frequency of the processor working with PE-M is decided as 45MHz, next step is to find the minimum supply voltage for PE-M, which guarantees correct operations of the PE-M with the target clock frequency (i.e., 45MHz). To this purpose, different libraries are used for logic and layout synthesis. As shown in Fig. 6, the minimum supply voltage of the PE-M is less than 1.0V. Therefore, we use a library characterized with 1.0V for synthesizing the PE-M.

III. Experimental Results

This part shows experimental results based on post-layout simulations of the multi-performance processor. The following subsection shows the maximum operating frequencies of the processor working with low-V_{DD} conditions, where the PE-M is implemented using a cell library characterized with lower supply voltage than 1.8V. Power and energy consumption results are also evaluated by executing multiple benchmarks on the processor. At last, the specifications of the processor chip are presented.

A. Performance of Low-V_{DD} Operation

The standard 1.8V library is characterized by NCX with different supply voltages ranging from 0.6V to 1.6V. Logic synthesis and layout synthesis are done by using these libraries. The results are shown in Fig.6. In the figure, curve of "our design" shows the result of PE-M based on a layout synthesized with different libraries. As can be seen from the figure, the maximum frequency is a convex function of the supply voltage. To compare with DVFS technology, one critical path is extracted from a design synthesized by a 1.8V library and the path is simulated with different supply voltages using HSPICE of SYNOPSYS, as shown in the figure. Since the DVFS-capable processor is typically synthesized with a single maximum supply voltage, the design runs with other

supply voltages may not achieve the best performance. As a result, the maximum clock frequency available for the DVFS-capable processor is a linear function of the supply voltage as shown in Fig.6. For example, to achieve 45MHz performance, our design runs with 1.0V supply voltage while the DVFS technology needs 1.14V to achieve the same performance. More specifically, since the energy consumption of a processor implemented with CMOS technology is proportional to the square of the supply voltage, our design is 30% more energy efficient than the typical DVFS processor.

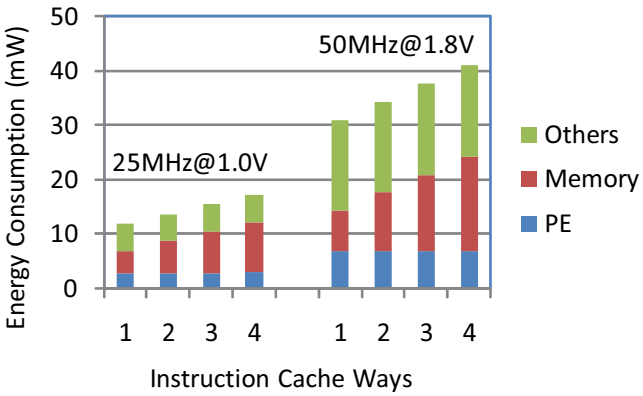

Fig. 7. Power consumption results of ADPCM.

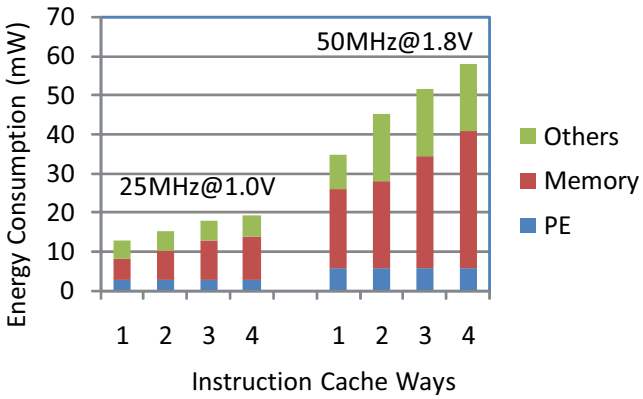

Fig. 8. Power consumption results of MPEG.

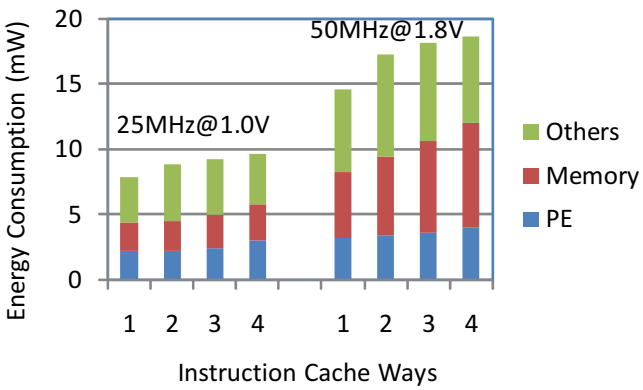

Fig. 9. Power consumption results of JPEG.

B. Power Consumption Results

By the multi-V_{DD} design methodology, the PE-M of processor is implemented with a library characterized by a 1.0V supply voltage. In the experiments, only one PE core is selected to run at the benchmark initialization phase. The activated cache ways are also fixed at the initialization phase and are unchanged during the program execution. Therefore, the power consumption of PE-H and PE-M are evaluated separately. Each kind of PE is evaluated with different cache configurations ranging from 4-way set-associative to direct mapped caches. The processor is evaluated by post-layout simulation. Parasitic parameters are extracted and back annotated for the post-layout simulation. We selected three benchmark programs in media applications, ADPCM, MPEG2 encoder (MPEG) and JPEG decoder (JPEG). The benchmarks run on the processor to collect switching activities separately. In the experiments, Verilog-XL of Cadence is used to collect switching activities and to store them in a switching activity interchange format (SAIF) data file. The SYNOPSYS Prime-Power based power evaluation tool is used to calculate the power consumption.

The benchmark programs run on PE-H at 50MHz and PE-M at 25MHz, respectively. Fig.7, Fig.8 and Fig.9 show the results of the power consumption of these benchmarks running on the processor with different PEs activated and different cache configurations. The results show that for the same number of cache ways, PE with low supply voltage consumes less power than that with high supply voltage, while the clock frequency shows inferior to PE with high supply voltage. Regarding the cache power consumption, a lower associative cache way takes less power consumption compared with the higher associative cache. This provides a chance to save power consumption for tasks with large slack time by reducing the number of cache ways activated without violating deadlines of the tasks.

C. Energy Consumption Results

The energy consumption and execution time of the benchmarks running on the processor are also evaluated. The results are shown in Fig.10. Bar charts and line charts show the energy consumption and execution time, respectively. The same benchmark program runs on PE-H and PE-M separately. The PE with a low supply voltage works at low clock frequency and thus it takes longer time to complete the same program than the PE with high supply voltage. However, the energy consumption of the PE with low supply voltage is smaller than that of the PE with high supply voltage. This is because the power consumption of a PE with low supply voltage is much smaller than that of a PE with high supply voltage. Regarding the selective-way cache, the energy efficiency depends on the type of benchmark. Direct-mapped cache (i.e., one-way cache) takes the smallest energy consumption for ADPCM and JPEG benchmarks. While for benchmark of MPEG, the case of 2-way instruction cache consumes the smallest energy. System designer can save the cache energy consumption by appropriately selecting the number of cache ways according to the target application programs.

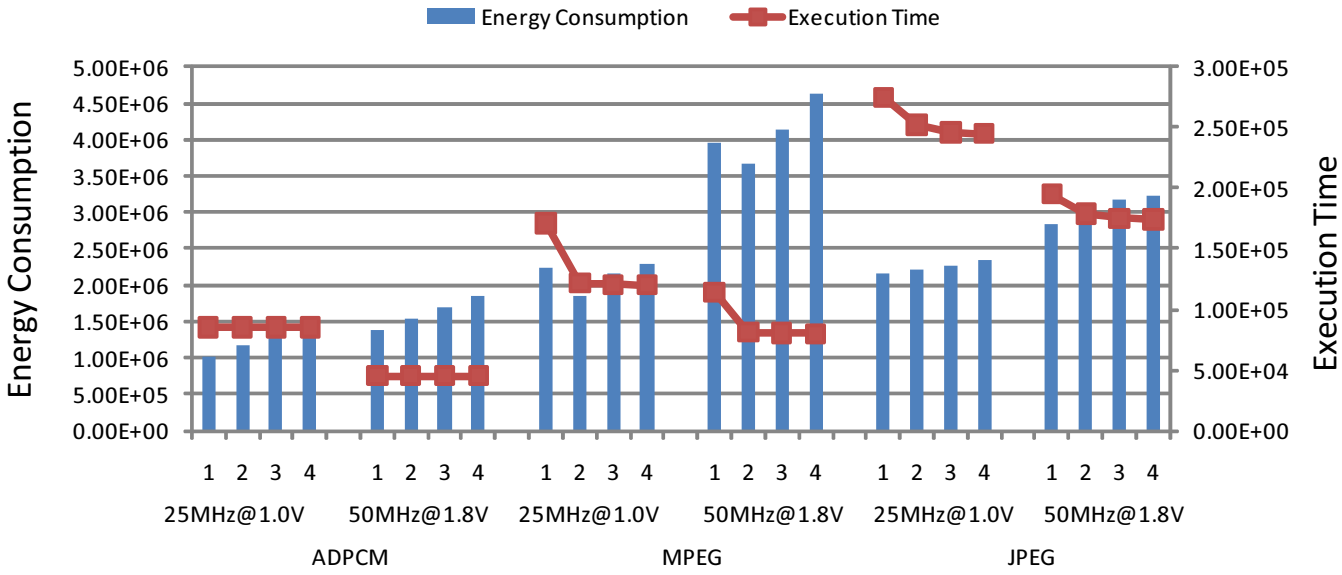

Fig. 10. Energy consumption of dual-PE processor.

D. Area Specifications of Processor

The processor is designed using commercially available 0.18 μm technology. PE-H and PE-M are worked correctly at 50MHz with 1.8V and 25MHz with 1.0V, respectively. The chip layout and chip area specifications are shown in Fig.11 and Table I, respectively. In the layout, the PE with high supply voltage (i.e., PE-H) is flattened during a logic synthesis process. Therefore, PE-H is not apparent in the chip layout image.

Multi-performance processor can reduce power consumption by assigning the PE with low supply voltage when the applications do not need the peak performance. Employing an additional PE with low supply voltage does not involve very large area cost. As shown in Table1, the area of PE-M is only 6.88% of the total chip.

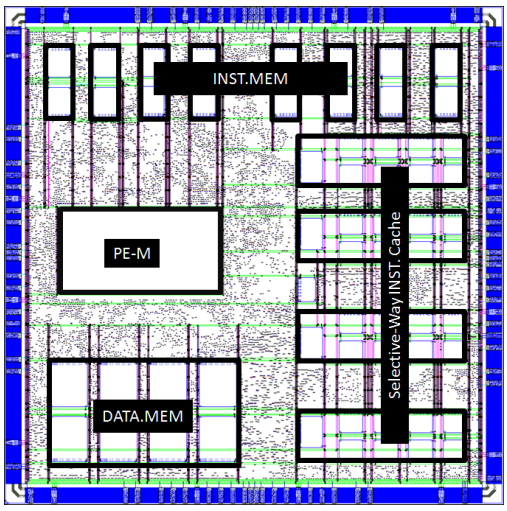

Fig. 11. Layout of dual-PE processor (5mm x 5mm).

IV. Summary and Conclusions

In this paper, design results of a multi-performance processor are presented. Two processing elements (PE) alternatively being active to execute tasks with different slack margins. The PE-H is designed by library with 1.8V supply voltage and PE-M is designed by library with 1.0V supply voltage. The multi-V_{DD} design flow and the level-shifter design are also proposed. Power and energy evaluation of the total processor is done by post-layout simulation with back annotated parasitic parameters. The experimental results show that the PE with low supply voltage takes smaller power consumption, smaller energy consumption and larger execution time compared with PE of high supply voltage. In addition, the experiments also checked the efficiency of the selective cache way architecture and the results show that lower associative way consumes lower power while takes longer execution time and the efficiency of the selective cache way technology depends on different applications.

TABLE I

Area specifications of processor.

Module Name	Area	Percentage
PE-H	1.58 mm^2	6.32%
PE-M	1.72 mm^2	6.88%
Data Memory	1.36 mm^2	5.44%
Instruction Memory	1.15 mm^2	4.6%
Instruction Cache Memory	2.03 mm^2	8.12%
I/O Buffer	2.99 mm^2	11.96%
Other	14.17 mm^2	56.68%
Total	25 mm^2	100%

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