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Yoshimura, Masayoshi
Faculty of Information Science and Electrical Engineering, Kyushu University : Assisitant Professor

Ogawa, Hiroshi
Graduate School of Industrial Technology, Nihon University | College of Industrial Technology, Nihon University : Professor

Hosokawa, Toshinori
日本大学生産工学部数理情報工学科 : 教授

Yamazaki, Koji
School of Information and Communication, Meiji University

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Evaluation of Transition Untestable Faults Using a Multi-Cycle Capture Test Generation Method

Masayoshi YOSHIMURA*, Hiroshi OGAWA†, Toshinori HOSOKAWA‡ and Koji YAMAZAKI§
*Faculty of Information Science and Electrical Engineering, Kyushu University
Nishi-ku, Fukuoka, 814–0001, Japan, Email: yosimura@ait.kyushu-u.ac.jp
†Graduate School of Industrial Technology, Nihon University, Narashino, Chiba 275-8575, Japan
‡College of Industrial Technology, Nihon University, Narashino, Chiba 275-8575, Japan
§School of Information and Communication, Meiji University, Suginami-ku, Tokyo 168-8555, Japan

***Abstract*—Overtesting induces unnecessary yield loss. Untestable faults have no effect on normal functions of circuits. However, in scan testing, untestable faults may be detected through scan chains. Detected untestable faults cause overtesting. Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults. Uncontrollable faults may be detected under invalid states through scan chains by shift-in operations. Unobservable faults cannot be observed at primary outputs, but their effects may be propagated to scan flip-flops. Thus, unobservable faults may be detected through scan chains by shift-out operations. Several methods to reduce the number of detected untestable faults were recently proposed. These methods identify invalid states and generate test patterns avoiding invalid states. As the result, the number of detected uncontrollable faults was reduced. However, they cannot reduce the number of detected unobservable faults. In this paper, both uncontrollable and unobservable faults are identified using a multi-cycle capture test generation method. We evaluate the relationship between the numbers of untestable faults and the number of time expansions for ISCAS'89 benchmark circuits, and also evaluate factors that untestable faults are identified.**

I. Introduction

Recently, many design methodologies have been developed to resolve the yield loss problem. One of methodologies for yield loss is to improve the test quality on manufacturing VLSIs.

Currently, Design for Testability (DFT) is one of methods to improve the test quality for VLSIs. A scan design method [1] is one of popular DFT methods for logic circuits. In full scan design method, all Flip-Flops (FFs) are replace with scan FFs. A scan FF is equivalent to a primary input and a primary output at the scan mode. In full scan designed circuits, each test pattern can be set to scan FFs using scan chains. However, in scan testing, untestable faults may be detected through scan chains. On the other hand, Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults. Uncontrollable faults may be detected under invalid states through scan chains by shift-in operations. Unobservable faults cannot be observed at primary outputs, but their effects may be propagated to scan flip-flops. Thus, unobservable faults may be detected through scan chains by shift-out operations. Detected untestable transition faults cause overtesting[2]. In this paper, our target fault model is a transition fault model.

Overtesting induces unnecessary yield loss. Untestable faults have no effect on normal functions of circuits. Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults. First, uncontrollable faults may be detected under invalid states through scan chains by shift-in operations. Second, unobservable faults cannot observe at primary outputs, but their effects may be propagate to scan flip-flop. Thus, unobservable faults may be detected through scan chains by shift-out operations. Several methods[3][4][5] to reduce the number of untestable faults were proposed. These methods identify invalid state and generate test pattern avoid invalid states. As the result, the number of detected uncontrollable faults was reduced. However, they cannot reduce the number of detected unobservable faults. These methods cannot reduce the number of detected unobservable faults.

Multi-cycle capture test methods [6] generate test patterns with multiple capture cycles. Circuits under the test sequentially operate with test sequences generated by multi-cycle capture test generation (MCTG). Let k be the number of sequential operations. If k is larger, the test generation complexity becomes one for sequential circuits and it is difficult to generate test sequence. On the other hand, If k is smaller, the test generation complexity is nearly equal to one for combinational circuits and it is easy to generate test sequence. When k is large, many untestable faults can be identified. A MCTG method identifies not only faults detected under only invalid states but also faults whose effects cannot be observed at primary outputs.

In this paper, we evaluate the relationship between the number of untestable faults and the number of time expansions(k). Next, we evaluate factors that untestable faults are identified. We classify the factors for untestable fault identification into four categories.

1) the condition of primary inputs controllability
2) the condition of primary outputs observability
3) the condition of justification
4) the condition of propagation for fault effects

This paper is organized as follows. In Section 2, preliminaries are introduced to transition fault model, untestable faults, multi-cycle capture test and detection of untestable

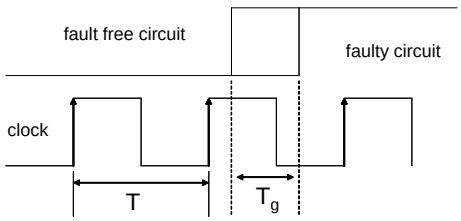

Fig. 1. A general transition fault model

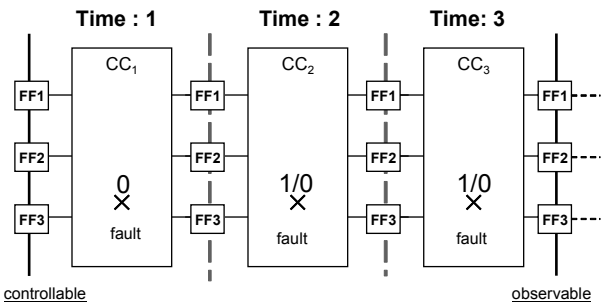

Fig. 2. A 2 cycle transition fault

faults. In Section 3, we propose factors that untestable faults are identified and classify the factors for untestable fault identification. Experimental results for ISCAS'89 benchmark circuits are shown in Section 4. Finally, Section 5 concludes the paper.

II. Preliminaries

In this section, we introduce transition fault model, untestable faults, multi-cycle capture test and the detection of untestable faults using scan chains.

A. Transition fault model

Let T be clock period, T_g be delay time of a path without transition fault and Del be additional delay time for a transition fault in Figure 1. If $Del > T - T_g$, the effect of transition faults propagate FFs. In broadside test which are equal to 2 cycle capture test, Del which can be observed FFs is from $2T - T_g$ to $T - T_g$. Figure 2 shows a 2 cycle transition fault model on 3-times expansion model.

In Figure 2, Del which can be observed FFs is from $3T - T_g$ to $T - T_g$ using 3 cycle capture test. Because we aim to reduce the overtesting of broadside testing, our target delay fault size Del is is from $2T - T_g$ to $T - T_g$ in this paper.

B. Untestable faults

Untestable faults are classified into combinational redundant faults sequentially redundant faults. The combinational redundant faults cannot be detected by any combinational test patterns. The sequential redundant faults do not affect the functions of circuits. Methods to identify these untestable faults use sequential ATPG [7][8][9] based on time expansion models [10] and invalid states identification [11][12].

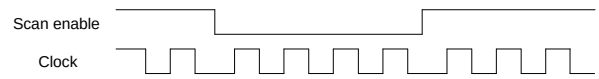

Fig. 3. A waveform of multi-cycle capture test sequence

C. Multi-Cycle Capture Test

Multi-cycle capture test methods for transition faults [6][13][14] generate test sequences with multiple capture cycles. Circuits under the test sequentially operates for two or more clock cycles by the generated test sequence. Let k be the number of sequential operations. Fig. 3 shows a waveform of $k = 4$ cycle capture test sequence. There are four capture clock cycles on one capture cycle in Fig. 3. If k is larger, the test generation complexity becomes one for sequential circuits. When k is large, the possibility of setting invalid states to scan FFs by multi-cycle capture test sequence is low. The possibility of detection of untestable faults by multi-cycle capture test sequences is low and many untestable faults can be identified. However, the MCTG is difficult for k-time expansion model. On the other hand, if k is smaller, the test generation complexity is nearly equal to one for combinational circuits. When k is small, the possibility of setting invalid states to scan FFs by multi-cycle capture test sequences is high. The possibility of detection of untestable faults by multi-cycle capture test sequences is high.

The relationship between k which is the number of time expansion and difficulty to generate multi-cycle test sequence is considered. If k is larger, the number of time expansions is large. Therefore, the size of test generation model is bigger and test generation is difficult. If k is smaller, the number of time expansion is small. Therefore, the size of test generation model is smaller and test generation is easy.

Next, the relationship between k and valid / invalid states is considered. If k is larger, the possibility of valid states after sequential operations of test sequences generated by multi-cycle capture test is higher. It is possible to transfer from invalid states to valid states. However, it is impossible to transfer from valid state to invalid state using sequential operations.

D. Detection of untestable faults using scan chains

On full scan designed circuits, each test pattern can be set to scan FFs and be observed to scan FFs through scan chains. A scan FF is equivalent to a primary input and a primary output at the scan mode. The test generation for full scan designed circuits is easy for ability to set each test pattern to scan FFs. On the other hand, untestable faults may be detected through scan chains. Detected untestable faults cause overtesting. Untestable faults consist of uncontrollable faults, unobservable faults, and uncontrollable and unobservable faults.

Invalid states [11][12] cannot reach from any valid states using sequential operation. However, invalid states can be set using only scan chains. Uncontrollable faults may be detected under only invalid states through scan chains by

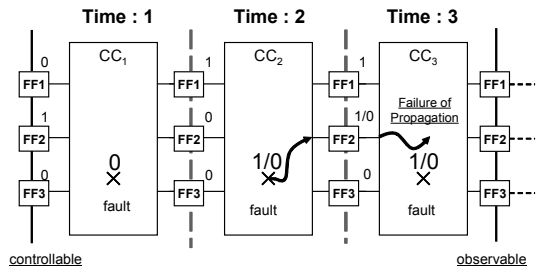

Fig. 4. A untestable transition faults on 3-time expansion model

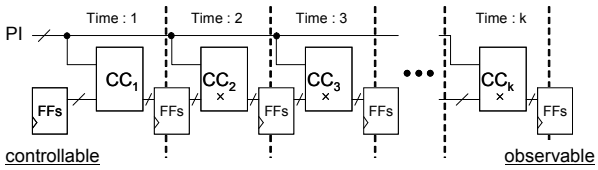

Fig. 5. k-time expansion model for transition faults

shift-in operations. Unobservable faults cannot be observed at primary outputs, but their effects may be propagated to scan flip-flops. Thus, unobservable faults may be detected through scan chains by shift-out operations.

A transition fault is detected with 2 cycle capture test pattern and may not be generated test pattern which is detected with 3 cycle capture test pattern. There are two cases. Fist, the fault effects cannot propagate to observable scan flip-flops. Second, states to detect the fault cannot be justified. This fault cannot be identified as untestable fault using 2 cycle capture test generation. Fig. 4 shows a untestable transition faults on 3-times expansion model.

III. An Evaluation Method of Transition Untestable Faults

A. k-time expansion model for transition faults

In k-time expansion model, pseudo primary inputs are outputs of scan FFs at time frame 1, pseudo primary outputs are inputs of scan FFs at time frame k, and combinational circuits are expanded sequential circuits to k-times frame. It is difficult to synchronize the frequencies of primary inputs and primary outputs on ATE with the frequency of internal FF's. Thus, the value of primary inputs is fixed at all the time frame and the effect of faults cannot be observed on primary outputs in k-time expansion model. Figure 5 shows k-time expansion model for transition faults.

B. Test generation method using multi-cycle capture test

In a transition fault test generation method using multi-cycle capture test, transition faults are detected using k-time expansion model. Target circuits are full scan designed circuits. Figure 6 shows an example of full scan designed circuits. In Fig. 6, Z, $Y1_D$ and $Y1_Q$ denote primary outputs, inputs of FFs and output of FFs, respectively. A transition fault test generation method using multi-cycle capture test transforms

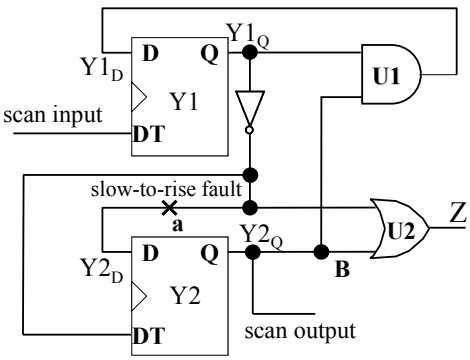

Fig. 6. full scan circuits

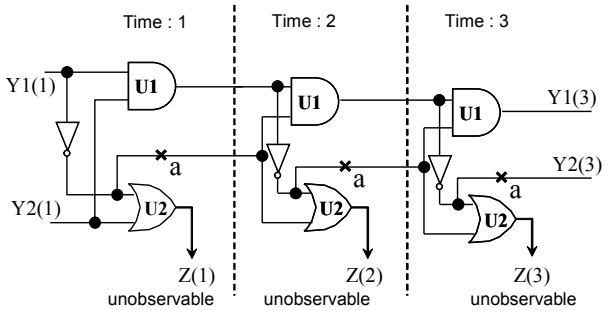

Fig. 7. A 3-time expansion model

full scan designed circuits in Fig. 6 to the 3-time expansion model in Fig. 7. In Fig. 7, $Z(i)$ denote primary outputs for time $i(1 \leq i \leq 3)$, $Y1(1)$ and $Y2(1)$ denote pseudo primary inputs, $Y1(3)$ and $Y2(3)$ denote pseudo primary outputs. The fault model assumes a single transition fault model in this paper. There are multiple faults at a corresponding signal line each time frame.

C. Untestable fault identification

The time frame where transition faults are activated influences the fault classification results. Figure 6 shows an example of full scan designed circuits. Figure 8 shows 2-time expansion model of Fig. 6. Figure 7 shows 3-time expansion model of Fig. 6. The value of primary inputs is fixed at all the time frame and the effect of faults cannot be observed on primary outputs in the time expansion model. The slow-to-rise faults of line a on Time 2 in Fig 8 and Time 2, 3 in Figure 7 are target faults of MCTG.

First, the slow-to-rise fault of line a on Time 2 in Fig 8 is targeted. It is necessary that assignment values of $Y1(1) = 1$ and $Y2(1) = 0$ to excite the fault. The effect of the slow-to-rise fault on line a is propagated to $Y2(2)$ by those assignment values. Thus, the slow-to-rise fault of line a on Time 2 in Fig 8 can be detected.

Second, the slow-to-rise fault of line a on Time 3 in Fig 9 is targeted. It is necessary that assignment values of $Y1(1) = 1$ and $Y2(1) = 1$ to excite the fault. On Time 3, the value of line a changes from 0 to 1. The effect of the slow-to-rise fault of

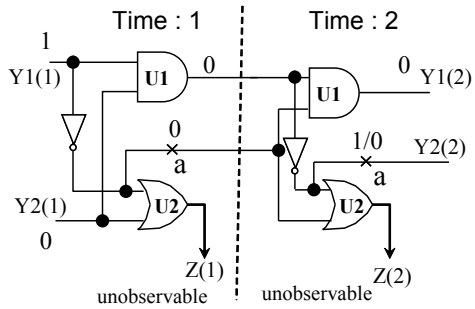

Fig. 8. A test generation for 2-time expansion model

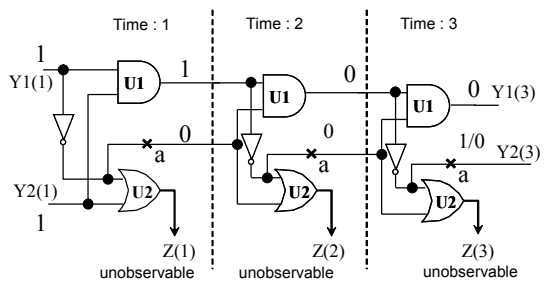

Fig. 9. Fault excitation on Time 3

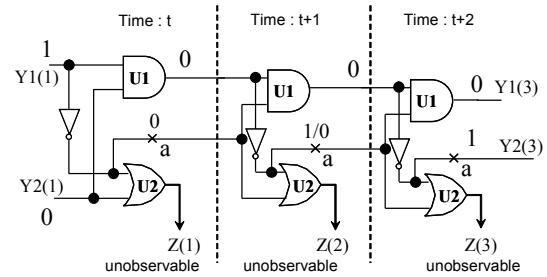

Fig. 10. Fault excitation on Time 2

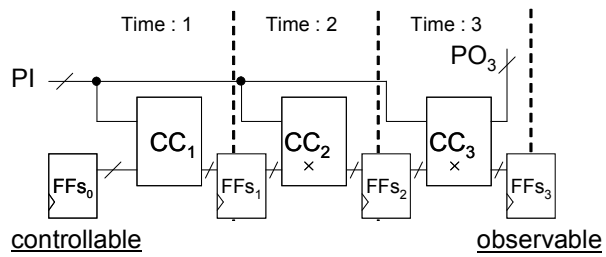

Fig. 11. A 3-time expansion model with PO_3

line a on Time 3 is propagated to $Y2(3)$ by those assignment values. The effect of the slow-to-rise fault of line a on Time 2 is not activated because the value of line a does not change from 0 to 1 on Time 2. Thus, the slow-to-rise fault of line a on Time 3 in Fig 9 can be detected.

Finally, the slow-to-rise fault of line a on Time 2 in Fig 10 is targeted. It is necessary that assignment values of $Y1(1) = 1$ and $Y2(1) = 0$ excite the fault. On Time 2, the value of line a changes from 0 to 1. However, the effect of the slow-to-rise fault of line a on Time 3 is not propagated to $Y1(3)$ or $Y2(3)$. Because the input value of the AND gate U1 is 0 on Time 3. Thus, the slow-to-rise fault of line a on Time 2 in Fig 10 cannot be detected and can be identified as untestable faults.

In these results, the slow-to-rise fault classification results of line a on Time 2 and that on Time 3 are different. When a fault is identified as untestable fault at least one excitation time, the fault is classified as untestable fault[9]. Therefore, it is necessary to excite faults on each time frame in order to identify untestable fault correctly.

D. Test generation for transition faults in k-time expansion models

A Soc (System-on-a-Chip) has multi clock domains. The test patterns for transition faults in each clock domain are generated. When FFs in the same clock domain capture the effects of transition faults, transition faults influence the circuit. Even if the effects of transition faults propagate to FFs in other clock domain or primary outputs, these transition faults do not generally be detected. The effects of transition fault in a clock domain do not always influence the circuit of other clock domain and systems which connected to primary outputs. Therefore, the value of primary inputs is fixed at all the time frame and the effect of faults cannot be observed on primary outputs in broad-side model.

Figure 11 shows a 3-time expansion model with PO_3 on Time 3. In Fig 11, when an effect of the transition fault which excited on Time 2 is captured a FFs_2 on Time 2 and the effect propagate to PO_3 on Time 3, the effect of the transition fault can be detected at PO_3. Because the value of FFs_2 on Time 2 propagates to PO_3, the effects of the transition fault do not propagate to PO_3. Therefore, if $a < b$, when effects of the transition fault which excited on Time a is captured FFs on Time a and the effect propagate to PO on Time b, the effect of the transition fault can be detected at PO on Time b.

In time expansion model whose k is 3 or more, the value of primary inputs is normally fixed at all the time frame. It is difficult to synchronize the frequencies of primary inputs on ATE with the frequency of internal FF's. However, the value of a primary input is not always fixed on sequential operation. Therefore, the condition that the value of primary inputs is fixed at all the time frame may be superfluous when untestable faults are identified.

There are four condition models for time expansion model whose k is 3 or more.

- **Model A** the value of primary inputs is fixed and the effects of transition faults cannot be detected at primary outputs.
- **Model B** the value of primary inputs is **not** fixed and the effects of transition faults cannot be detected at primary outputs.
- **Model C** the value of primary inputs is fixed and the effects of transition faults **can** be detected at primary outputs.

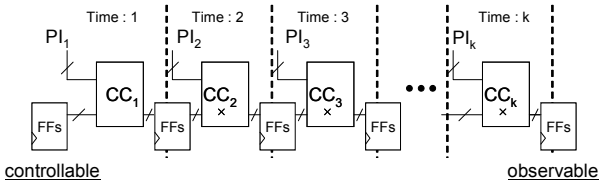

Fig. 12. A k-time expansion model based on Model B

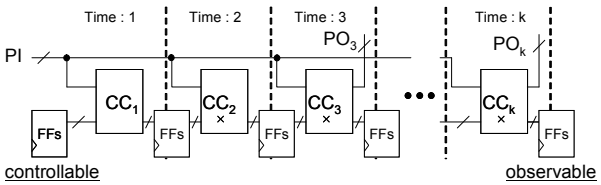

Fig. 13. A k-time expansion model based on Model C

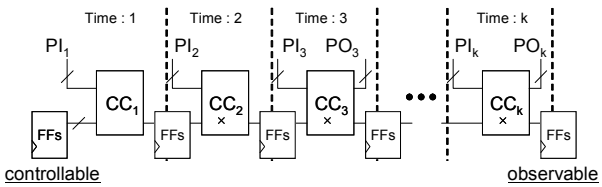

Fig. 14. A k-time expansion model based on Model D

- **Model D** the value of primary inputs is **not** fixed and the effects of transition faults **can** be detected at primary outputs.

Figure 12, 13 and 14 shows k-time expansion models based on Model B, Model C and Model D, respectively.

Model A and the condition of broad-side model are same. On Model B, the condition of primary inputs is relaxed. On Model C, the condition of primary outputs is relaxed. On Model D, the condition of primary inputs and primary outputs are relaxed. On Model A, the number of identified untestable faults is largest in four conditions. On the other hand, the number of identified untestable faults is smallest on Model D in four conditions.

IV. Experimental Results

In this section, we evaluate the relationship between the number of identified untestable faults and the excited time for transition faults on time expansion model with MCTG. MCTG is implemented on C and generates for full scan versions of ISCAS'89 benchmark circuits. Our implementation tool is called STAGY[15]. STAGY generates multi-cycle capture test sequences to multiple faults on time expansion models. In these experiments, the number of capture cycle is 6. The characteristics of benchmark circuits are shown in Table I. In Tab.I, Cir, PI, PO, FF, Fault denote the circuit name, the number of primary inputs, the number of primary outputs, the number of flip-flops and the number of target faults, respectively.

First, we evaluate the relationship of between the excited times of faults and the number of untestable faults. In these experiments, there are five kinds of excited times for transition faults (from Time 2 to Time 6). Test patterns are generated for each fault 5 times, changing the excitation time. Table II shows experimental results. In Tab.II, Cir, UT_2, UT_6, $UT_{4D,1UT}$, $UT_{1D,4UT}$ denote the circuit name, the number of untestable faults on 2-time expansion model, the number of untestable faults on 6-time expansion model, the number of faults which are identified as untestable faults under only one excitation time and are identified as detected faults under other five excitation time on 6-time expansion model, and the number of faults which are identified as detected faults under only one excitation time and are identified as untestable faults under other five excitation time on 6-time expansion model, respectively. In these results, there is no fault identified as untestable faults ($UT_{4D,1UT}$) under only one excitation time. However, there are detected faults ($UT_{1D,4UT}$) under only one excitation time and which are identified as untestable faults under other excitation time. Finally, These faults ($UT_{1D,4UT}$) are identified as untestable faults[9]. The excitation time is 6 for faults. Thus, Time 6 is the last time frame. When the test pattern is generated for the transition fault excited at the only last time frame, the fault might be identified to be not the untestable fault but detected fault.

Next, we evaluate the relationship between Model A, Model B, Model C and Model D. Target faults on each Model B, Model C and Model D are identified as untestable faults on Model A and identified as detected untestable faults on 2-time expansion model. Table III shows experimental results. In Tab.III, Cir, $UT_6 - UT_2$, Model B, Model C and Model D denote the circuit name, the number of the target faults, the number of untestable faults on Model B, the number of untestable faults on Model C, the number of untestable faults on Model D, respectively. In Tab.III, the number of untestable faults on Model B is smaller than that of Model C in each the

TABLE I
Benchmark characteristics

Cir	PI	PO	FF	Fault
s5378	35	49	179	4,245
s9234	19	22	228	6,471
s13207	31	121	669	8,477
s15850	14	87	597	10,531
s35932	35	320	1,728	35,638
s38417	28	106	1,636	27,908

TABLE II
A relationship of between excitation time and the number of untestable faults

Cir	Fault	UT_2	UT_6	$UT_{4D,1UT}$	$UT_{1D,4UT}$
s5378	4,245	233	617	0	9
s9234	6,471	519	972	0	144
s13207	8,477	334	1,220	0	251
s15850	10,531	516	1,350	0	185
s38417	35,638	4,469	4,856	0	24
s38584	27,908	368	1,418	0	117

TABLE III
A RELATIONSHIP OF BETWEEN MODEL A, MODEL B, MODEL C AND MODEL D

Cir	$UT_6 - UT_2$	UT_B	UT_C	UT_D
s5378	384	256	338	203
s9234	453	210	422	162
s13207	886	697	845	678
s15850	834	313	809	280
s35932	387	300	335	233
s38417	1,050	740	1,004	676

TABLE IV
FACTORS OF IDENTIFIED UNTESTABLE FAULTS

Cir	$UT_6 - UT_2$	PIPO	Just	Prop
s5378	384	181	79	124
s9234	453	291	55	107
s13207	886	208	204	474
s15850	834	554	62	218
s35932	387	154	57	176
s38417	1,050	374	283	393

circuits. The number of untestable faults of Model D is larger than that of Model B and Model C in s35932. On the other hand, the number of untestable faults of Model D is smaller than that of Model B and Model C in s13207. Under only the condition Model D, there are faults identified as untestable fault in s35932. On the other hand, all untestable faults under the condition Model D are identified as untestable faults under both the condition of Model B and under the condition of Model C in s13207.

Finally, we analyzed factors that untestable faults are identified under the condition of Model A. Factors are classified into three categories which consist of fixed primary inputs and undetected primary outputs, justification of states are excited faults and propagation for fault effects. Target faults are identified as untestable faults on Model A and identified as detected untestable faults on 2-time expansion model. Table IV shows experimental results. In Tab.IV, Cir, $UT_6 - UT_2$, PIPO, Just and Prop denote the circuit name, the number of target faults, the number of classified untestable faults which cannot justify and the number of classified untestable faults which cannot propagate for the fault effects, respectively. In Tab.IV, Just is the smaller than PIPO and Prop in each the circuits. In s5378, s9234 and s15850, PIPO is the largest in all the factors. On the other hand, Prop is the largest in s9234, s13207, s35932 and s38417 in all the factors. Thus, all factors are necessary to identify untestable faults in this experimental results.

V. CONCLUSION

In this paper, we evaluated the relationship between the number of untestable faults and the number of time expansions for ISCAS'89 benchmark circuits. We proposed four factors that untestable faults are identified. We classified the factors for untestable fault identification into four categories on experimental results. Experimental results show that there are detected faults under only one excitation time and which are identified as untestable faults under other excitation time and are identified as untestable faults, finally. We show the relationship of the number of untestable faults under each condition of Model A, Model B, Model C and Model D.

In our future work, an efficient method to identify untestable faults and a multi-cycle capture test generation methods for 0 detected untestable faults must be developed.

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