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Signal Probability Control for Relieving NBTI in SRAM Cells

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Abstract—Negative Bias Temperature Instability (NBTI) is one of the major reliability problems in advanced technologies. NBTI causes threshold voltage degradation in a PMOS transistor which is biased to negative voltage. In an SRAM cell, due to NBTI, threshold voltage degrades in the load PMOS transistors. The degradation has the impact on Static Noise Margin (SNM), which is a measure of read stability of a 6-T SRAM cell. In this paper, we discuss the relationship between NBTI degradation in an SRAM cell and the signal probability. This is because, it is the key parameter of NBTI degradation. Based on the observations, we propose a novel cell-flipping technique in order to make signal probability close to 50%. The long cell-flipping period leads to threshold voltage degradation as large as the original case where the cell-flipping technique is not applied. Thus, we employ the short flipping period to the cell-flipping technique without any stall of operations. In consequence of applying the cell-flipping technique to a register file, we can relieve threshold voltage degradation by 70% after the SRAM cell is used for 3 years.

Index Terms—NBTI, SRAM, signal probability, register file.

I. INTRODUCTION

Transistor performance has been advanced by scaling the process technologies. However, the technology scaling is going on for the limitation. The supply voltage does not scale at the same pace of the device size. It leads to higher current densities and thus increases temperature [13]. In addition, the decrease in the number of atoms in a transistor makes the process variations seriously [3]. In these situations, device degradation accelerates. Thus the device lifetime is getting shorter and shorter.

As a gate oxide thickness becomes thinner and thinner, the serious problem of Negative Bias Temperature Instability (NBTI) is emerging. It is accelerated by high temperature and electric field. As the gate oxide thickness reaches 4nm, NBTI becomes much more dominant than Hot Carrier Induced (HCI) degradation of NMOS transistors [2]. The range of typical stress temperature is 100 – 250°C and the oxide electric field is typically below 6MV/cm [11], [14]. NBTI degrades the threshold voltage in negatively biased PMOS transistors. On the other hand, the threshold voltage recovers in positively biased PMOS transistors. Therefore, the threshold voltage degradation depends on the signal probability, which is defined as the rate that the logic one occurs for a signal.

In an SRAM cell, NBTI causes read stability degradation [6], [8], [9]. Static Noise Margin (SNM) is one of the measures of read stability. SNM degradation has the potential to cause destructive read. Therefore, a solution for mitigating NBTI degradation is strongly required.

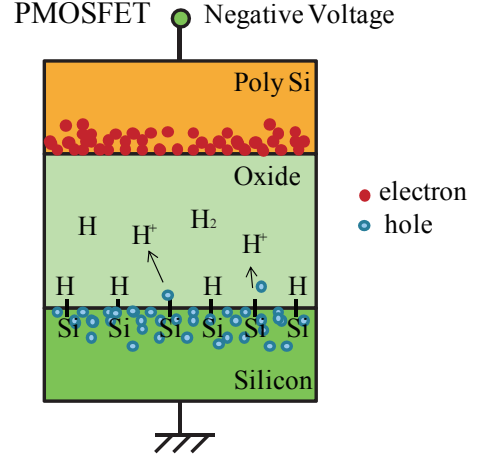


Fig. 1. NBTI on PMOSFET

In this paper, we focus on the relation of the signal probability to NBTI degradation in an SRAM cell. We analyze the trend of NBTI degradation on SRAM cells under the different signal probabilities. In order to mitigate NBTI degradation, we try to make the signal probability of the load PMOS transistors on an SRAM cell close to 50% by flipping the contents of the cell at short intervals.

The rest of the paper is organized as follows. In Section II, we explain models of NBTI and of the threshold voltage degradation and discuss the impact of NBTI on an SRAM cell. In Section III, we summarize related works and point out their problems. In Section IV, we propose a novel NBTI relieving technique. Section V presents a case study of our technique on a register file. We conclude the paper in Section VI.

II. MECHANISM AND MODEL OF NBTI ON PMOS

NBTI phenomenon can be described by reaction diffusion framework (RD) [9], [10], [11], [15], [16]. NBTI occurs due to generating interface traps at the Si-SiO₂ interface when a negative voltage is applied to a PMOS transistor (Figure 1). In the Si-SiO₂ interface, some of the atoms bond with hydrogen, leading to the formation of weak Si-H bonds. Under negative bias condition and high temperature condition, electron holes from the inversion layer can break Si-H bonds and generate the interface trap and hydrogen (H or H₂) [11], [14]. This is the reaction regime. As time goes on, released hydrogen diffuses away from interface, the process limits the trap formation. This is the diffusion regime. Because

the interface trap is generated in this way, the threshold voltage increases.

On the other hands, NBTI degradation can be recovered by annealing if the NBTI stress voltage is removed. The broken $S_i - H$ bonds recombine and hence the threshold voltage recovers [4].

A. Dynamic and Long Term NBTI model

The stress and recovery phenomenon of NBTI is modeled in [15] (dynamic NBTI model) as follows:

Stress model:

$$\Delta V_{th}(t) = (K_v(t - t_0)^{1/2} + {}^{2n}\sqrt{\Delta V_{th}(t_0)})^{2n} \quad (1)$$

Recovery model:

$$\Delta V_{th}(t) = \Delta V_{th}(t_1) \left(1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(t - t_1)}}{2t_{ox} + \sqrt{Ct}} \right) \quad (2)$$

K_v and C are variables which depend on a temperature. ξ_1 and ξ_2 are coefficient. t_e is the variable which depends on recovery times. And n is the time exponent. If diffusing species is H , n is $1/4$ and if diffusing species is H_2 , n is $1/6$ [8]. In the reaction of breaking $S_i - H$ bonds, H_2 tends to be dominant [8], [14]. Therefore, we use the time exponent value of $1/6$. This model can predict the ΔV_{th} shift after a device is used for t time.

However, the dynamic NBTI model is not suitable for predicting a long term degradation. This model spends $m = t/T_{clk}$ cycles on prediction of the ΔV_{th} , where T_{clk} is stress and recovery cycle. In high performance circuits operating at GHz, T_{clk} is very small. As a result, m becomes huge cycles in long term. It increases the calculation times drastically. Therefore, the long term threshold voltage degradation is modeled in [2] (long term model) as follows:

Long term model:

$$\Delta V_{th} = \left(\frac{\sqrt{K_v^2 \alpha T_{clk}}}{1 - \beta_t^{1/2n}} \right)^{2n} \quad (3)$$

$$\beta_t = 1 - \frac{2\xi_1 t_e + \sqrt{\xi_2 C(1 - \alpha)T_{clk}}}{2t_{ox} + \sqrt{Ct}} \quad (4)$$

This model is derived from (1) and (2). α is stress probability, which is the rate that the logic zero occurs for a signal. Therefore, signal probability is described as $1 - \alpha$. In this paper, we use these models to predict threshold voltage degradation.

B. Impact of NBTI on an SRAM Cell

Figure 2 describes an 6-T SRAM cell, which consists of two CMOS inverters. There are two load PMOS transistors (P1 and P2). Due to NBTI degradation, the threshold voltage degrades in the load PMOS transistors[6], [8], [9]. As a result the read stability degrades in an SRAM cell. Static Noise Margin (SNM) is a popular measure for evaluating read stability[12].

When a 6-T SRAM cell designed on 70nm technology is used for 3 years, SNM degrades by about 10% [9]. Due to SNM degradation, a read access destructs the content of the SRAM cell. Thus, a technique for reducing threshold voltage degradation is required. When an SRAM cell holds value 0 (1), P1 is ON (OFF) and P2 is OFF (ON). Therefore, in order to mitigate NBTI degradation, the signal probability of both load PMOS transistors should be close to 50%.

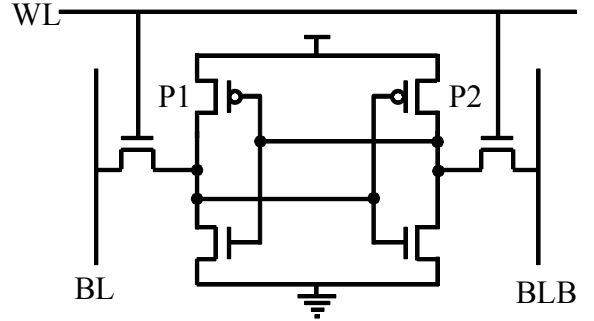


Fig. 2. 6-T SRAM cell

III. CELL-FLIPPING TECHNIQUE FOR SRAM

A. Related Works

In order to mitigate the threshold voltage degradation, the signal probability should be close to 50%. Kumar et al. propose a cell-flipping technique and apply it to caches[9]. The technique has two modes. One is *Normal mode*, where the original data are written to caches and the other is *Flip mode*, where the data are once flipped then written. The mode changes according to the flipping signal, which switches every day. In this technique, every time the mode switches, all values in caches are flipped and thus the cache stalls. The periodically cell-flipping technique may be expensive in terms of delay because an XOR gate must be introduced in the read/write data paths.

Penelope[1] is an NBTI-aware processor, which also tries to make the signal probability close to 50% in SRAM arrays. The idea is to write the special value while the entry of the SRAM array is in the idle state. Writing a special value does not have path delay penalty because it does not require XOR gates on the data path. In the case study in a register file, they sample the value of register entry periodically. The sampled value is flipped and is written to the entry when the register entry is in the idle state. The write operation is controlled in order to hold the inverted sample value for 50% for the overall time. Therefore, the signal probability is close to 50%. However, this technique increases the number of write operations. Register files are one of the hottest components in processor[13]. Increasing the number of write operations increases the power consumption and thus also does operating temperature, which NBTI depend on exponentially.

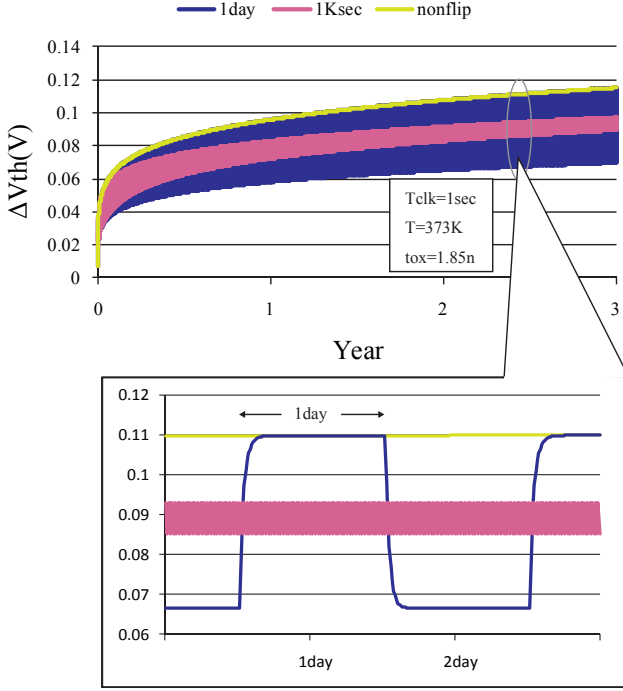


Fig. 3. Effect of mode switching cycle on ΔV_{th}

B. Mode Switching Cycle Effect

We call this switching interval *mode switching cycle*. We evaluate the effect of the mode switching cycle on the threshold voltage degradation. The threshold voltage degradation is evaluated by dynamic NBTI model explained as expressions (1) and (2). We assume that the stress and recovery cycle (T_{clk}) is 1sec. The period of the device operation is 3 years. It is assumed that the stress probability α is 0.9 and 0.1 in *Normal mode* and *Flip mode*, respectively. The evaluation results are shown in Figure 3. We select one day (denoted as 1day in Figure 3) and 1K seconds (denoted as 1Ksec in the figure 3) for the mode switching cycle. nonflip in Figure 3 indicates the original case where the cell-flipping technique is not applied. The threshold voltage degradation in 1day is as large as that in nonflip. In contrast, the threshold voltage degradation in 1Ksec is approximately 25% smaller than that in nonflip. That is, shorter mode switching cycle is desirable.

In high performance circuits operating at over GHz, we expect that T_{clk} is smaller than 1 second. Unfortunately, in the dynamic NBTI model, small T_{clk} drastically increases calculation times for predicting threshold voltage degradation. In the evaluation, we predict the threshold voltage degradation using a small T_{clk} where the device is used for a short term. As a result, the threshold voltage degradation is smaller than the practical case for a short term. We expect that the threshold voltage degradation can be mitigated at small T_{clk} when we continue to use the device for long term. Therefore, even though we use the small T_{clk} of 1 second in this evaluation, we can get the trend of threshold voltage degradation.

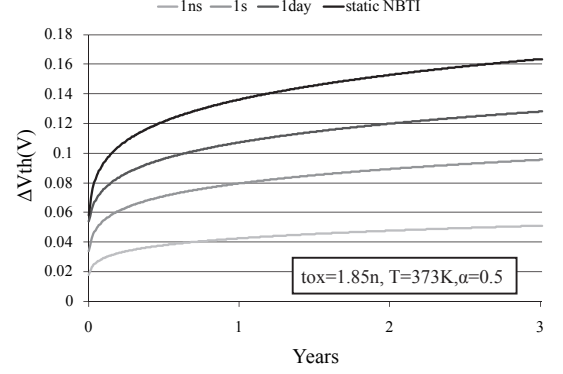


Fig. 4. Effect of stress and recovery cycle on ΔV_{th}

In addition, NBTI degradation depends on a T_{clk} . Figure 4 explains that the threshold voltage degradation depends on the T_{clk} . We predict the threshold voltage degradation by using the long term model. We assume that the stress probability (α) is 0.5. We vary T_{clk} between 1n second (denoted as 1ns in Figure 4), 1 second (denoted as 1s in the figure) and 1day (denoted as 1day). static NBTI in Figure 4 denotes the case where the device is constantly stressed for 3 years. In other words, it is the worst case for the threshold voltage degradation. As T_{clk} is larger, the threshold voltage degradation gets closer to the worst case. On the other hand, as T_{clk} is smaller, the threshold voltage degradation is relieved. However, it has a minimum value limited by the condition described below. Even when $T_{recovery}$ is smaller than a boundary time (t'), the threshold voltage degradation can not be smaller than the minimum value. $T_{recovery}$ and t' are defined as $T_{clk}(1 - \alpha)$ and $t' = t_{ox}/d$ respectively. An example of t' is 3.85ms for t_{ox} of 1.85nm. In high performance circuits operating at over GHz, it is expected that $T_{recovery}$ is smaller than t' . However, some bits of SRAM array may not flip when the write data are biased. For example, when positive data of half words are written to an entry of memory array continuously, the upper bits of an SRAM array is held on zero. From these observations above, we found, a mode switching cycle should be shorter than t' .

IV. MODE SWITCHING CYCLE EFFECT AWARE CELL-FLIPPING CIRCUIT

In order to make the mode switching cycle short, we improve the cell-flipping technique as shown in Figure 5. It is an SRAM array with cell-flipping circuits. We coin this cell-flipping technique Short Term Cell-flipping (STCF) technique. It can switch the mode without any performance loss. We explain the reason why. The STCF SRAM array consist of SRAM array, Flip signal, Flip bits and two XOR circuits. Flip signal indicate the mode. In *Normal mode*, Flip signal is 0. In *Flip mode*, Flip signal is 1. In order to control Flip signal, an additional counter is required. When the counter value is equal to the mode switching cycle, Flip signal is switched. Flip bit is associated with each entry and is used to indicate

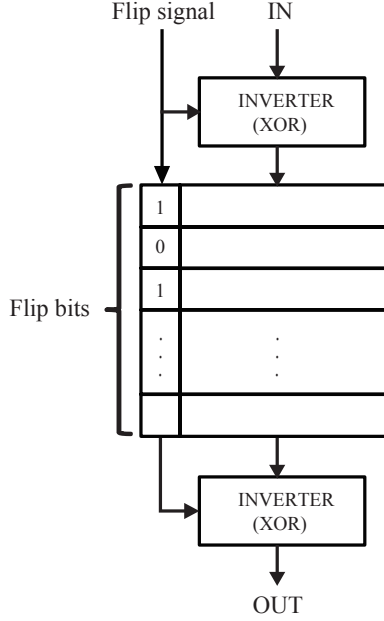


Fig. 5. STCF SRAM array

whether data in the entry is flipped or not. XORs are used to be flipped read/write data.

It operates as follows. When a Flip signal is 1 (*Flip mode*), a write data are once flipped then written to the entry and Flip signal is written to the Flip bit of the entry. When a read access occurs, if reading Flip bit is 1, the read data are flipped by XOR. Therefore, it can avoid the stall just behind the mode switching.

V. CASE STUDY ON REGISTER FILE

STCF can be applied to caches, register files and scheduling tables in a processor, because they consist of SRAM arrays. In this section, we show a case study on a register file, which is known as one of the hottest components in a processor[13]. We use Toshiba's Media Embedded Processor (MeP) [5], which has 16 general purpose registers. Reg 13 is used as tiny data area pointer. Reg 14 is used as global pointer. Reg 15 is used as stack pointer.

A. Mode Switching Cycle Detection

If a write access doesn't occur in each mode cycle, the register entry data have not flipped. Therefore, the signal probability may not be close to 50%. In order to decide the suitable mode switching cycle, we evaluate the Mean Cycle to Writing (MCTW) of each register entry. It is shown in Figure 6. We perform the RTL simulation and extract data of each register entry and write enable signal every cycle. In some benchmark programs, the write access hardly occurs on some registers. In order to make signal probability close to 50%, the mode switching cycle should be much longer than MCTW. However, MCTW of some register is much larger. Therefore, we can't decide on the suitable mode switching cycle.

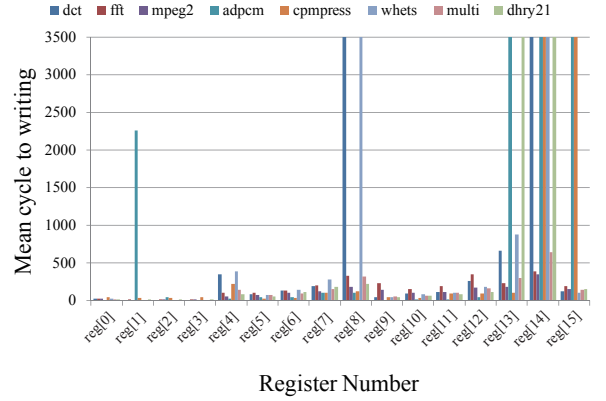


Fig. 6. Mean Cycle to Writing

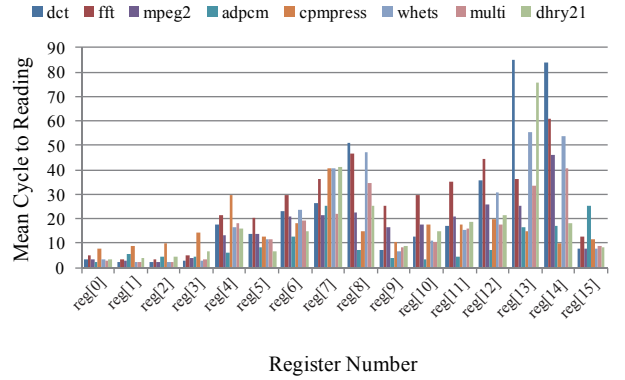


Fig. 7. Mean Cycle to Reading

Given this factor, we focus on the Mean Cycle to Reading (MCTR). It is shown in Figure 7. MCTR of each register is less than 90 cycle on average in all benchmark programs. Therefore, we improve STCF technique as follows. When the register data are read, it is flipped and written back to the entry. We expect that the improved technique can flip by several hundred cycles after switching the mode. However, if all read data are written back, write access is increased. In order to reduce the write back operations, we start to write back after the most register were written. The improved STCF technique is called Short Term Cell-flipping on Read and Write back(STCFRW).

Figure 8 describes the SRAM array of STCFRW. When the mode switches to *Flip mode*, the write data are once flipped then written by XOR. The read data are latched and are flipped in the next pipeline stage. XOR is placed in the next pipeline stage to avoid the increase in critical path delay. It is mentioned in the next section. If $(Flip\ signal \oplus Flip\ bit) \cap WBEN \cap \overline{WEN}$ is valid, the read data are selected by MUX and write back to the entry. $WBEN$ indicates write back enable signal which controls the write back operation. In order to control $WBEN$, an additional counter is required. It counts

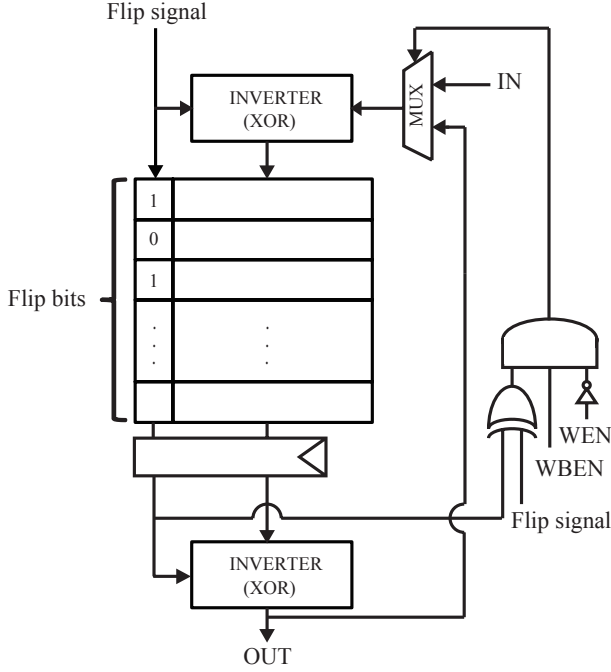


Fig. 8. STCFRW SRAM array

the clock cycle to write back starting cycles and when the clock cycle is equal to the cycles, $WBEN$ is enabled. This write back starting cycles is fixed at cycles expecting that the write access occurs in most register entries. $WBEN$ is write enable signal of write data. When $WBEN$ is enabled, the read data are abandoned. It can not flip the content of the register entry. However, we expect that the conflict is rare and that the conflict penalty is little, because next read occurs shortly. We set that the mode switching cycle is 10K cycles and write back starting cycle is 1K cycles, because write access occurs in most register entry every 1K cycles.

STCFRW does not guarantee that all register entries are flipped every mode cycle. If any read or write access does not occur in a register, its content is not flipped. It should be noted that the register is not efficiently used. Hence, we expect the compiler to utilize the register more frequently.

B. Area and Performance Overhead

To apply STCF to a register file, the additional circuits require some area overheads. There are three inverters consisting of 32bits XOR, one is connected to the write port, the others are connected to the read ports. Flip bit is required for each register file entry. And the counter for controlling Flip signal is required. In addition, when STCFRW is applied to the register file, it requires some additional circuits, which are a XOR, a 3 inputs AND, a 32bit register and a MUX. We assume that the register file consists of a single bit line SRAM and calculate the number of transistor of each additional circuits. It is shown in Table I.

These additional circuits increase delay. In the write port, the XOR and write back path increase the path delay. However,

TABLE I
THE NUMBER OF TRANSISTOR OF ADDITIONAL CIRCUIT IN STCFRW

circuit	composition	number of transistor
register file	32bit \times 16 entries	2,560
XOR(inverter)	32bit \times 3	1,536
Flip bit	1bit \times 16entries	80
counter	14bit	784
MUX	1	14
XOR	1	16
AND3	1	8
register (buffer)	33bit	165

we expect that the extra delay may be hidden by the delay of the address decoder in register file. On the other hand, in the read ports, the extra delay can't be hidden by any other delays. In order to avoid the performance degradation, the XOR for cell-flipping is placed in the succeeding pipeline stage. Because the register file is one of the timing critical components in the processor. We expect that the path in the succeeding pipeline stage is shorter than the path in the register file. Therefore we can hide the extra delay by timing margin in the succeeding pipeline stage.

C. Effect on Signal Probability and Threshold Voltage

Next, we show the effect of STCF and STCFRW on the stress probability and on the threshold voltage. We evaluate the stress probability by extracting the register entry data every cycle from RTL simulation. We calculate the threshold voltage by using the long term model of NBTI degradation which is shown in (3) and (4). The long term model's parameters are assumed by referring to [15]. In addition, the technology dependent parameters such as t_{ox} , initial V_{th} and V_{dd} are assumed by referring to 65nm Predictive Technology Model (PTM) [7].

Figure 9 presents the effect of the SRAM cell-flipping on stress probability. (a) shows the original, (b) shows STCF and (c) shows STCFRW. The dct result is the typical case in all benchmark programs. In (a), the stress probability is biased to high. In (b), the stress probability of the register which is hardly written can't be made close to 50%. In (c), the stress probability of all register is very close to 50%. In the other benchmark programs, those stress probabilities is very close to 50%. In the adpcm, stress probability is most distant from 50%. It is 58%. Therefore, the effect of flipping does not depend on any application characteristics.

Figure 10 presents the threshold voltage degradation. We assume that the register file is used with these stress probabilities for 3 years. (a) shows the original and (b) shows STCFRW. In (a), the worst case threshold voltage is degraded by about 160mV. In (b), the threshold voltage degradation is relieved to about 50mV. The threshold voltage degradation can be reduced by 70% in comparison with the original.

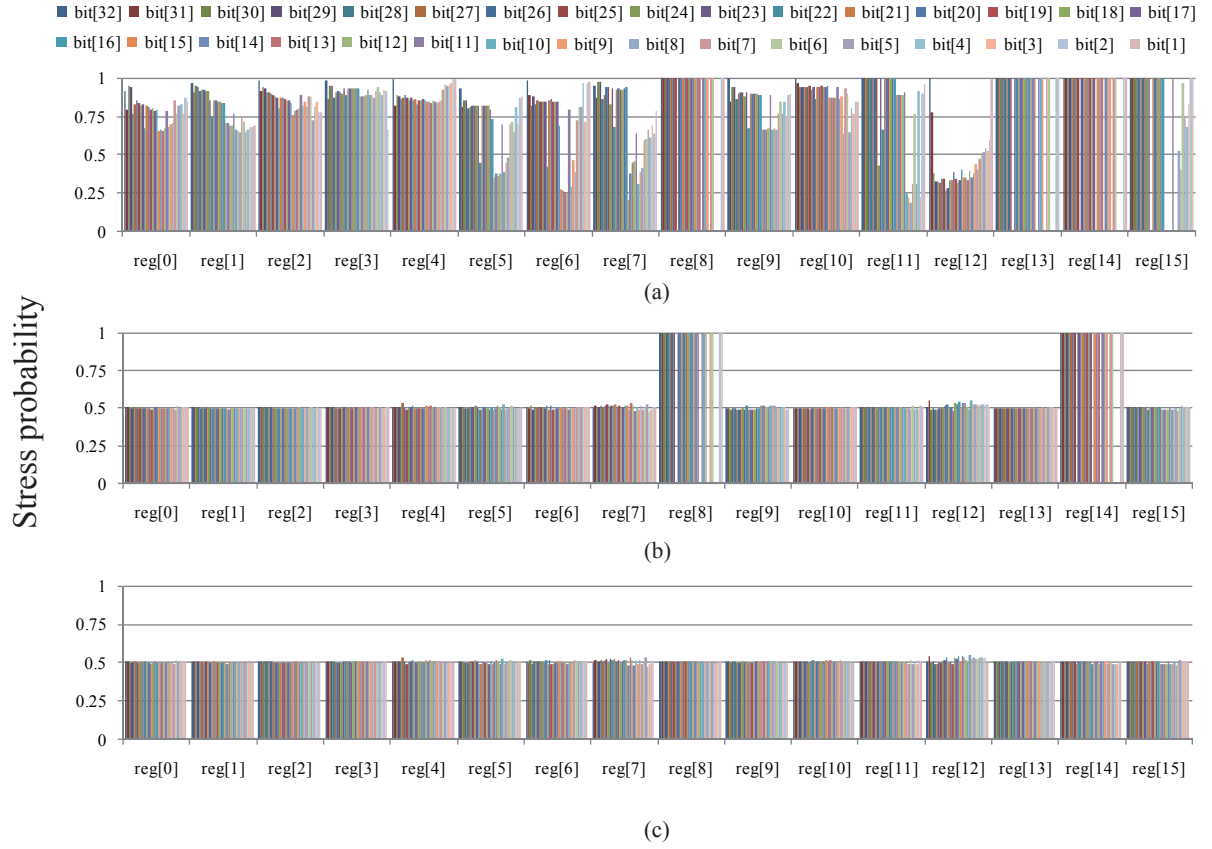


Fig. 9. Stress probability:(a) the original, (b) STCF and (c) STCFRW

VI. CONCLUSIONS

The signal probability is a key parameter of NBTI. In SRAM cells, NBTI degradation can be relieved by making signal probability close to 50%. In this paper, we propose a novel technique of cell-flipping for NBTI mitigation. Our experimental results show that when the mode switching cycle is much long, the threshold voltage degradations is as large as the original. Hence, the existing cell-flipping technique, whose mode switching cycle is too long, can't relieve NBTI degradation effectively. Our novel technique of cell-flipping employs short mode switching cycle and avoids the performance penalty. Applying the cell-flipping technique to register file, we can relieve threshold voltage degradation by 70%, which is caused by NBTI degradation.

One of the future studies regarding SRAM lifetime is considering Positive Bias Temperature Instability (PBTI). Recently, a high-k gate oxide is applied to decrease leakage power consumption. The high dielectric constant causes PBTI which affects NMOS transistors [6]. When PBTI and NBTI affect a cell in combination, its SNM is seriously damaged. We expect that our cell-flipping technique can also relieve PBTI degradation because PBTI effect is similar to NBTI and

because its stress condition is opposite to NBTI.

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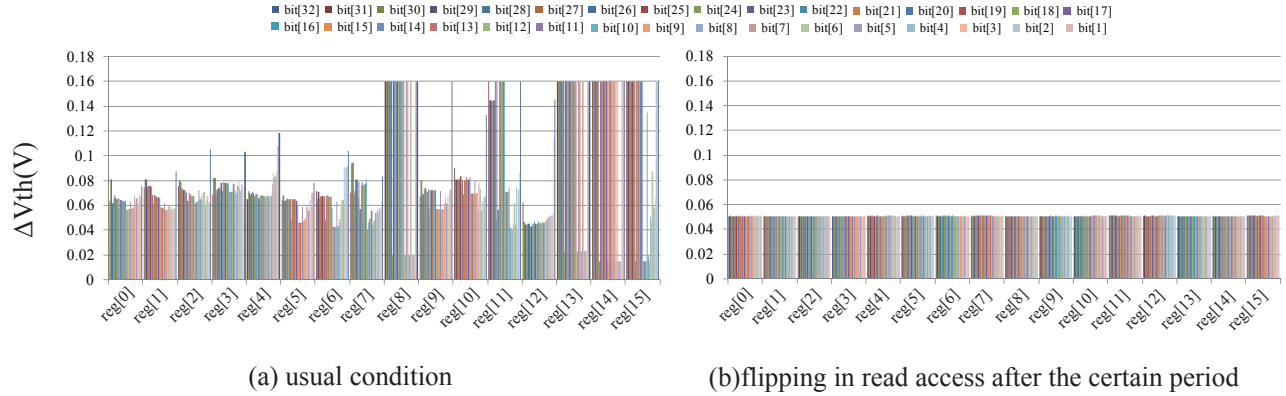


Fig. 10. Effect of STCFRW on ΔV_{th}

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