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***Abstract*—Since the clock power consumption in today's processors is considerably large, reducing the clock power consumption contributes to the reduction of the total power consumption in the processors. Recently, a gated flip-flop is proposed for reducing the clock power consumption of flip-flop circuits. The gated flip-flop employs a clock-gating circuit which cuts off an internal clock signal if the data stored in the flip-flop does not need to be updated. This reduces the clocking power consumption. However, the power dissipated in the clock-gating circuit is still large. For reducing the power dissipated in the clock-gating circuit, this paper proposes a technique for unifying the multiple clock-gating circuits, which reduces the overhead of the clock-gating circuit. Experimental results obtained using an RTL model of a commercial embedded processor demonstrate that our technique reduces the power consumption of register circuits in the processor by 44% on an average and 53% at the best case compared to the register circuits composed of the conventional gated flip-flops.**

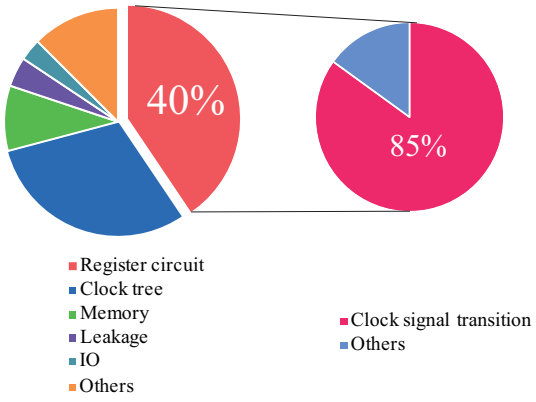

Fig. 1. Power Breakdown of Microprocessor

I. Introduction

Ever increasing performance of microprocessors results in an explosion of the power consumption in the microprocessors. In a typical microprocessor, the power dissipated in register circuits is dominant [1]. Figure 1 shows a break down of the power contributions in a commercial RISC-type microprocessor which is synthesized by ourselves using a commercial 65nm process technology. As can be seen from the Figure, the power consumption of register circuits is around 40% of the total power consumption of the microprocessor. This demonstrates that the reduction of the power dissipated in the register circuits largely contributes to the reduction of the total power consumption of the microprocessor. Another important observation is that more than 80% of the power consumption in the register circuits is dissipated due to clock-signal transitions in flip-flop circuits. This is mainly because a probability of signal transitions in a clock port of a flip-flop is much higher than that in a data port of the flip-flop. Therefore, reducing the clocking power in the flip-flops contributes to the power reduction of microprocessors.

Clock-gating is widely used for reducing the power dissipated in the clock ports of the register circuits [2]. This reduces the probability of the clock-signal transitions in the flip-flop circuits. For example, SYNOPSYS Power_Compiler exploits an enable signal connected to a register circuit for cutting off the clock signal to the flip-flops [3]. The register here is defined as a set of flip-flops which share a common enable signal. If the enable signal is false, the clock signal is gated and any flip-flop in the register does not consume the clocking power. However, there still exists a room for reducing the clocking power, since this approach cannot separately stop the clock supply to a subset of the flip-flops in the register circuit which is controlled by a common enable signal. For making finer grained clock gating possible, a technique of gated flip-flop is proposed [4]. This technique makes it possible to perform bitwise clock gating. The gated flip-flop employs an internal clock-gating circuit which stops the clock supply to the flip-flop if an input value of the flip-flop is equal to a value stored in the flip-flop. The main drawback of the gated flip-flop is its large area and power overheads in the internal clock-gating circuit. This paper proposes a technique for unifying the multiple clock-gating circuits, which reduces the power and area overheads of the clock-gating circuit.

The rest of the paper is organized in the following way. Section 2 summarizes related work. Our idea for unifying multiple gated flip-flops is presented in Section 3. In Section 4, experiments and results using a commercial microprocessor are shown. Section 5 concludes this paper.

II. Related Work

A. Fine-Grained Clock Gating

Recent microprocessors used in many computer systems have a 32-bit or 64-bit data path. Although those processors normally performs 32-bit or 64-bit operations, narrow-width operations are still frequent. Brooks et al. [5] show

that roughly 50% of the integer instructions in SPECint95 benchmark programs require less than or equal to a 16-bit precision, even though the underlying processor has a 64-bit data path. Since conventional processors always assign the full-bit width of a register entry even for the narrow-width operand, the upper bits of the register entry are useless and dissipate wasteful clocking power in corresponding flip-flops. A technique presented in [5] detects these useless upper bits dynamically and cuts off the clock supply to these bits for reducing the wasteful clocking power consumption. The narrow-width operand is exploited in a concept called partially guarded computation [6]. The idea is to divide a functional unit into two parts, MSP (Most Significant Part) and LSP (Least Significant Part), and to perform only the LSP computation if the range of output data can be covered by LSP only. MSP computation is disabled dynamically by using clock-gating for saving the power consumption of the MSP. Similar idea is applied to register files [7]. The idea is to partition a register file into two sb-word banks. If an MSP of each register file entry is used for sign extension only, the clock supply to the MSP is gated for saving the power consumption. The techniques presented above drastically reduce the power dissipated for clocking as well as the power dissipated in functional units. However, the problem is that they involve a considerable overhead for detecting conditions of clock gating. For example, all of above presented techniques need to detect all-zeros or all-ones in an input of the MSP, which involves considerable delay, area and power overheads. Another problem is that those techniques can be applied to registers on a data path only. Unlike those techniques, our technique aims at both reducing the overhead to dynamically detect the conditions for clock gating and reducing the switching activities of clock ports in every registers including pipeline registers, a register file, status register and so on.

B. Low Power Flip-Flops

Flip-flops are the building blocks of fast and small memories such as register files. A typical master-slave flip-flop consists of two latches, a master latch and a slave latch. When the clock signal is high, the master latch turns on and the slave latch turns off. In this phase, the mater latch samples whatever inputs it receives and outputs them. The slave latch, however, does not sample its inputs but merely outputs whatever it has most recently stored. On the falling edge of the clock, the master turns off and the slave turns on. Thus the master keeps its most recent input and stops sampling. The slave samples the new inputs from the master and output it. Since the clock transition causes internal switching activity in the master-slave flip-flop as explained above, non-negligible power is dissipated in the flip-flop even if no state change occurs. Our technique proposed in this paper reduces the clocking power consumption in the master-slave flip-flop.

In the past, several low power designs for the master-slave flip-flop have been proposed, such as data look-ahead flip-flop [8], clock-on-demand flip-flop [9], and gated flip-flop [4]. The common idea among the above techniques is to insert

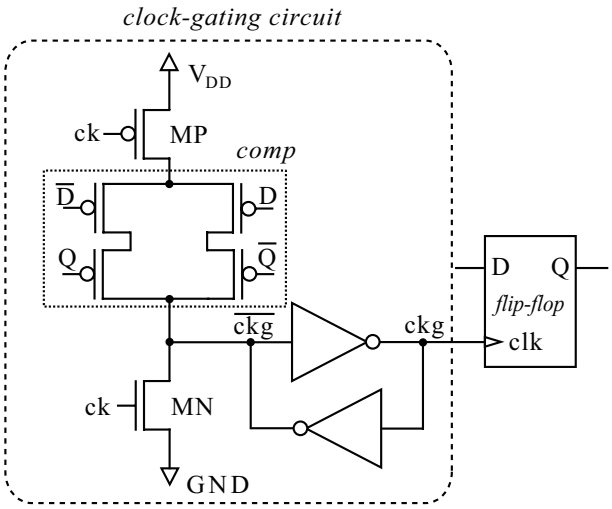

Fig. 2. Gated Flip-Flop [4]

conditional circuitry into their clock path to cut off the clock signal in a case that the inputs will produce no change in the outputs. Strollo et al. [4] have proposed two versions of the gated flip-flop. In the double-gated flip-flop, each of the master and slave latches has its own clock-gating circuit. The circuit consists of a comparator that checks whether the current input value and the value stored in the flip-flop are different from each other and a logic which cuts off the clock signal based on the output of the comparator. In the sequential-gated flip-flop, the master and the slave share the same clock-gating circuit instead of having their own individual circuit as in the double-gated flip-flop. This drastically reduce the clocking power consumption. However, one of the most critical issues in the gated flip-flops is its power overhead in the clock-gating circuit. As the frequency of state transitions in the flip-flop increases, the power overhead by the clock-gating circuit increases. Therefore, if the value stored in the flip-flop needs to be updated frequently, the gated flip-flop consumes more power than a normal flip-flop. Another serious issue is its area overhead. This area overhead leads to an increase of a chip area required for a processor and may consume more power. Our technique aims at reducing these overheads by sharing the clock-gating circuit among multiple flip-flops.

C. Preliminal Analysis

An example of the conventional gated flip-flop circuit is shown in Figure 2. The gated flip-flop consists of a normal flip-flop and a clock-gating circuit for cutting off the clock supply to the flip-flop part if values of input D and output Q of the flip-flop are the same from each other. The technique reduces the clocking power if the value stored in the flip-flop does not need to be updated. However, if the state transition probability of the flip-flop is more than a specific value, the gated flip-flop dissipates more power than a normal master-slave flip-flop. We refer to this specific value as a break-even probability. It is very important to apply the gated flip-flop only

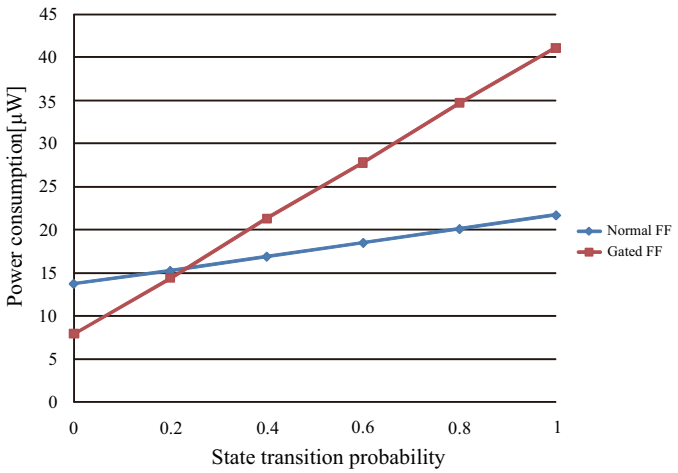

Fig. 3. Power Consumption of Gated Flip-Flop

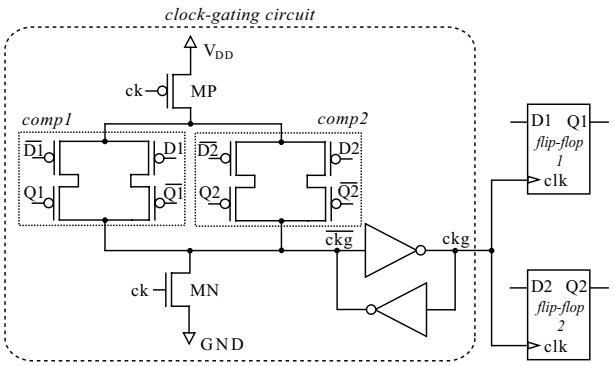

Fig. 4. Schematic of 2-bit Unified Gated Flip-Flops

if the state transition probability is less than the break-even probability for reducing the power consumption of register circuits.

Figure 3 shows the power consumptions of a normal master-slave flip-flop and a gated flip-flop for different state transition probabilities in flip-flops. Horizontal axis shows state transition probability of the flip-flops. Vertical axis shows the power consumption of the flip-flops. The state transition probability represents the average number of state translations in a flip-flop per a clock cycle. Since the state transition in a flip-flop occurs at most once in a clock cycle, the state transition probability is no more than 1. As can be seen from the Figure, the gated flip-flop consumes less power than that of the normal flip-flop if the state transition probability is lower than 23%. This is because the power consumption in the clock gating circuit is less than the reduction of the clocking power in the flip-flop part of the gated flip-flop if the state transition probability is lower than 23%.

III. Unified Gated Flip-Flop

This section shows our idea of unifying multiple gated flip-flops for reducing the clocking power consumption of register circuits.

A. Unification of Multiple Clock-Gating Circuits

One possible approach to reducing the power overhead in the clock-gating circuit is to reduce the load capacitance of a clock input port. Our idea is to share a single clock-gating circuit among multiple flip-flops. An example of a 2-bit unified gated flip-flop is shown in Figure 4. For reducing the load capacitance of the clock input port per bit, multiple flip-flops share a *ck* pin. The conditions for cutting off the clock signal are computed by a circuit which is composed of multiple $comp_i$ circuits connected in parallel. The number of *comp* circuits connected in parallel is equal to the number of flip-flops unified together. An internal clock signal *ckg* connected to flip-flops is activated if a value of D_i is different from a value of Q_i. Therefore, if a value of D port even in a single flip-flop is equal to a value of Q port in the same flip-flop, the clock is provided to all flip-flops. This implies that the switching probability in *ckg* port increases as the number of flip-flops unified increases. This may increase the clocking power consumption even though the load capacitance of *ck* port per bit is reduced by unifying multiple flip-flops.

B. Layout and Area Overhead

This section shows a relation between the number of unified flip-flops and a layout area of the unified gated flip-flop. The clock-gating circuit is designed by our selves from a scratch using a commercial $0.18\mu m$ process technology. The clock-gating circuit is concatenated with normal master-slave flip-flops selected from an existing standard cell library.

Figure 5 shows layout areas required for the unified gated flip-flops. Horizontal axis shows the number of flip-flops unified together. Vertical axis shows the ratio of the layout area required for a n-bit unified gated flip-flop to that required for the n-bit normal flip-flops. For example, the layout area of a 1-bit gated flip-flop is double of the area of the 1-bit normal flip-flop. Our unified gated flip-flop shares the clock-gating circuit among several flip-flops. Therefore, as the number of flip-flops unified together increases, the area of the unified gated flip-flop per bit decreases. For example, area overhead

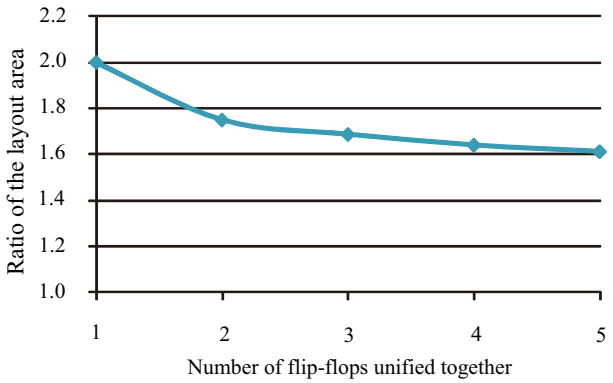

Fig. 5. Layout Area

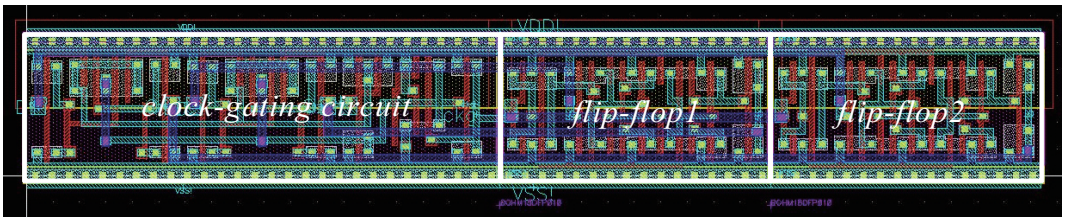

Fig. 6. Layout of 2-bit Gated Flip-Flop

per bit involved in a 4-bit unified gated flip-flop is 38% smaller than that of the conventional 1-bit gated flip-flop.

Figure 6 shows a layout image of a 2-bit unified gated flip-flop. The left most block and the right two blocks show the clock-gating circuit and normal flip-flops, respectively.

C. Power and Delay Results

This section shows power and delay results obtained through SPICE simulation using SYNOPSYS HSPICE. A SPICE netlist used in the simulation is extracted from the physical layout designed by ourselves. Supply voltage used is 1.8V. A target process technology in this experiment is a commercial $0.18\mu m$ CMOS process technology.

1) Power Consumption: Normal flip-flop, conventional, 2-bit unified, 3-bit unified, 4-bit unified and 5-bit unified gated flip-flops are evaluated for different state transition probabilities. In the evaluations for the unified gated flip-flops, state transition probabilities of all unified flip-flops are set to be the same from each other, since all unified flip-flops share a common clock signal and a common data input. For considering the power dissipated in input ports, inverter circuits are connected to every D_i and ck ports. All power consumption results include the power consumption of these inverter circuits as well.

Power consumption results are shown in Figure 7. Horizontal axis represents the state transition probability of the flip-flop. Vertical axis represents the power consumption. As can be seen from the Figure, there is a specific state transition probability where the power consumption of the unified gated flip-flop gets over the power consumption of the normal flip-flop. We refer to this specific probability as a break-even probability. The break-even probabilities for 2-bit, 3-bit, 4-bit and 5-bit unified gated flip-flops are 48%, 57%, 62%, and 63%, respectively.

2) Setup, hold and Delay: This section shows results of setup time, hold time and delay of our unified gated flip-flops. All results are obtained through SPICE simulation using SYNOPSYS HSPICE.

TableI shows setup time, hold time and delay of five different types of flip-flops in picosecond. Normal FF, CONV GFF, 2-BIT UGFF, 3-BIT UGFF, 4-BIT UGFF, and 5-BIT UGFF represent normal master-slave flip-flop, conventional gated flip-flop [4], 2-bit unified gated flip-flop, 3-bit unified gated flip-flop, 4-bit unified gated flip-flop, and 5-bit unified gated flip-flop, respectively. The delay represents waiting time

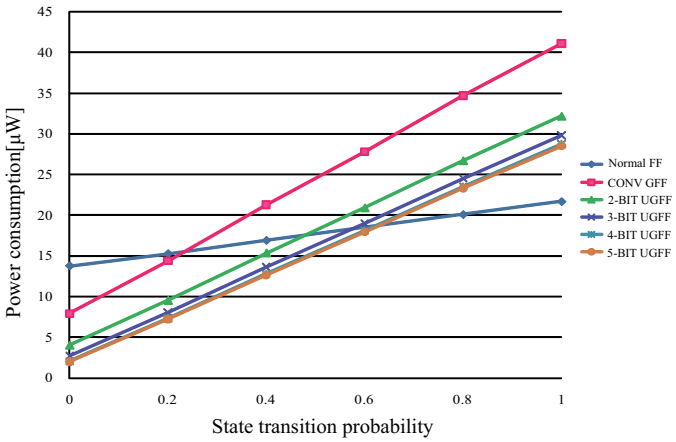

Fig. 7. Power Consumption of Unified Gated Flip-Flops

for a Q output signal available from a rising edge of a clock signal. As can be seen from the Table, a width of latch window of our unified gated flip-flops are wider than that of the normal flip-flop except for 3-bit unified gated flip-flop. Note that the latch window represents the time period during which an input data can be latched. The width of the latch window can be calculated by summing the setup time and hold time. The delay of gated flip-flops are much larger than that of the normal flip-flop. This makes it difficult to apply our unified gated flip-flops to a critical path of the target circuit. This is the main disadvantage of our unified gated flip-flop. However, an increase of the delay in the 4-bit unified gated flip-flop over the normal flip-flop is about 35 picoseconds, which is less than 1% of the critical-path delay in a processor whose clock frequency is 250MHz. This is not very significant. One of our future plans is to prove that our unified flip-flop can be applied

TABLE I
TIMING PARAMETERS

	setup [ps]		hold [ps]		delay [ps]	
	rise	fall	rise	fall	rise	fall
Nomal FF	9.74	9.74	−2.41	−2.42	25.7	24.7
CONV GFF	3.78	4.88	9.75	9.75	41.9	39.9
2-BIT UGFF	−9.74	−9.74	17.06	18.29	49.4	46.7
3-BIT UGFF	−9.74	−9.74	29.27	29.28	54.8	52.3
4-BIT UGFF	−24.38	−24.39	29.27	34.16	60.2	57.7
5-BIT UGFF	−29.27	−29.27	34.16	37.82	65.5	62.3

in actual processors with negligible performance degradation of the processors.

IV. Case Study

This section shows the power consumption results of registers in a commercial microprocessor.

A. Experimental Setup

We target a MIPS-based RISC processor, Media embedded Processor (MeP) [10], which is developed by Toshiba. It has 5 pipeline stages and 16 general purpose registers. We apply clock gating to the processor in advance. First, we run benchmark programs presented in Table II on an RTL model of the processor to obtain the state transition probabilities of every bits in registers whose bit-width is equal to or more than four bits. Verilog-XL of Cadence is used for the simulation. Next, we calculate the power consumption of the register circuits based on the state transition probabilities obtained through the Verilog RTL simulation and the power consumption of the unified gated flip-flop obtained through SPICE simulation.

TABLE II
Benchmark program

Benchmark	Descriptions
dct	Discrete Cosine Transform
fft	Fast Fourier Transform
JPEG	JPEG encorder
MPEG2	MPEG2 encorder
adpcm	ADPCM decoder
compress	file compression
dhry21	Dhrystone: integer arithmetic
whets	Whetstone: floating-point arithmetic

Normal flip-flop, conventional gated flip-flop, 2-bit unified gated flip-flop, 3-bit unified gated flip-flop, and 4-bit unified gated flip-flops are evaluated. We apply the unified gated flip-flop from an MSB (Most Significant Bit) of a register. If there is a fraction in an LSB (Least Significant Bit) part of the register, we apply a narrower unified gated flip-flop to the fraction part. For example, suppose we apply the 4-bit unified gated flip-flop to a 10-bit register. In this case, two 4-bit unified flip-flops are applied to the 8-bit MSB part of the register and one 2-bit unified flip-flop is applied to the 2-bit LSB part of the register. We apply different types of gated flip-flops to 139 registers in the MeP processor and analyze the power consumption of the registers.

B. Experimental Result

Figure 8 shows average supplied clock signal probabilities. The supplied clock signal probability represents the number of rising clock transitions propagated to an internal flip-flop per a clock cycle. The probabilities of the flip-flops are averaged over the registers in the processor. Even if the state of only one flip-flop of the unified gated flip-flops needs to

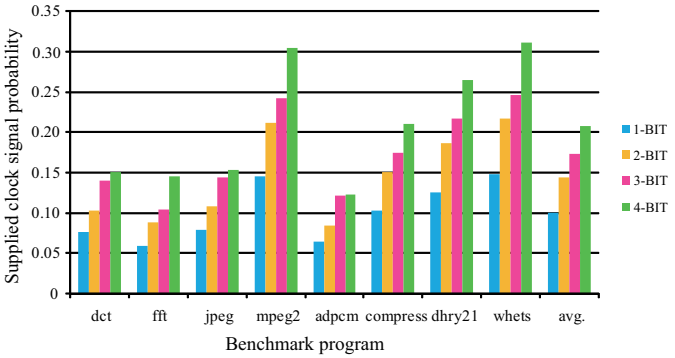

Fig. 8. Average Supplied Clock Signal Probability

be updated, the clock signal is supplied to every internal unified flip-flops. Therefore, as the number of flip-flops unified together increases the average supplied clock signal probability also increases. This may cause an increase of the power consumption of the unified gated flip-flop although the load capacitance of the clock port per bit decreases. Figure 9 shows the power consumption results. Horizontal and vertical axes show benchmark programs and the power consumption values normalized by the power consumption of the registers which employ the normal flip-flops. As can be seen from the Figure, the 4-bit unified gated flip-flop reduces the power consumption of registers in the processor by 44% on an average and by 53% at the best case. If we compare with the normal flip-flop, the 4-bit unified gated flip-flop reduces the power consumption by 57% on an average and by 67% at the best case.

C. consideration

Figure 10 shows the power consumptions of three register circuits in the MeP processor. Vertical axis represents the ratio of the power consumption in the register composed of the 4-bit unified gated flip-flop to the power consumption in the same register composed of the normal flip-flop. In *Reg52*, the power consumption is widely reduced by employing the 4-bit unified gated flip-flop. However, the power reduction depends on the benchmark program. For example, the power consumption can

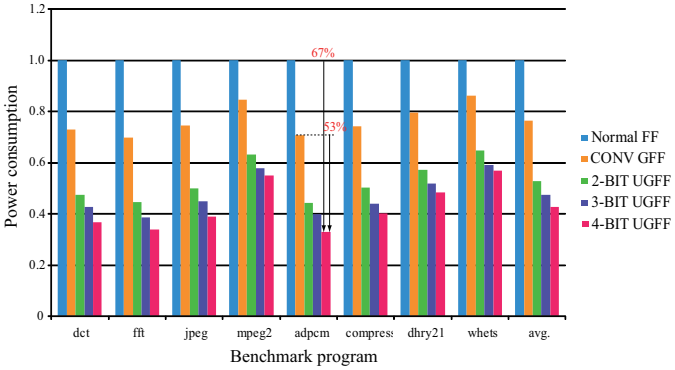

Fig. 9. Power Consumption Results

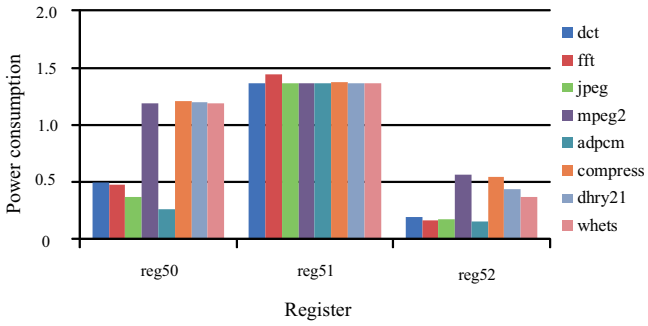

Fig. 10. Power Consumption of Registers

be reduced by more than 80% for *DCT*, *FFT*, *JPEG* and *ADPCM*. In *Reg52*, the power reduction also depends on the benchmark program. This is because *DCT*, *FFT*, *JPEG* and *ADPCM* use *Reg50* and *Reg52* less frequently than the other benchmark programs, and therefore, the unified gated flip-flop can effectively reduce the clocking power consumption in register circuits. These results imply that the power consumption of register in ASICs (Application Specific Integrated Circuits) can be reduced more widely if appropriate types of unified gated flip-flops are selected and applied to the register circuits. Contrarily, if the unified gated flip-flops are applied to registers inadequately, the power consumption of the registers may be larger than that of registers composed of the normal flip-flops. The results for *Reg51* show that the power consumption of the register composed of the 4-bit unified gated flip-flop is larger than that of the register composed of the normal flip-flop for every benchmark programs. This is because all benchmark programs use *Reg51* very frequently and the state of the flip-flop needs to be updated very frequently. Therefore, to such a register, the normal flip-flops should be applied instead of applying the unified gated flip-flops. It is our future work to selectively apply appropriate types of flip-flops to register circuits according to the state transition probabilities of the registers.

V. Conclusions

This paper presents our idea of unifying multiple gated flip-flops for reducing the power consumption in register circuits. Experimental results obtained using an RTL model of a commercial embedded processor demonstrate that our technique reduces the power consumption of register circuits in the processor by 44% on an average and 53% at the best case compared to the register circuits composed of the conventional gated flip-flops. Physical layouts of unified gated flip-flops using a commercial $0.18\mu m$ process technology demonstrate that our technique also reduces the area overhead by 38% compared with the conventional gated flip-flop. The main drawback of our technique is its large delay overhead. Our future work will be devoted to selectively apply appropriate types of flip-flops to registers with taking the circuit delay into consideration.

Acknowledgment

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