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Improving the Quality Factor of Inductor in Si-Substrate by Introducing Fully Depleted PN-junctions

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Abstract: This paper presents a novel technique to improve the quality factor (Q-factor) of a standard inductor in Si-substrate without post-processing. The proposed method employs a distributed grid of N-well in the P-substrate beneath the inductor. This will create a layer of PN junctions. The width of the N-well is chosen wisely so that full depletion occurs in every PN junction, forming a large depleted area which has high resistivity, thus reduces the substrate loss and increases Q-factor of the inductor. An example of the proposed idea is illustrated using a 1nH inductor in 0.18 μm CMOS technology. In this paper, High-Frequency Simulation Structure (HFSS)[1] based on finite element method is used for simulation. As expected, the electromagnetic (EM) simulation shows that the total equivalent resistance of the inductor decreases, resulting in the improvement of its Q-factor by 9%. Finally, the improved inductor is used to design a 5GHz cross-coupled CMOS LC oscillator, which results in an improvement of 2.1dBc/Hz of phase noise at 10 kHz offset frequency.

Keywords: Inductor Layout Optimization, CMOS inductor, Improved Q, LC Oscillator

1. Introduction

The monolithic inductor is a primary component in the radio-frequency integrated circuits (RFICs), especially in the voltage-controlled oscillator (VCO) where it is used in the resonant circuit. The performance of the VCO, especially the phase noise, highly depends on the inductor's quality factor. Considering an LC tank, the quality factor (Q_T) is given by;

$$\frac{1}{Q_T} = \frac{1}{Q_L} + \frac{1}{Q_C}$$

In the design of a VCO, it is important to have a high Q_T because it leads to a VCO with low phase noise and low power consumption operation. The quality factor of the inductor (Q_L) is relatively small compared to that of the capacitor. Therefore, Q_L is the limiting parameter. Consequently, many studies have been done to improve the quality factor of the CMOS inductors.

On the one hand, metallic losses degrade Q_L. Current crowding[2,3] is the phenomenon where the inner turn of the inductor contributes in more metallic losses to the inductor than the outer turn. Therefore, the use of a non-uniform metal width, where the inner turn has a narrower width than the outer turn, has been presented in the references 2) and 3) as a way to increase the Q_L of the CMOS inductor. Also, adopting non-uniform coil spacing increases the Q_L[4]

Moreover, the CMOS inductor suffers from losses due to the CMOS substrate proximity, leading to additional degradation in Q_L. Since the Si substrate has low resistivity, the use of higher resistivity material such as GaAs and SOI[5,6] has been suggested. However, the issue of compatibility with CMOS need to be addressed. Another method to reduce the substrate loss is by completely removing the substrate underneath the inductor structure. This removal can be done by doing selective etching/silicon micromachining techniques[7,8]. However, this method requires additional complicated processing steps during the fabrication. The proton and helium-3 bombardment also have been proposed to reduce the substrate loss in the references 9)–11) by locally creating a semi-insulating substrate area, resulting high-Q inductors. Nevertheless, this method comes with high process cost. In the references 12)-14), active inductors were designed by using MOS transistors to improve Q_L. An active inductor occupies only a small area than a spiral inductor. However, active inductors suffer from high noise, which results in poorer noise performance and higher power consumption.

In this paper, we present a method to reduce the substrate losses and to improve the quality factor of standard CMOS inductor by designing a depletion layer in the Si substrate. No additional steps are required in the fabrication process, and we used the inductor already

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available in the foundry's library. The improved inductor is then used in 5 GHz cross-coupled CMOS LC oscillator to enhance the phase noise. The rest of the paper is organized as follows. Section 2 presents a background discussion on the spiral CMOS inductor and its losses. Section 3 elaborates more on the design of the depletion layer, followed by the simulations results in Section 4.

2. Losses in CMOS Spiral Inductor

There are many ways to layout a planar spiral inductor such as circular, square, hexagonal or orthogonal shape. Circular spiral is the optimum structure. However, it is not supported by many mask generation systems. The hexagonal structure is the closest to the circular shape, and it can be easily layout, even though its quality factor is slightly lower. In this work, the hexagonal spiral inductor was used, which is already available in the foundry's library. The expression of a hexagonal spiral inductor, L, is given by[15]:

$$L = 1.71\frac{\mu_0 n^2 d_{avg}}{\pi}\left[ln\left(\frac{2.23}{\rho}\right) + 0.17\rho^2\right] \quad (1)$$

where μ_0 is the permeability of the free space, n is the number of turns, d_{avg} is the average diameter of the spiral, and ρ is the percentage of the inductor area that is filled by metal traces. Nevertheless, from this expression, neither the information on the quality factor nor on the inductor's losses can be retrieved.

The losses in the inductor can be categorized into two groups: metal losses, and substrate losses. First, the metal losses can be modeled as a series resistance, which is defined by the product of the sheet resistance (Ω/□) and the number of squares in the spiral. The series resistance's value depends on the type of metal used and the thickness of the metal. At higher frequencies, the inductor suffers from "current crowding" as we illustrated in the introduction section. It is due to the eddy currents that are induced by the magnetic field and penetrates into the metal coil. On top of that, the skin effect becomes significant at frequencies above 2 GHz, which further increases the metal losses of the inductor.

Secondly, the CMOS inductor faces severe energy loss due to the low resistivity of the substrate, which sees large current flows to the substrate and degrades the quality factor of the inductor. The primary source of the substrate

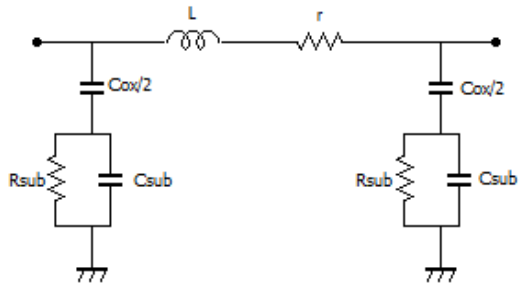

Figure 1. Lump circuit model of a CMOS inductor.

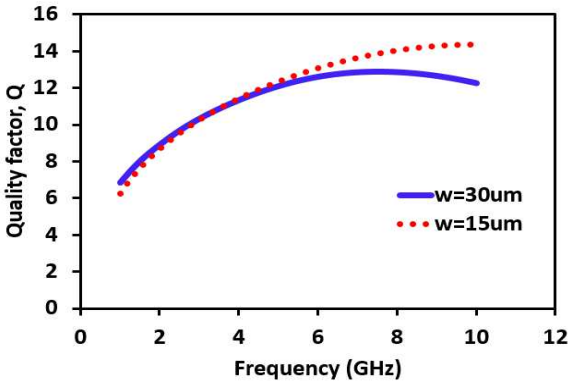

Figure 2. The simulated quality factor of a CMOS inductor for trace width of 15µm and 30µm.

loss is the capacitive coupling, where the conduction current from the coil flows into the substrate.

Another source is the inductive coupling due to the penetration of magnetic field into the substrates. **Fig. 1** illustrates the lumped circuit model of the inductor, where L represents the inductance, r is the series resistance, R_{sub} and C_{sub} represent the resistive and capacitive losses in the CMOS substrate, respectively.

Optimum design of a CMOS inductor requires that the spiral trace is as wide as possible until the skin effect becomes significant. For a good design at high frequency, the spiral trace is between 9 µm and 15 µm. In fact, by using wider spiral traces, the series resistance, r, can be reduced. However, R_{sub} will also decrease, which resulting more losses to the substrate, and thus mask the benefit of having a small r. **Fig. 2** shows the quality factor of the CMOS inductor for trace widths of 15 µm and 30 µm. At lower frequencies, the inductor with a trace width of 30 µm has better quality factor due to the small series resistance. However, beyond 3 GHz, the skin effect becomes more apparent, as well the couplings to the

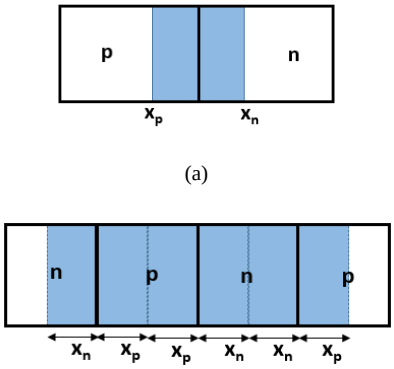

Figure 3. A PN junction with depletion area (a) Construction of a large area of depletion layer (b)

substrate becomes stronger, which results in a lower quality factor.

Therefore, to use a wider spiral trace for the inductor at high frequency, we propose a method to increase the resistivity of the substrate. It can be achieved by creating a full depletion layer in the substrate, underneath the inductor structure. Since the depleted area almost has no carriers, the resistance of this area approaches infinity. The advantage of using this method is that it does not require additional steps in the fabrication process. Moreover, standard CMOS inductor from the foundry's library can be employed. In 2005, Jian *et. al.*.[16] proposed the use of PNP substrate isolation structures (JSIS) to reduce substrate loss. In the reference 16), the N-well is biased to control the size of the depletion layer. On the contrary, we propose employing the properties of full depletion of PN-junction, which does not require any external biasing voltage.

3. Full Depletion Layer in Si Substrate

To use wider spiral trace and to increase the resistivity of the substrate, we propose an implementation of a depletion layer underneath the inductor's structure. For that, the theory of PN-junction is employed. Consider a PN-junction as shown in **Fig. 3 (a).** At the junction's interface, the electrons from the N-well and holes from the P-substrate start to cross to the other side until it reaches the equilibrium state. In return, a depletion area which is almost free from any carriers is formed at the junction. Due to the limited number of carriers, the resistivity of this depletion area is much higher than any remainder of the device. This area is defined by x_n and x_p, with x_n is the depletion region in N-well and x_p is the depletion region in P-substrate. The expression of x_n and x_p are as follows[17]:

$$x_p = x_d \frac{N_d}{N_d + N_a} \qquad x_n = x_d \frac{N_a}{N_d + N_a} \tag{2}$$

$$x_d = \sqrt{\frac{2\varepsilon_s}{q}\frac{N_a + N_d}{N_a N_d}(\phi_i - V_a)} \tag{3}$$

where N_a and N_d are the doping concentration in the P-type and the N-type semiconductors respectively, q is the electron's charge, ε_s is the permittivity of silicon, V_a is the applied bias voltage, ϕ_i is the built-in voltage, and x_d is the total width of the depletion area.

In order to obtain a full depletion layer, a distributed grid structure of N-well is designed in the P-substrate to create the PN junctions. From **Fig. 3 (b),** we can see that the width of each N-well has to be $2x_n$ in width with separation $2x_p$ to have a full depletion on the desired area. To calculate the value of x_p and x_n, the value of the variables used in the calculations are as follows:

- Acceptor concentration, $N_a = 1.35 \times 10^{15}$ cm^{-3}
- Donor concentration, $N_d = 5.0 \times 10^{15}$ cm^{-3}
- Electron's charge, $q = 1.6 \times 10^{-19}$ C

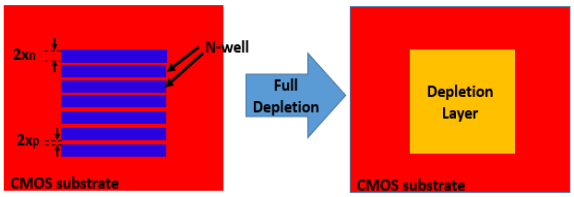

Figure 4. Top-view of the distributed grid N-well on CMOS substrate and its equivalent depletion area.

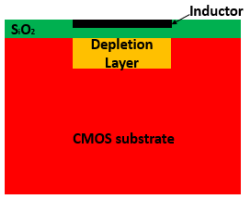

Figure 5. Cross-section of the whole structure.

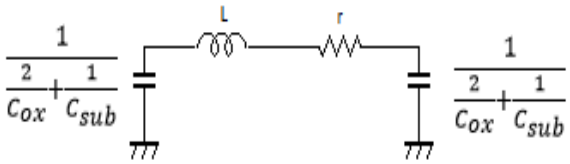

Figure 6. Simplified lump circuit model of inductor with depletion layer.

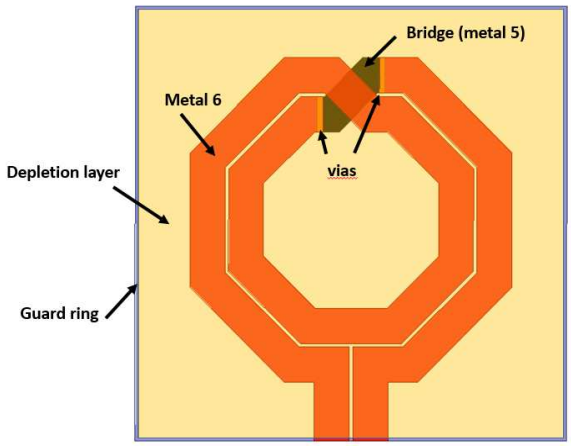

Figure 7. Layout of a symmetrical inductor (width trace=30 µm).

- Permittivity of silicon, ε_s = 1.034 x 10^{-10} Fm^{-1}
- Boltzmann constant, k = 1.38 x 10^{-23} JK^{-1}
- Intrinsic carrier concentration, n_i = 1.45 x 10^{10} cm^{-3}

Applying Eq. (2) and Eq. (3), we obtained $2x_n$=0.3816µm and $2x_p$=1.4136µm. The thickness of the depletion layer is 20µm. The length of the N-well stripes depends on the value of the inductor because the higher the value, then the larger the inductor. Therefore, larger depletion area is required. In our case, we used an inductor of 1 nH, which size is 363 µm x 363 µm including the guard ring. The size of created depletion area is 361µm x 361µm. **Fig. 4** illustrates the top view of the distributed grid N-well on CMOS substrate with its equivalent depletion area. **Fig. 5** shows the cross-section of the whole structure. By implementing the depletion layer underneath the inductor, the conductivity of the substrate in that area is almost zero and the resistivity becomes very high. Hence, R_{sub} can be neglected, and the lump circuit model reduces to the circuit in **Fig. 6.** The value of C_{ox} is 4.316 µF/m² and the

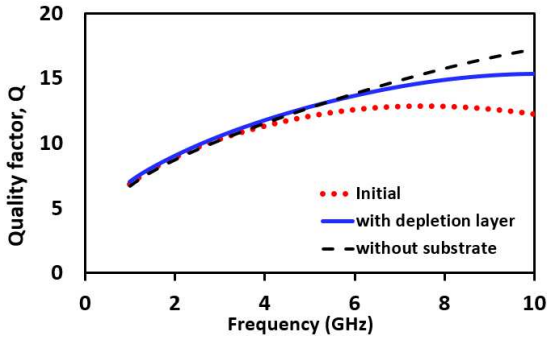

Figure 8. Quality factor of inductors.

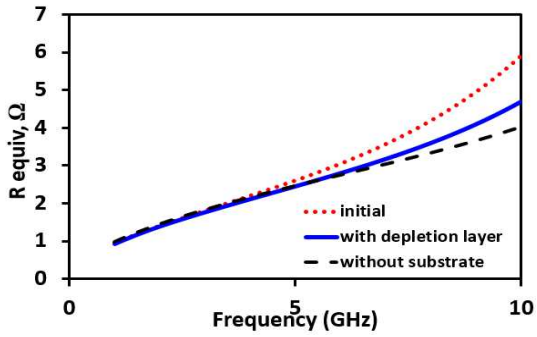

Figure 9. Total equivalent resistance of inductors.

value of C_{sub} is 0.505 µF/m². Based on simulation, for a 1 nH inductor, the series resistance is about 1.25 Ω.

4. Simulation Results and Discussions

In this work, a symmetrical inductor, which layout is illustrated in **Fig. 7** was used. It is on metal M6 with a bridge on metal M5, and M6 and M5 are connected by vias. The size of this inductor is 363 µm x 363 µm including the guard ring. Since it is going to be used in the 5 GHz cross-coupled CMOS LC oscillator, the value of the inductance is about 1nH. We describe more details about the selection of the inductor value in the following paragraphs. In this paper, High-Frequency Simulation Structure (HFSS) based on finite element method is used to perform the S-Parameters simulations. The depletion layer is modeled as a silicon with ε_r = 12, σ = 0.1 S/m and a depletion thickness = 20 µm. The depletion layer is in a square shape, laying below the inductor structure and the guard ring. From the S-Parameter simulations, we can obtain the value of the inductance and the total equivalent resistance of the inductor. **Fig. 8** compares the quality factor of the inductor of a 30µm trace width for different cases: the initial

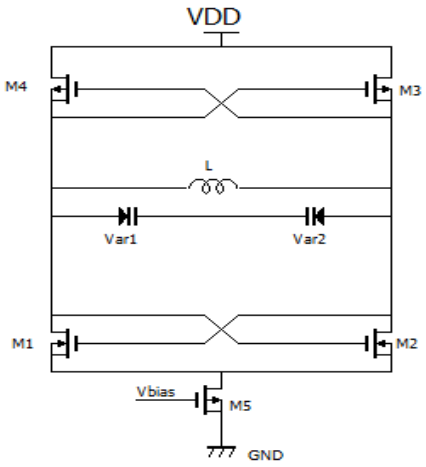

Figure 10. Cross-coupled LC oscillator.

inductor, the inductor with depletion layer and the inductor without substrate (the ideal case). At lower frequencies, the performance of Q for all cases are almost the same. However, above 4 GHz, due to larger R_{sub} (therefore smaller current leaks to the substrate), the inductor with depletion layer gives higher quality factor compared to the initial inductor (foundry inductor). This enhancement can also be explained by means of total equivalent resistance, R_{equiv} which represents the total losses of the inductor. **Fig. 9** show the inductor with depletion layer has lower R_{equiv}, and thus lower losses, which explains its better quality factor at that range of frequencies. At our frequency of interest, which is 5 GHz, a 0.88 improvement in Q_L is observed, resulting in a new Q_L=13.25. Better improvement is seen at a higher frequency, with 2.03 and a 3.1 improvement at 8 GHz and 10 GHz respectively.

The performance of the inductor with depletion layer is also compared with the ideal case without the substrate. The proposed inductor's quality factor exhibits only a small difference at our frequency of interest. However, at higher frequencies above 5 GHz, the inductor without substrate has better performance, both in quality factor and total equivalent resistance, because the inductor with depletion layer still suffers from the substrate capacitor, C_{sub}. At high frequencies, the C_{sub} acts like low impedance, therefore, more current losses to the ground.

A 5 GHz LC cross-coupled oscillator was designed in CMOS 0.18 µm, which schematic is illustrated in **Fig. 10**.

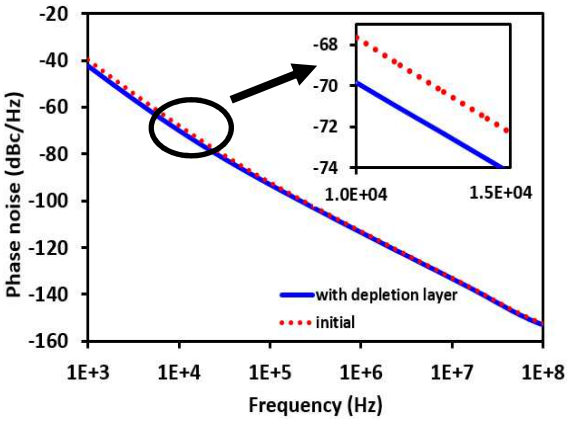

Figure 11. Phase noise performance of the oscillator. At the top right corner is a zoom in of phase noise in $1/f^3$ region.

The transistors M1, M2, M3, and M4, are the NMOS and PMOS cross-coupled pairs. The transistor M5 acts as a current source. This oscillator uses MOS varactor for tuning. The inductor with depletion layer in the substrate was used. The power supply is 1.5 V, and this circuit consumes 0.53 mA. In **Fig. 11,** the simulation results shows that there are improvements in the phase noise both in $1/f^3$ and $1/f^2$ regions, which are about 2.4 dB and 1 dB improvement, respectively. At 10 kHz offset from the carrier, the phase noise of this oscillator is -69.84 dBc/Hz.

In order to compare the performance of this oscillator with other published work in the literature, a common figure of merit (FOM) is used. The FOM takes into account the phase noise (L) at the offset frequency (Δf) from the carrier frequency, f_0. The FOM is given by:

$$\text{FOM} = L\{\Delta f\} + 20log_{10}\left(\frac{f_0}{\Delta f}\right) + 10log_{10}\left(\frac{P}{1mW}\right) \quad (4)$$

Base on Eq. (4), the FOM of this 5 GHz LC oscillator is 183.3. **Table I** summarizes the performance of the design oscillator by using an inductor with depletion layer in the substrate and compare with recent literature papers.

5. Conclusions

In this paper, a method to reduce the loss due to the substrate in a monolithic CMOS spiral inductor has been proposed. By using the properties of the full depletion layer of PN-junction, a large depletion area is created in the p-substrate, which results in a higher resistivity of the substrate. The Q_L of 1 nH inductor is improved by 9% from

its initial value at 5 GHz, and larger improvement could be expected at higher frequencies with the larger inductors. The EM simulation shows that 16% and 25% improvement of Q_L at 8 GHz and 10 GHz respectively. This improved inductor is used in 5 GHz cross-coupled LC oscillator, and better phase noise is achieved.

Table I Performance summary and comparison with other published results.

	This work* (initial inductor)	**This work* (improved inductor)**	**Ref[18] 2011****	**Ref[19] 2012****
Process	CMOS 0.18 µm	CMOS 0.18 µm	CMOS 0.18 µm	CMOS 0.18 µm
Vdd (V)	1.5	1.5	1.4	1.0
f_0 (GHz)	5.18	5.16	4.9	5.32
Power (mW)	1.18	1.18	2.49	2.30
L@10kHz (dBc/Hz)	-67.65	-69.84	-65.1	-68.0
Tuning Range	18.0%	18.0%	14.7%	14.1%
FOM	181.1	183.3	174.9	178.9

*Simulation results **Measurement results

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