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Design of a Differential Delay Circuit with 100ps Resolution

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Abstract: In this work, a digital controlled differential delay circuit for BOST(build-out-self-test) with hundreds picosecond resolution is presented. The proposed circuit operates with high speed at 500MHz under 1.8V supply according to Hspice simulation and shows a wide range operation and low static power. It also performs symmetrical rise and fall operation.

Keywords: Build-out-self-test(BOST), Phase-locked loop(PLL)

1. Introduction

Recently, with the progress in LSI technology, demands to reduce testing costs and times have become especially a key issue. Accordingly, some methods that utilize hardware to facilitate testing have been proposed. A method of testing a system LSI is BIST (build-in-self-test), in which a test circuit is embedded within the chip of the system LSI. Another is BOST (build-out-self-test), in which a part of testing signals are provided from the chip on a load board of an LSI tester [1]. Since BOST can put many test units on the performance-board and achieves high speed, low cost measurement, it will be widely used for test system. This paper attempts to determine a differential delay cell topology to answer the accurate edge placement control in ATE(automated test equipment). The proposed circuit can provide a delay time less than 100ps for 1 LSB and 6.4ns for 1 MSB. The circuit can be used with high speed comparator in the BOST LSI tester.

We investigated a qualitative discussion for three basic delay cells. The first delay cell (shown in **Fig.1**) is the conventional single-ended current-starved inverter cell. While this cells provide low intrinsic device noise and high signal-to-noise ratio(SNR), mainly due to its full voltage swing, it has a poor power supply rejection ratio(PSRR) [2]. It is difficult to obtain the same rise and fall time of two output signals by using this delay cell. The input-output response simulation results of the delay cell was shown in **Fig.2**. The delay time of rising edge and falling edge are not consistent. **Figure 3** shows the characteristics of the rise delay time and fall delay time when we use the basic delay cell which shown in **Fig.1**. From **Fig.3**, it is obvious that the rise and fall delay time at Vdd/2 are too different to use for measurement equipment. In order to overcome this asymmetrical problem, increasing the numbers of inverters is necessary. We use a pair of the basic delay cell, the same delay time of rise and fall edge will be achieved. But, with increasing the numbers of inverters, the step of delay time to be controlled become larger. In our previous work [3], a delay cell which used even numbers single-ended current-mode configuration was presented. The rising and falling edge characteristics was shown in **Fig.4**. The rise delay time is consistent with fall delay time in the range of 232ps-246ps. And, by using PLL, 2ps precision was achieved. The drawback of this cell is the operation in low speed (250MHz) and narrow range of controllable delay time (nearly 14ps).

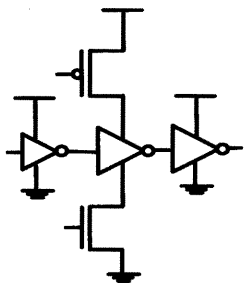

Fig. 1 Conventional single-ended delaycell.

The differential delay cell is less sensitive to common-mode voltage variations, supply voltage variations, and it is more suitable for mixed-mode applications [2]. The drawback of the source coupled differential delay cell (shown in **Fig.5**) is the high power consumption because of the static bias current flows in the circuit.

The parallel configuration delay cell of the dynamic single-ended (shown in **Fig.6**) was tried for

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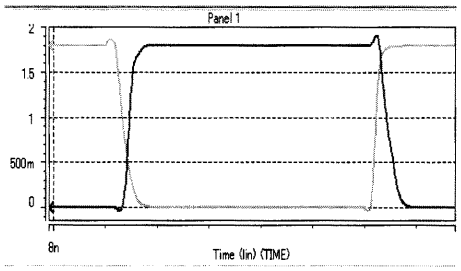

Fig. 2 The input-output response simulations results of single-ended delaycell.

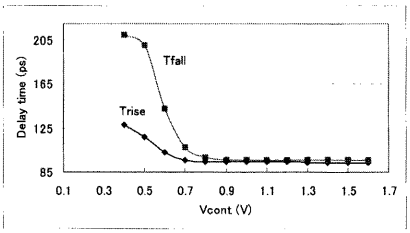

Fig. 3 Values of Trise(delay time at rising edge) and Tfall(delay time at falling edge) versus Vcont(controlled voltage) for single-ended delaycell.

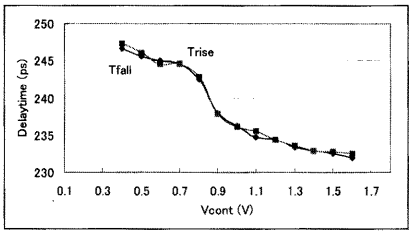

Fig. 4 Values of Trise and Tfall versus Vcont for single-ended delaycell(using even numbers of inverters).

differential input. Although it gave low power consumption, asymmetrical problems still exists. Because the each side transistors worked independently, it causes the different delay at rise and fall edges as same as **Fig.1**'s circuit. The simulation result of rise and fall time delay was shown in **Fig.7**. The largest difference between rise and fall delay time is nearly 5ps. In this configuration, the upper and lower transistors can be replaced by one transistor because of the push-pull operation.

To obtain the low power consumption, the high speed performance and the symmetrical input-output characteristic, a new differential delay cell is proposed as shown in **Fig.8**. This basic design is same as the single-end delay cell, a dynamic switch architecture is used in order to achieve the low power consumption. By adjusting the current, the rise and fall delay time can be manipulated.

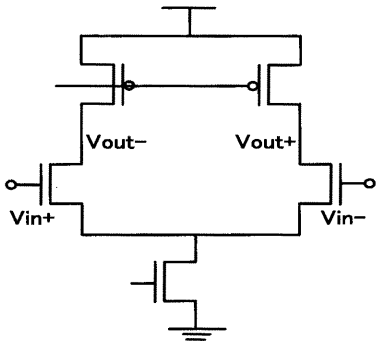

Fig. 5 Conventional differential delaycell.

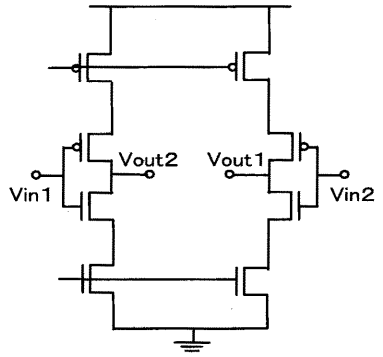

Fig. 6 Parallel configuration of the dynamic single-ended delaycell.

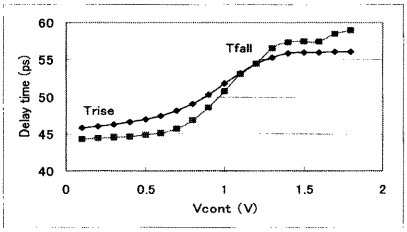

Fig. 7 Values of Trise and Tfall versus Vcont for parallel configuration of the dynamic single-ended delaycell.

The bottom NMOSFET and the top PMOSFET are used for charging and discharging supply like as a resister. The same gate voltages are also provided as delaycells in the PLL's. Latch circuit configuration is used to improve the symmetry of rise and fall time, by using the positive feedback mechanism. The transistors of the slower branch delaycelll is accelerated by the faster branch change.

2. Architecture

A simplified block diagram of the proposed delay adjustment circuit is shown in **Fig.9**. The architecture consists of three primary circuit blocks: a

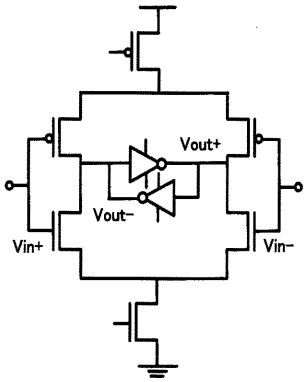

Fig. 8 Proposed differential cell circuit.

phase-locked loop, a delay adjustment section and a 6 bit digital switch.

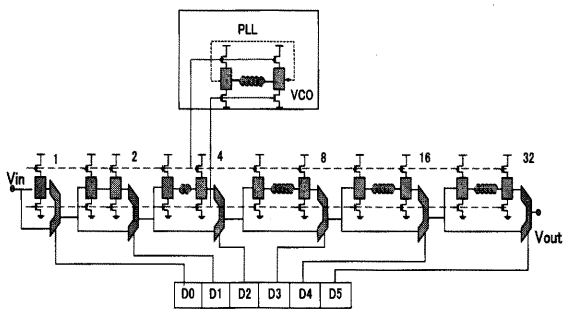

Fig. 9 Simplified block diagram of the delay adjustment circuit.

The delay adjustment section consists of 6 delay chains with multiplexer. By using the 6 bit digital switches, the circuit provide a digital control with available delay step resolution. Each delay line consists of a series of controllable delay cells. Propagation delay adjustment is accomplished using a series of basic delay cells and multiplexer. The cascading architecture increases the range of overall delay. The 6 bit digital switch is used to drive the selection lines of each multiplexer. When the D0 to D5 are ON, all of 63 delay cells in 6 delay chains are selected. A PLL circuit is designed for stabling the delay circuit. As a critical part of PLL, voltage-controlled oscillator (VCO) is composed of 32 basic delay cells which are used in the delay chains. Because the VCO cells and delay cells are same, by adjusting the reference signal of the PLL under the locked state, the delay time can be manipulated for a wanted value in a time region. The schematic of a delay circuit unit is shown in **Fig.10**. The proposed circuit contains two parts: delay element section and multiplexer. In 6 delay chains, the delay elements are composed of 1, 2, 4, 8, 16, 32 basic delay cells, respectively. Compared this design with our previous work, the numbers of transistors are reduced, therefore, higher operation speed will be expected.

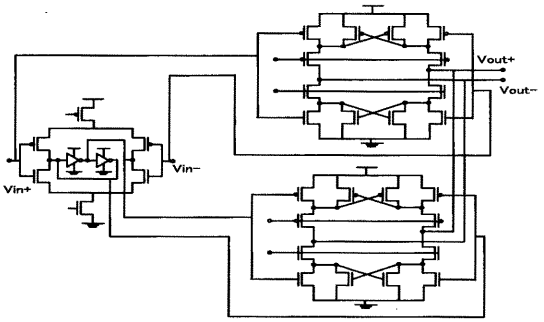

Fig. 10 The schematic of delay unit circuit.

Figure 11 shows the PLL circuit, which is composed of 6 main components: phase/frequency detector (PFD), charge pump (CP), loop filter, V-bias circuit, VCO, and divider. All of the components are designed in CMOS process except the RC loop filter. The negative feedback gives the PLL the ability to lock.

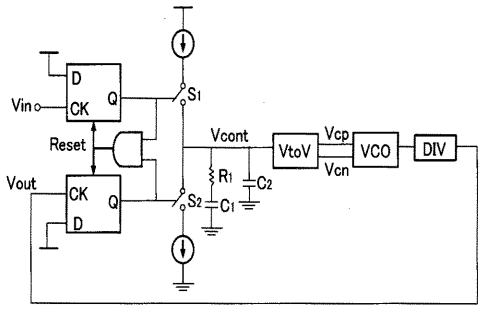

Fig. 11 The block diagram of PLL circuit.

The primary purpose of the PFD is simply to measure the difference in phase between the two input signals and produce an output that is proportional to the difference. Since the objective of the PLL is to ensure that the feedback signal is equal to the reference signal, the PFD commands the rest of the PLL to either lower or raise the frequency coming out of the VCO. The PFD circuit is composed of two D flip flops and one AND gate. The up and down output of the PFD is tied to the CP current source which is composed of a simple current mirror circuit. In this design, a passive RC filter is used to smooth the output of the PFD, and to provide the V-bias circuit a DC signal having the least ripple. Capacitor C2 integrates the CP currents, R1 and C1

reduce the ripple on the DC signal to V-bias circuit. About the parameters of the R1, C1, as the reference [4], the optimum conditions is the C1=8*C2. The product of R1 and C1 are set to larger value than the repletion time of the PLL reference signal. R1=10k, C1=25pf, C2=8pf were set in this design.

The V-bias circuit is inserted between the loop filter and the VCO, and it generates two bias voltages Vcp and Vcn, and provides them to the current source transistor of delay cell which replace the dynamic switch. **Figure 12** shows the V-bias circuit and its simulation results was shown in **Fig.13**. Vcp and Vcn change in the region of 0.6V to 1.25V.

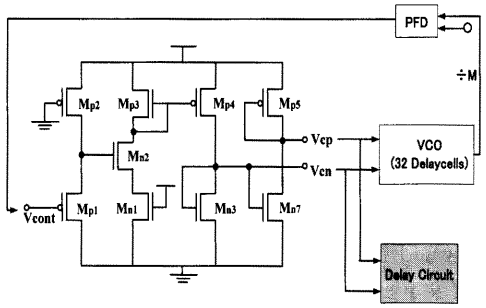

Fig. 12 The schematic of V-bias circuit.

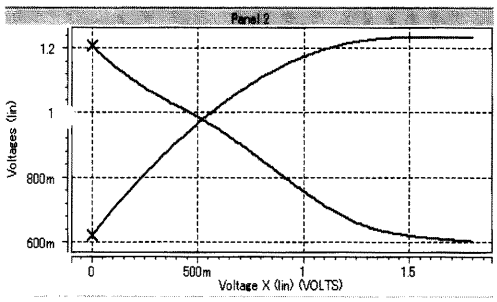

Fig. 13 Simulation results of the V-bias circuit.

3. Simulation Results and Discussions

The proposed delay circuit was simulated with the TSMC018 CMOS process model by Hspice. The performances of the PLL circuit and the delay section are verified through the simulation. **Figure 14** and **15** show the delay circuit simulation results, when setting all of the 6 bit digital switches in ON and OFF respectively. When all of the switches are OFF, only 6 multiplexers work. In **Fig.14**, we can get 6 delay chain's output waveforms are symmetrical and the rise delay time is 0.6136ns, fall delay time is 0.6158ns (in our previous work [3], the value was about 3.6ns). When all of the switches are ON, 6 delay chains and 6 multiplexers work. **Figure 15** shows 6 delay chain's output waveforms are also symmetrical and the rise delay time and fall delay time is 5.5953ns and 5.5823ns, respectively (in our previous work [3], the value was about 15.75ns). The proposed differential delay circuit can operate at 500MHz (in the previous work, the highest input signal is 250MHz.) Under the PLL locked state, since the delay time of the delay cell is variable, the whole delay time also can be manipulated by adjusting the PLL input reference signal. Total power consumption including PLL circuit is 18mW.

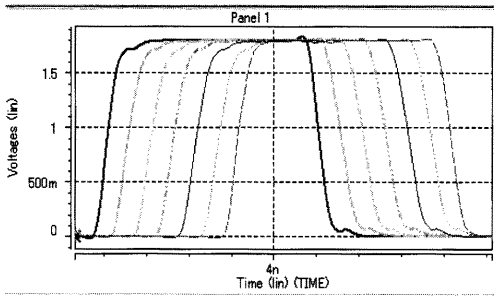

Fig. 14 The input-output response simulation results of delay circuit (Minimum delay).The input signal is 500MHz.

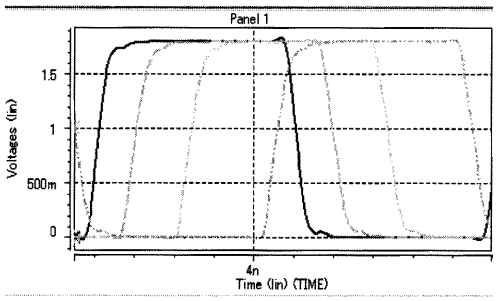

Fig. 15 The input-output response simulation results of delay circuit (Maximum delay).The input signal is 500MHz.

Figure 16 shows the delay cell's rise and fall delay time characteristics. It is obvious that the delay time can be manipulated the range of 80ps to 105ps (25ps controllable time range) by adjusting the value of Vcont. In our previous work [3], the controllable time range was only 14ps. It also shows the consistent of the rise and fall delay time and verifies the credibility of output signal symmetry analysis in the section 2. As shown in **Fig.16**, the largest difference between rise and fall time is less than 1.5ps.

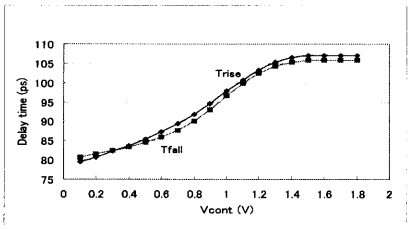

Fig. 16 Values of Trise and Tfall versus Vcont for proposed differential delay cell.

4. Conclusion

In this paper, a differential delay circuit proofed by PLL for Built-Out-Self-Test has been designed in CMOS process. The proposed circuit can operate in 500MHz under 1.8V supply with the delay resolution of less than 100ps and only 18mW of power consumption. The whole controllable range is less than 6.4ns under PLL locked state with a high precision. The simulation results confirm the qualitative analysis. The proposed circuit is useful of the high speed LSI tester for BOST.

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