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A Recessed Channel MOSFET with Plasma-grown Silicon Oxynitride Gate Dielectric

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Abstract: Fabrication and electrical characterization of a recessed channel n-MOSFET on a p on p^+ epi-layer and with plasma-grown silicon oxynitride (SiON) as the gate dielectric, are reported. This non-planar MOSFET structure was devised to have suppressed short channel effects; and the effects of plasma-grown SiON on the device characteristics were studied. The proposed structure was fabricated by using anisotropic wet etching to etch the channel and by using solid phase diffusion to form the source and drain. The gate silicon oxynitride layer (thickness 7nm) was fabricated by nitridation of pre-grown SiO_2 in a nitrogen plasma. The pre-oxide was also grown by oxidation of Si in oxygen plasma. Plasma-grown gate SiON showed higher breakdown strength over plasma-grown SiO_2. MOSFETs (L/W=2.2μm/22μm) with plasma nitrided gate SiON demonstrated higher on-state currents compared with devices with plasma-grown gate SiO_2. The improved on-state currents are related to increased channel carrier mobility which is supposed to be due to interface property improvements brought about by plasma nitridation.

Keywords: MOSFET, Recessed channel, Silicon oxynitride, Plasma nitridation, Mobility

1. Introduction

Higher performance from integrated circuits (ICs) has been achieved by continual scaling of the metal-oxide-semiconductor field-effect-transistor (MOSFET)[1]. Scaling of the conventional Si-SiO_2 based, planar MOSFET has come so far that it has reached fundamental material and physical limits; and hence, new materials, device structures and processes are being investigated in order to continue the present IC performance trends[1)-3)].

MOSFET scaling has resulted in gate dielectric thickness reduction to a few nanometers. The decreasing device dimensions while supply voltages are not being scaled proportionally have caused significant increase in the internal electric fields which could give rise to hot carrier generation. The reliability of the gate SiO_2 has degraded due to inevitable high tunneling leakage currents through the ultra-thin oxide and due to increased hot carrier injection into the gate dielectric. At ultra-thin levels, gate SiO_2 also suffers from dopant (boron) penetration. The dielectric silicon oxynitride (SiON) has been identified to be a replacement for SiO_2 due to its improved reliability over pure SiO_2; especially, enhanced resistance to high field stressing, improved hot carrier immunity and resistance against dopant penetration[2]. SiON grown by the widely used method of thermal nitrtidation of SiO_2 in NH_3 however has disadvantages of high densities of fixed charges, electron traps and interface states. Further, the thermal methods incorporate a higher N content at the oxide/Si interface which leads to mobility degradation of channel carriers in MOSFETs. Growth of SiON by nitridation in nitrogen plasma has shown potential to grow ultra-thin SiON films with fewer drawbacks.

The conventional planar MOSFET scaled down to sub-micrometer channel lengths suffers performance degradation due to short channel effects. In order to suppress short channel effects shallower source/drain (S/D) junctions, higher doping densities and steeper doping profiles, and thinner gate oxides are needed[2]. However, thinner S/Ds cause higher series resistance; higher doping levels cause increased impurity scattering and higher junction capacitance; and thinner gate dielectrics cause higher gate leakages thus affecting device performance. There are also technological limitations of forming ultra-shallow S/D and steep dopant profiles, and of nano-scale patterning. Several non-conventional device structures with non-uniform substrate doping profiles have been investigated to overcome short channel effects[3]; namely, delta-doped (DD) MOSFET, pocket implanted (PI) MOSFET, epitaxial (epi-) MOSFET and silicon-on-insulator (SOI) structures. They have exhibited improved short channel effect suppression at the expense of process complexity, and degraded perfor-

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mance in some cases. Recessed channel structures with thick S/D and shallower junction depths have been proposed to have suppressed short channel effects while having reduced S/D resistance.

We have devised a non-planar structure with a recessed channel on a p on p^+ epi-layer so as to have thick S/D, zero junction depth and a lightly doped channel layer. The simulated device characteristics showed that at sub-micrometer channel lengths this structure can effectively suppress short channel effects without appreciable effect on the on-state currents[4].

The present work investigates the feasibility of fabrication of the devised recessed channel (RC) MOSFET with plasma grown SiON as the gate dielectric, and its device characteristics. Both the aspects of gate dielectric improvement and device structure modification were combined due to their respective contributions to reliability and performance improvements of scaled MOSFETs. Fabrication of the proposed structure was achieved by using anisotropic wet etching to etch the channel and by using solid phase diffusion to form the source and drain. The gate oxynitride was grown by nitrogen plasma nitridation of plasma-grown SiO_2. Plasma oxidation was required to grow the pre-oxide since the use of high temperature rapid thermal oxidation resulted in a defective oxide. The devices with plasma-grown gate SiON showed higher drain currents compared with devices with plasma-grown gate SiO_2.

2. Fabrication of RC-MOSFET

p on p^+ epitaxial Si wafers (boron doped) with (100) orientation were cleaned in standard SC1 RCA cleaner, washed in deionized water and dried in N_2. The initial thickness and resistivity of the p layer were 4μm and $\sim$ 10Ωcm ($N_p \sim 5x10^{15}cm^{-3}$), respectively, and the resistivity of the p^+ layer was $\sim$ 0.01Ωcm ($N_{p+} \sim 1x10^{18}cm^{-3}$) as measured by spread resistance profiling. Phosphosilicate glass (PSG) was then spin-coated on the cleaned Si wafer and the wafer was annealed by rapid thermal method (RTA) in N_2 at 900°C in order to heavily dope (n^+) a thin surface layer with phosphorous by the solid phase diffusion process. Thereafter, the PSG layer was removed by dipping in buffered HF and a thick SiO_2 layer was grown by rapid thermal oxidation to serve as an etching mask for KOH wet etching.

The thick SiO_2 layer was then patterned according to the source and drain region pattern by electron beam lithography followed by SiO_2 etching in CF_4 plasma. Anisotropic wet etching of Si was carried out using a 55% KOH solution at room temperature in an ultrasonic bath to etch the U-shaped channel. Etching was stopped before complete V-shape formation. After channel etching, a thin oxide was grown by oxidation in inductively coupled oxygen plasma. Oxidation was carried out in O_2/Ar plasma at rf power of 500W and discharge pressure of 1Pa. Some samples were then plasma nitrided in nitrogen plasma at rf power of 500W and discharge pressure of 0.6Pa. After plasma nitridation (/oxidation) samples were annealed in N_2 at 600°C. The source/drain and gate electrodes were formed by sputter deposition of Al and patterning by UV lithography and wet etching. After electrode formation, devices were subjected to a post metallization annealing in N_2 at 400°C.

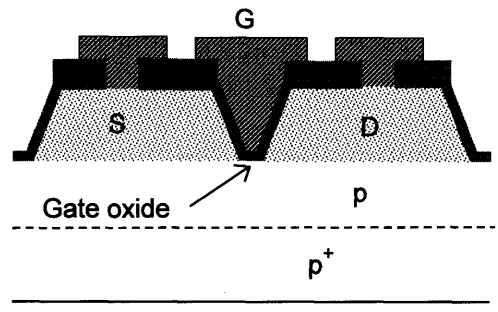

Fig. 1 Cross-sectional diagram of the fabricated RC-MOSFET.

The fabricated MOSFETs were characterized by spread resistance profiling for determining S/D junction depths and the position of the p/p^+ junction; and by SEM measurements to determine the channel dimensions. The electrical characteristics of the devices were obtained using a probe station (Cascade Microtech) and a semiconductor parameter analyzer (HP 4156A).

3. Device Characteristics

(a) Device Geometry: Figure 1 shows a cross-sectional diagram of the fabricated MOSFET. KOH etching of Si (100) surfaces results in a V-shaped groove in the <110> direction with (111) planes as its slanting sides due to the much higher rate of etching of (100) surfaces compared with (111) surfaces. SEM measurements showed that the etched groove has atomically flat surfaces. **Figure 2(a)** shows an FIB image of the layout of the fabri-

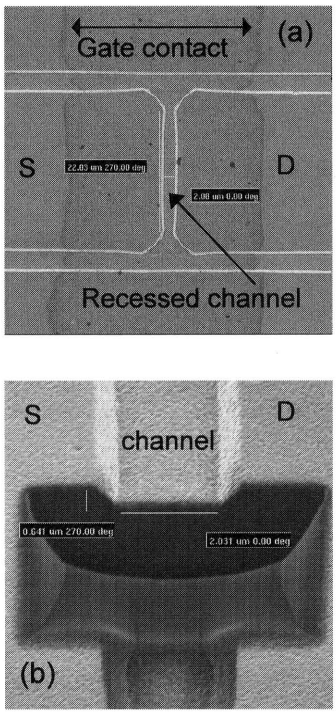

Fig. 2 (a) FIB image of the layout of the RC-MOSFET. (b) FIB image showing the grooved channel of the RC-MOSFET after metallization. (angle of view: 45° to the top surface)

cated RC-MOSFET structure and **Fig. 2(b)** is an FIB image viewed at 45° showing the grooved channel after metallization. The channel dimensions were: length, 2.2μm and width, 22μm, and the channel (groove) depth was 0.64μm as determined by SEM measurements. S/D junction depth was determined by the spread resistance depth profiler (SRP). **Figure 3** shows the SRP profiles of both the RC-MOSFETs with SiO_2 and SiON as the gate dielectric after the complete fabrication process. According to the resistance profiles the p/n junction depth is 0.55μm and there is no difference in the S/D junction depths between samples with SiON and non-nitrided SiO_2. This is a result of the very low temperatures involved in the plasma nitridation process. SRP obtained just after P diffusion however showed lower junction depths indicating that subsequent high temperature processes cause dopant re-diffusion. The p-layer thickness after the complete fabrication process was 2.5μm. The average thickness of the gate oxide and oxynitride layers was 7nm when calculated from high frequency C-V measurements.

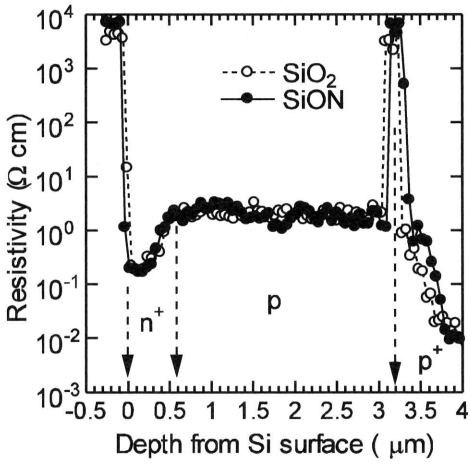

Fig. 3 Spread resistance profiles (SRP) of the RC-MOSFETs with gate SiO_2 and SiON, after the complete fabrication process.

(b) Gate Oxide Characteristics: The leakage current and break down characteristics were evaluated for gate oxides in a recessed channel structure, which was fabricated without S/D diffusions. The dimensions of the test oxides on the groove were: width at the groove bottom, 15μm; length, 55μm; and the oxide area, 17x55μm^2. These test structures were used to evaluate the oxide thickness by high frequency C-V measurements. The gate electrode covered parts of the thick oxide layer on the S/D regions, and it was assumed that the leakage current through the thick oxide (110nm) was negligible compared with that through the thin (7nm) gate oxide.

Figure 4 shows the typical leakage current characteristics of the oxide and oxynitride films in the recessed channel structure. In general, at higher ox-

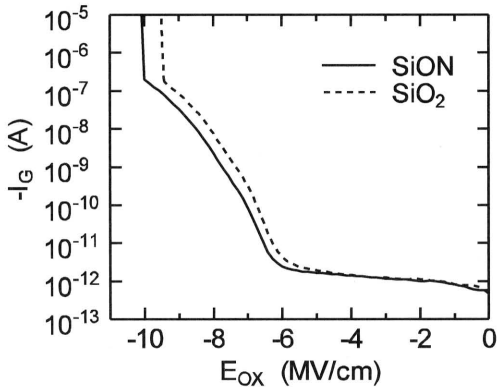

Fig. 4 Leakage current characteristics of the SiO_2 and SiON gate dielectrics in the recessed channel structure.

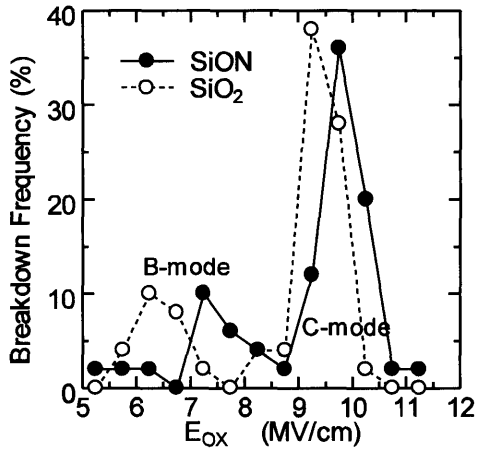

Fig. 5 Breakdown characteristics of the SiO_2 and SiON gate dielectrics in the recessed channel structure.

ide fields, leakage current was a little lower for SiON possibly due to a change in the Fowler-Nordheim tunneling parameters. The time-zero breakdown characteristics of the films shown in **Fig. 5** indicate improvements in the breakdown strength for SiON. C-mode fields have shifted by $\sim$ 0.5MV/cm and B-mode fields by $\sim$ 1MV/cm to higher fields upon nitridation.

(c) Electrical Characteristics of the RC-MOSFET: The electrical characteristics of the RC-MOSFETs were investigated to evaluate the feasibility of device fabrication as well as to observe the effects of plasma nitridation of the gate oxide on device performance.

Linear characteristics (I_D vs V_G) of the RC-MOSFET for the drain voltage V_D=0.05V are shown in **Fig. 6**. Evaluation of threshold voltage gave values of 0.045V for the MOSFET with SiON and 0.070V for SiO_2. The almost the same threshold voltage values indicate that there have been no structural changes or dopant profile modifications as a result of the additional plasma nitridation process.

Figure 7 shows the subthreshold characteristics of the RC-MOSFET for V_D=5V and 0.05V. A substantial increase in the subthreshold (near threshold) leakage current could be observed with increasing drain bias. This is not due to punch through effect (short channel effect), but was observed to be partly due to increased junction leakage in the not yet optimized S/D structures. The increase of the subthreshold current when the gate voltage is decreasing (increasing in the negative direction) as seen in the curves for V_D=5V, is typical of the gate induced drain leakage (GIDL) effect. GIDL is a result of the electron-hole pair generation by band-to-band tunneling of carriers which may occur at the gate-to-drain overlap region of the heavily doped drain under relatively high V_{DG} (drain in deep depletion) when the gate oxide is thin (<10nm)[2]. In the present case, N_{n+} ($\sim 10^{18}cm^{-3}$) and V_{DG} are not so high. Therefore a possible mechanism for the observed I_{GIDL} is the band-to-defect tunneling via interface states[5]. There can be a high density of defects at the gate-oxide/drain-Si(111) interface. Electron-hole pairs can be generated by tunneling of electrons trapped in the interface states into the (drain) conduction band under fairly high V_{DG}, and the generated holes may require thermal emission to be emitted into the valance band of Si depending on the energy level of the interface state (**Fig. 8**). The tunneled electrons collected by the drain constitute the I_{GIDL}. Thus the observed leakage current component in the subthreshold region could be due to

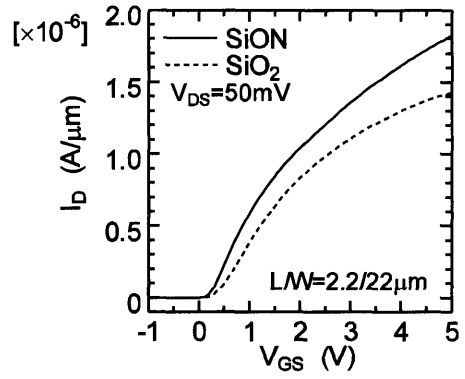

Fig. 6 Linear characteristics of the RC-MOSFETs with SiON and SiO_2 as the gate dielectric.

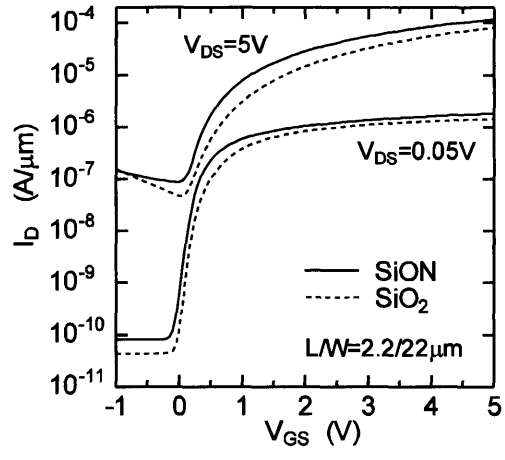

Fig. 7 Plots of I_D vs V_G of the RC-MOSFETs showing subthreshold characteristics.

the additional effect of gate overlapping the Si(111) surface of the drain. This is an experimentally observed drawback of the present RC structure. This current component could be reduced by having a shallower channel and a shorter gate electrode.

Saturation drain characteristics (I_D vs V_D) of the RC-MOSFET for V_G=0 to 5V are shown in **Fig. 9**. Higher on-state currents can be observed in the RC-MOSFET with SiON gate dielectric especially at higher gate voltages. Since the equivalent oxide thicknesses are the same, the increased drain current could be a result of an increase in the channel carrier mobility. **Figure 10** shows the variation of the field effect mobility, μ_{FE}, derived from the drain characteristics for small V_D.

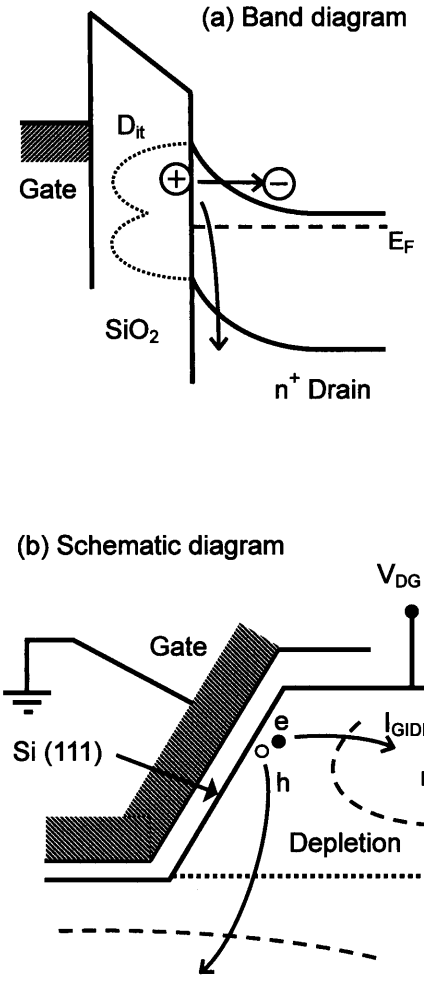

Fig. 8 Mechanism of band-to-defect tunneling of carriers via interface states, which results in I_{GIDL} in RC-MOSFET. (a) band diagram, (b) schematic diagram.

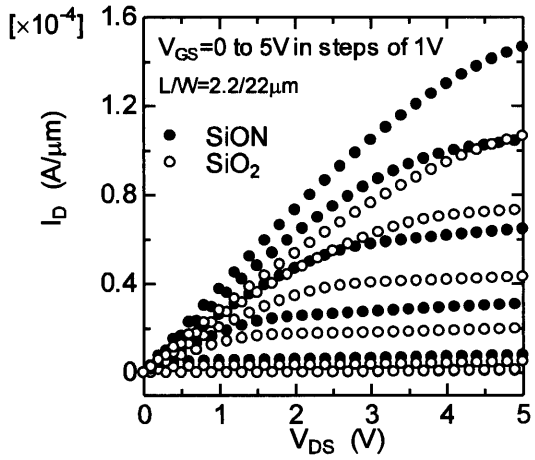

Fig. 9 Saturation I-V characteristics of the RC-MOSFET, for V_G from 0 to 5V in steps of 1V.

RC-MOSFET with SiON gate dielectric shows higher field effect mobility, μ_{FE}, compared with SiO_2 device (**Fig. 10**). It has been reported that high-field electron mobility with lightly nitrided oxides had improved over SiO_2 [6]. In contrast, peak electron mobility with SiON has shown reductions compared with SiO_2 when the interface N concentration increases above $\sim$ 0.5 atom% [2]. The mobility modulation in SiON under high effective fields has, however, not been well explained in the literature. Channel carrier mobility will be directly affected by charge trapping by interface states and carrier scattering due to trapped charges. In the planar SiON/Si and SiO_2/Si systems the mid-gap interface state densities were observed to be almost the same. However, SiON had lower fixed charge density and therefore the observed higher mobility could be partly due to reduced Coulomb scattering with less trapped charges in SiON. There is a possibility in the present SiO_2/Si system, where oxidation is by low temperature processing, that nitridation could lower the interface roughness and thereby reduce surface roughness scattering. Further, in the present structures, oxide/Si interface may be under stress due to non-planar nature. Oxide stress can cause structural damages in the underlying Si and could affect device performance. Since SiO_2 is generally under compressive stress and Si_3N_4 on Si is under tensile stress, SiON can have less or zero stress. The oxide stress may be reduced due to N incorporation in the bulk of the thin oxide, and it is possible that this suppresses any structural defect formation in Si inversion region thus leading to higher channel carrier mobility.

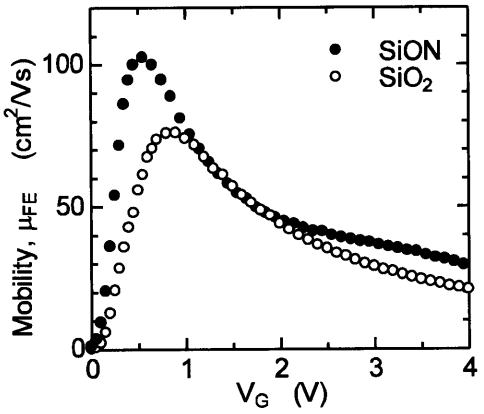

Fig. 10 Field effect mobility, μ_{FE}, of the channel electrons in RC-MOSFETs with SiON and SiO_2 gate dielectrics (V_D=0.05V).

It has also been suggested that acceptor like interface states located close to or inside the conduction band in the Si/SiO_2 system are markedly reduced by nitridation and the high field mobility reduction due to electron trapping by these interface states is greatly suppressed by gate oxide nitridation[7]. This could also be relevant to the present system as well.

In spite of the performance improvements due to nitridation of the gate oxide, the overall performance of the fabricated RC-MOSFETs is below the maximums reported for planar MOSFETs with similar channel lengths. Optimization of the device fabrication process, especially S/D formation, channel etching and gate oxynitride growth, is expected to bring about enhanced performance. Our experiments achieved channel etching down to L_{ch}=100nm, and 10nm channel lengths have been reported to be successfully formed by KOH wet etching. Therefore there is the possibility that the present RC-MOSFET fabrication process could be extended to ultra-short channel lengths and that nitridation induced improvements could be achieved at such short channel lengths as well.

4. Conclusions

RC-MOSFETs on a p on p^+ epi-layer were successfully fabricated by using anisotropic wet etching to etch the channel, solid phase diffusion to form the source and drain, and using plasma oxidation and nitridation to grow the gate SiON. The fabricated devices have dimensions of L/W=2.2μm/22μm, and gate dielectric thickness of 7nm. The S/D thickness was 0.55μm. Gate SiON was formed by N plasma nitridation of the pre-oxide which was also grown by plasma processing. Both the O plasma and the N plasma were generated by inductively coupled rf excitation. Plasma nitridation of the gate oxide resulted in improved breakdown strength. RC-MOSFETs with plasma grown gate SiON demonstrated higher on-state currents as a result of improved channel carrier mobility compared with devices with plasma grown SiO_2. Less fixed charged scattering, lower oxide stress related interface defects and probably lower near-conduction band interface state densities are considered to be possible causes for the higher channel carrier mobility in devices with plasma nitrided gate SiON. From the I-V characteristics a possible structure related subthreshold parasitic leakage current component was also identified. There is potential to scale the studied RC-MOSFET to shorter channel lengths and to achieve performance improvements by optimizing the device fabrication process.

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