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https://doi.org/10.15017/1516049

出版情報：九州大学大学院システム情報科学紀要. 9 (2), pp.67-72, 2004-09-24. 九州大学大学院システム情報科学研究院
バージョン：
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Simulated Characteristics of Deep-submicrometer Recessed Channel epi-MOSFETs

Rohana PERERA* , Akihiro IKEDA** and Yukinori KUROKI**

(Received June 10, 2004)

Abstract: Characteristics of ultra short channel length recessed channel n-MOSFETs on a p on p^+ epitaxial layer (RC epi-MOSFET) were simulated using the two dimensional device simulator MEDICI. The simulated recessed channel (RC) structure consists of thicker source/drain, zero source/drain junction depth and a lightly doped channel layer. Conventional short channel planar MOSFETs and RC-MOSFETs with uniformly doped substrate were also simulated for performance comparison. High field simulations were carried out using carrier energy balance equations while the single carrier drift-diffusion set of equations was used for low field simulations. Simulation results showed that the RC epi- structure has suppressed threshold voltage roll-off and lower subthreshold swing compared with planar and RC-MOSFETs with uniform substrate doping, without significant reduction in on-state current.

Keywords: Device simulation, MOSFET, Recessed channel, Epitaxial structure, Short channel effects

1. Introduction

Metal-oxide-semiconductor field effect transistors (MOSFETs) scaled down to deep-submicrometer gate lengths require shallow source/drain (S/D) junctions, higher and steeper doping profiles and thinner gate oxides to suppress short channel effects (SCEs)[1)-4)]. At sub 0.1μm channel lengths substrate doping needs to be in the order of $\sim 10^{18}\text{cm}^{-3}$ and such high doping levels lead to undesirably high threshold voltages and large junction capacitances thereby limiting the circuit speed[5)]. Performance degradation due to high resistance of the shallow S/D regions and leakage currents across heavily doped junctions are also limiting factors. The channel carrier mobility is also affected by increased impurity scattering. Formation of shallow S/Ds only a few tens of nm deep with high dopant concentrations and steep profiles, and the high cost of lithography for nano-scale patterning are also technological challenges.

To avoid the problems of high junction capacitance and degraded mobility encountered with heavy doping while maintaining better subthreshold (and on-state) characteristics non-uniform substrate doping profiles and non-conventional device structures have been adopted[3),4),6)]. One approach is the devices that have retrograded channel doping profiles -namely, delta doped (DD) MOSFET[6),7)] or the pulsed shaped doped MOSFET[5)]. This structure is reported to have suppressed SCEs without having high threshold voltage or degraded mobility. A structure with similar effects is the pocket implanted (PI) (or halo-doped) MOSFET, which is also reported to be fairly effective in suppressing SCEs[6),8)] but have degraded on-state currents due to high threshold voltages and lower mobility in the heavily doped pocket regions[8)]. Performance improvements in both the DD and PI MOSFETs depend on the DD/pocket profile control, and the fabrication of DD devices with steep doping profiles has been reported to be a complex process[7)]. Another approach is the silicon-on-insulator (SOI) structures[4)]. The thick buried oxide of the SOI devices, on which lie the S/D, dramatically reduces the junction capacitance; and the possibility to have a thin Si layer as the channel allows a low channel doping density. Yet another approach is the epitaxial (epi-) MOSFET[4)]. Epi-MOSFET also consists of an almost intrinsic epitaxial layer of Si on a heavily doped substrate layer. In both the SOI and epi- MOSFETs the S/D depths are limited by the thickness of the Si epi-layer, which is required to be very thin to suppress short channel effects, and hence, the increased S/D series resistance of these MOSFET structures significantly reduces the current drive and speed response. In order to have thick S/D and thus reduce the S/D resistance, elevated S/D[3),9)] or recessed channel SOI[10)] structures have been proposed.

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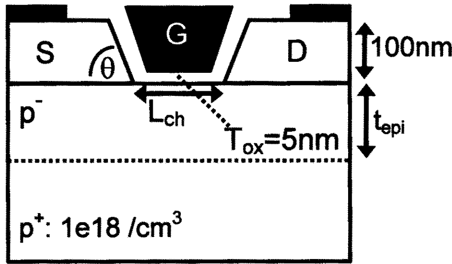

Fig. 1 Schematic cross-section of the recessed channel epi-MOSFET.

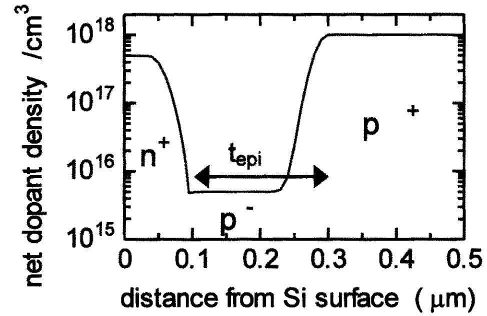

Fig. 2 Vertical doping profile of the RC epi-MOSFET.

The present work reports on a simulation study on a recessed channel deep submicrometer n-MOSFET on a p on p^+ epitaxial layer, devised to achieve better performance by suppressing short channel effects. Both the substrate and S/D engineering concepts are combined to have a retrograded channel impurity profile and elevated S/D with zero junction depth and thereby achieve better short channel effect suppression without increased S/D resistance, high junction capacitance or junction leakage, degraded mobility or very high threshold voltage. The proposed structure is non-planar and consists of S/D in the epi-layer, separated by a groove (a V-groove gate) so that the channel is at the bottom of the groove. This structure can be fabricated fairly simply by anistropic wet etching of Si by KOH solution to etch the V-shaped groove[11]. Simulation was carried out with the two dimensional device simulator MEDICI (ver. 2002.4.0 Synopsys, Inc., 2002) which is capable of simulating the behavior of deep submicrometer devices with arbitrary device geometry and non-planar surface topologies[12]. Simulation results show that the proposed structure can effectively suppress short channel effects without significant reduction in on-state current.

2. Device Structure and Simulation

Figure 1 shows the schematic cross-section of the recessed channel n-MOSFET simulated in this work. The angle θ was taken to be 54.7° following the exact value that would result from KOH etching (or to be 45° when the drain characteristics are simulated due to the constraint on number of grid points). The gate oxide thickness (T_{ox}) at the bottom of the groove was 5nm while the thickness on the side walls of the groove was taken to be 8.16nm considering the faster oxide growth rate (×1.6) on the heavily doped (111) oriented side walls. S/D thickness was 100nm, and was 75nm long at the top surface. The S/D doping density was uniform (N_D=5x10^{17}cm^{-3}) for a vertical distance of 35nm and then followed a hemi-Gaussian profile so that the metallurgical junction is at the level of groove bottom (**Fig.2**). In the lateral direction the S/D concentration was uniform. The p^+ substrate has a constant dopant density of N_{p+}=1x10^{18}cm^{-3} while the epi-layer also has a constant density of N_{p-}=5x10^{15}cm^{-3}. However, from p^+ region to p^- region, the dopant density varies following a hemi-Gaussian profile resulting in a transition region of ~ 75nm. The epilayer thickness at the channel, t_{epi}, is as indicated in **Fig.2**. The above dopant profiles were assumed in order to be fairly consistent with the profiles that would be found in the real device after the complete fabrication process.

The planar n-MOS structure considered for making comparisons with the RC structure is a conventional single S/D structure with a uniformly doped substrate (**Fig. 3**). T_{ox}=5nm, X_j=50nm and S/D length=150nm. The maximum S/D concentration was 5x10^{17}cm^{-3} and N_B=5x10^{15}cm^{-3}. The S/D dopant diffusion was taken into account and the lateral diffusion was represented by a hemi-Gaussian profile. The lateral doping profile just below the Si/SiO_2 interface and the vertical profile across S/D are shown in **Fig. 4**.

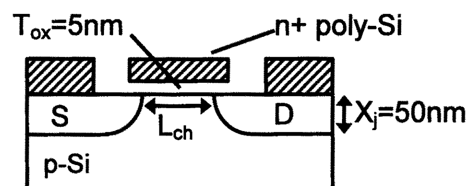

Fig. 3 Cross-sectional diagram of the planar n-MOSFET.

In every device structure the gate electrode was n^+ poly silicon; and the source, drain and substrate electrodes were assumed to be neutral contacts so that no uncertain resistances are added. The length of the simulated structure was 340 (or 300)nm + L_{ch} for RC devices and 300nm+L_{ch} for planar MOSFETs while all the structures had a (Si) depth of 700nm.

For simulation of low field characteristics (subthreshold characteristics, V_{th} and transconductance) the single carrier drift-diffusion set of equations were employed since at low bias and low current levels carrier heating is negligible. With these equations the mobility models used were a concentration dependant mobility model, an enhanced surface mobility model that takes into account phonon scattering, surface roughness scattering and charged impurity scattering, and a parallel field dependent mobility model. For simulation of drain characteristics, the electron and hole energy balance (EB) equations were used together with the drift-diffusion equations (the hydrodynamic model)[12] so that carrier heating in high and rapidly varying fields is taken into account. A carrier temperature based impact ionization model was also included, and the full energy balance equations consisted of transient effects and carrier cooling due to impact ionization. With the EB model a carrier temperature based mobility model was used to account for mobility effects due to high (parallel) fields while an empirical model which combines the effects of bulk Si and the Si-oxide interface (Lombardi surface mobility model) was used to model the bulk and inversion layer mobility (transverse field effects). For simplicity, simulations were carried out without including interface charges or traps.

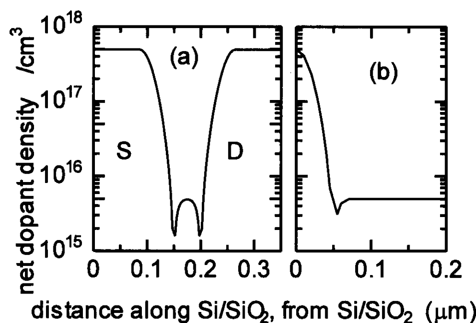

Fig. 4 Doping profiles of the planar n-MOSFET (L_{ch}=50nm, X_j=50nm). (a) lateral profile across S and D, (b) vertical profile across S/D.

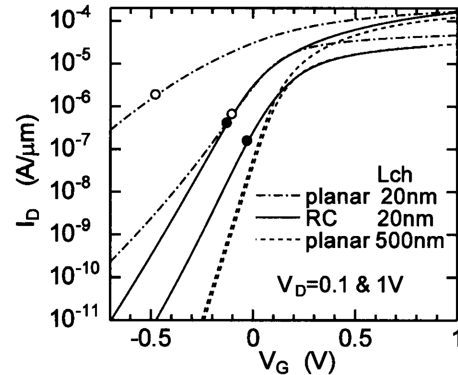

Fig. 5 Plots of drain current, I_D, vs gate voltage, V_G, of a planar and a RC-MOSFET with L_{ch}=20nm for V_D=0.1V and 1.0V. Also shown are the characteristics of a planar MOSFET with L_{ch}=500nm. Circles show V_{th} for each case.

3. Results and Discussion

Subthreshold characteristics of 20nm channel length planar and RC MOSFETs with uniform substrate doping (UD) (N_B=1x10^{15}cm^{-3}) simulated for the drain voltage V_D=0.1V and 1V are shown in **Fig. 5**. Also shown in the figure are the characteristics of a long channel (500nm) planar MOSFET.

As can be seen from the plots, the planar MOSFET with L_{ch}=20nm has unacceptably high subthreshold swing or (1/gradient), S, lower threshold voltage, V_{th}, and larger shift in V_{th} with V_D, indicating that short channel effects (SCE) are significant in this structure and that substrate doping level is too low and the S/D junction depth is too high to suppress SCEs at this ultra short channel length level. However the RC-MOSFET with the same low substrate doping level is observed to have better subthreshold characteristics. With the view of further improving the RC-MOSFET characteristics the effects of introducing a heavily doped substrate layer on the MOSFET parameters were analyzed.

Figures 6(a) and **6(b)** show the variations of the threshold voltage and subthreshold swing, respectively of the RC epi-MOSFET with the channel epi-layer thickness, t_{epi}. Plots are shown for the channel lengths of 50nm and 20nm and for the drain biases of 0.1V and 1.0V. **Figure 7** shows the variation of the maximum saturation transconductance, g_m, of the RC epi-MOSFET , with t_{epi}. In each graph the larger, unconnected symbols on the right

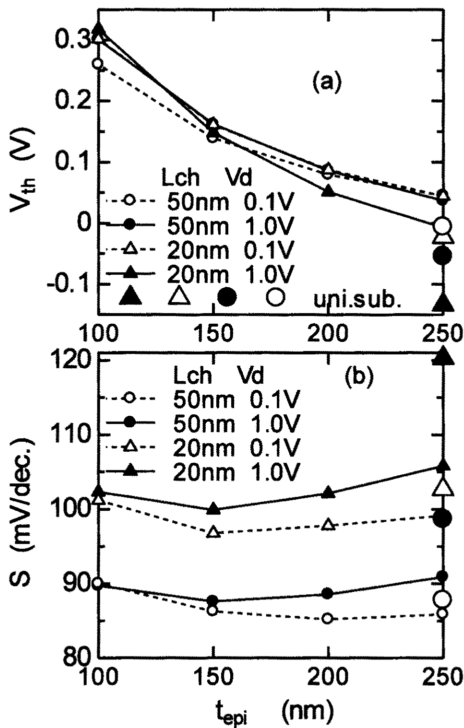

Fig. 6 Variation of (a) the threshold voltage, V_{th}, and (b) the subthreshold swing, S, of RC epi-MOSFETs, with the channel epi-layer thickness, t_{epi}.

vertical axis show the corresponding values for the uniformly doped substrate.

The V_{th} was evaluated from extrapolating $\sqrt{I_D}$ to zero on the V_G axis. Although the drain current of the RC epi-MOSFET may not follow the same I_D-V_G relationship as that of the planar MOSFET, this method turned out to be a consistent graphical method for the evaluation of V_{th} of the epi-MOSFET. As can be expected, V_{th} of the RC epi MOSFET increases with decreasing epilayer thickness. Subthreshold swing, S, shows a reduction in the epi structure compared with the devices with uniformly doped substrate, especially for the case of high drain voltages (**Fig. 6(b)**), suggesting that the drain field penetration into the source junction is significantly suppressed by the presence of the heavily doped substrate layer. When t_{epi} decreases from 250nm to 150nm S reduces further, though slowly, and then shows a small increase at t_{epi}=100nm, for which case the lightly doped layer thickness is ~ 25nm. The increase in S could partly be due to the increased depletion capacitance that will be present when the lightly doped layer is very thin[2),4)]. Similar behavior has been observed with planar epi-MOSFETs as well[4)].

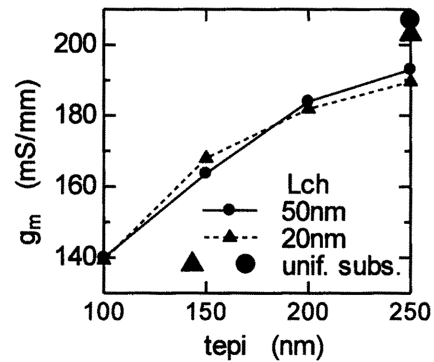

Fig. 7 Variation of the maximum saturation transconductance, g_m, (at V_D=1V) of 20nm and 50nm channel length RC epi-MOSFETs, with the channel epilayer thickness, t_{epi}.

Saturation transconductance of the RC epi-MOSFET shows degradation with decreasing epilayer thickness, t_{epi}, (**Fig.7**) which will lead to degraded on-state currents. This behavior could be due to the increased transverse field found with decreasing t_{epi}.

The above dependences of V_{th}, S and g_m on t_{epi} was used as a rough guideline for selecting an appropriate t_{epi} value for a device so that further analysis on epi-MOSFET characteristics could be made on a device with a fixed t_{epi}. Considering the observed mid V_{th} value, lower S and not too much degraded g_m, the epilayer thickness, t_{epi}, of 200nm (which corresponds to a very lightly doped ($5x10^{15}cm^{-3}$) layer of ~ 125nm) was selected for cross-analysis of RC epi-MOSFETs with different submicrometer channel lengths.

Figure 8 shows the conduction band (electron) potential, E_c/q, variation of the RC epi-MOSFET (t_{epi}=200nm, L_{ch}=50nm) under different bias conditions from fully-off to fully-on state. The lines correspond to gradually increasing vertical distances from the top surface of S/D up to the p^+ layer. The lines have been shifted left/right to show the potential barrier/slope clearly. No anomalous behavior is observed in these plots, and these diagrams illustrate the operation of the RC epi-MOSFET.

Figure 9 shows that V_{th} roll-off in the RC epi-MOSFETs with t_{epi}=200nm is well suppressed compared with uniformly doped substrate RC and planar MOSFETs. In the sub 0.1 μm channel range the RC epi-MOSFET shows the lowest S factor of the three device types (**Fig. 10**). Thus there is evidence that the RC epi structure has much better subthreshold characteristics compared with uniformly doped RC and planar MOSFETs.

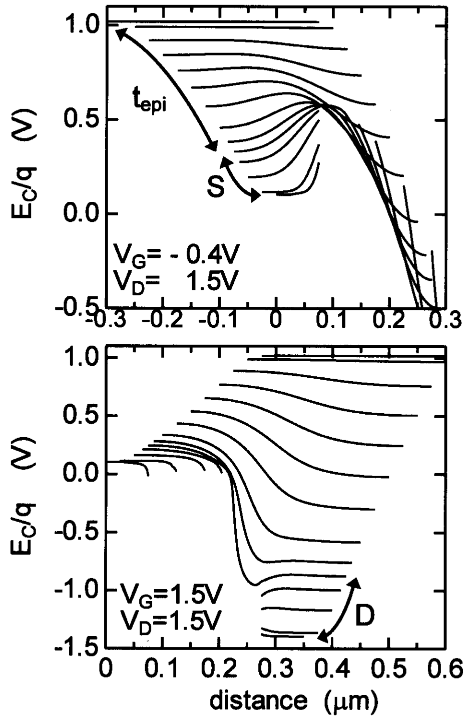

Fig. 8 Conduction band (electron) potential, E_c/q, diagrams of the RC epi-MOSFET (t_{epi}=200nm, L_{ch}=50nm) for different V_G and V_D biases.

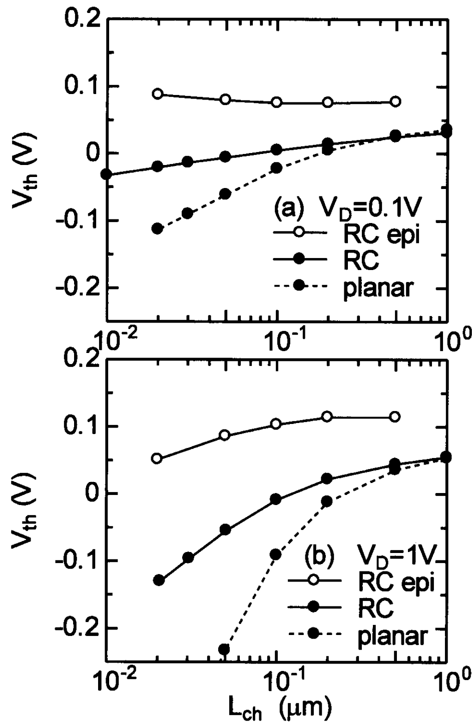

Fig. 9 Threshold voltage roll-off of RC epi-MOSFETs (t_{epi}=200nm), and RC and planar MOSFETs with uniformly doped substrate for (a) V_D=0.1V (b) V_D=1.0V.

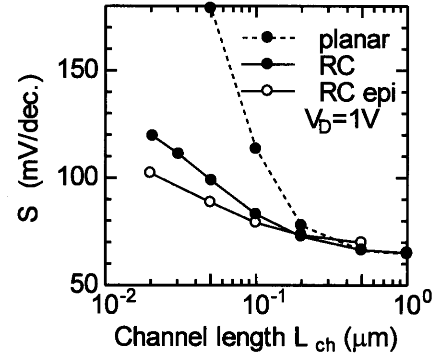

Fig. 10 Variation of subthreshold swing, S, with the channel length, L_{ch}, for RC epi-MOSFET (t_{epi}=200nm), and RC MOSFET and planar MOSFET with uniformly doped substrate at V_D=1V.

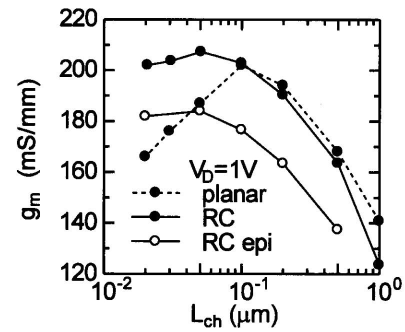

Fig. 11 Variation of the maximum saturation transconductance, g_m, of the RC epi-MOSFET, RC MOSFET with UD substrate and planar MOSFET with UD substrate at V_D=1V.

For all the channel lengths the g_m shows a lower value than those for the uniformly doped substrate case (**Fig.11**). This could partly be due to the increased transverse field in the epi-MOSFET. The saturation of g_m observed at channel lengths $\leq$ 50nm for both RC structures could be due to the fact that the effect of S/D resistance becomes significant at ultra short channel lengths as well as due to possible carrier velocity saturation with high lateral fields. In the case of the planar MOSFET the sudden fall in g_m for $L_{ch} \leq$ 100nm could be due to the additional effect of gate beginning to loose control over the drain current when V_D is fairly high (V_D=1V) as was also observed in subthreshold characteristics in **Fig. 5**.

The drain characteristics of 50nm channel length RC epi-MOSFET, and RC and planar MOSFETs with uniformly doped substrate are shown in **Fig. 12**, for the gate bias of 1V. The variations shown are

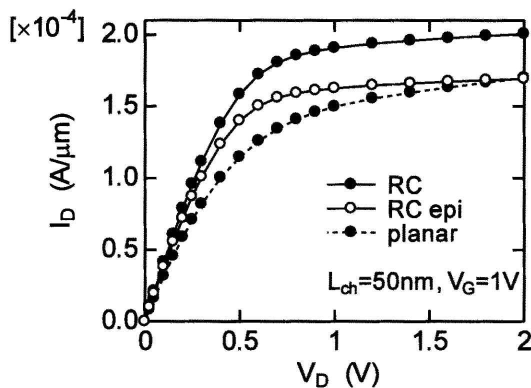

Fig. 12 Simulated drain characteristics (I_D vs V_D) of RC epi-MOSFET, and RC and planar MOSFETs with uniformly doped substrate for L_{ch}=50nm and V_G=1V.

expected to be highly accurate since the most appropriate models available in MEDICI, that account for carrier heating, velocity overshoot and impact ionization phenomena in ultrashort channel devices were employed for drain characteristics simulation. As can be expected, the saturation drain current of the RC epi-MOSFET is lower than its UD substrate counterpart. Although reduced, the I_{Dsat} value for the RC epi-MOSFET indicated in **Fig. 12** is close to that of the planar MOSFET. Since the V_{th} of the planar MOSFET is lower than that of the RC-structures, the difference in I_{ON} between the RC- and planar structures will be higher when the same gate drive (V_G-V_{th}) is considered. Further, it was observed that by decreasing the gate oxide thickness and increasing the S/D dopant concentration, g_m and I_{ON} of both RC structures could be significantly increased.

The observations made in this study and the reported effects of the epilayer on the planar MOSFETs indicate that the parameters of the present RC epi-MOSFET can be altered so that specifications for a particular application are met. The channel epilayer thickness, t_{epi}, can be further reduced to have much tighter control over SCEs and to have lower I_{OFF} at the expense of on-state current for low power applications; and S/D concentration may be increased to have higher g_m and I_{ON} for high performance applications while having acceptable subthreshold characteristics. Thus the present study provides a basis for optimizing the properties of the proposed RC epi-MOSFET.

4. Conclusions

A device simulation study was carried out on a deep submicrometer, recessed channel n-MOSFET structure on a p on p^+ epilayer. The simulation results show that the RC epi structure has suppressed short channel effects -lower V_{th} roll-off and lower subthreshold swing compared with RC MOSFETs and conventional planar MOSFETs with uniformly doped substrate, without on-state current being significantly affected. There is potential in the proposed structure to make modifications in the device parameters so as to meet application specifications.

Acknowledgements

R. Perera gratefully acknowledges a postgraduate scholarship from the Ministry of Education, Culture, Sports, Science and Technology of Japan.

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