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Bifurcation Behavior of a Power-Factor-Correction Boost Converter

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Abstract: The aim of this paper is to investigate the bifurcation behavior of the Power-Factor-Correction (PFC) boost converter under the conventional average-current-mode control. The converter is operated in continuous-conduction mode. Boost PFC converter is a nonlinear circuit due to the contribution of the multiplier and a large duty cycle variation that reveals the difficulty of analysis. Designers preferred to work in the direction toward putting some assumptions that reduced the system to be a linear model. Then, the stability problem could be solved and the regions of stability were determined. However, instability phenomena have been detected in the regions predicted to be stable by the prior linear PFC models. This fact makes us more susceptible to these linear models, and reflects the highly needs to consider the system by a nonlinear model. This forces us to investigate these problems and to develop new approaches. The bifurcation analysis performed by computer simulation packages reveals interesting effects of variation of some chosen parameters on the stability of the converter. The results are illustrated by time-domain waveforms and phase plane curves. Experiment results confirm the simulation results with a good matching. Such an analysis allows convenient detection of the unstable phenomena in the PFC circuit and so on, prediction of stability boundaries and facilitates the selection of parameters values to guarantee stable operation.

Keywords: Power factor correction, Boost converter, Average current mode control, Stability, Nonlinear phenomena, Period doubling bifurcation, Chaos

1. Introduction

Electronic equipment typically has the problem that a diode bridge-capacitor rectifier at the front end of the power circuit results in distorted input current waveform with high crest factor and harmonic content. Such a problem has prompted the development of Power Factor Correction (PFC) converter. There are many converter topologies that can be used as PFC converter. Among them, the commonly used one is the boost converter [1]. Many topologies for controlling PFC have been introduced. Average current mode control performs perfect power factor correction [2),3)]. The active PFC converter can be implemented using either the two-stage technique or the single-stage technique. The two-stage technique shown in **Fig.1** is the most commonly used technique due to its high power factor and especially for higher power applications. The active PFC stage is employed as the pre-regulator stage of the two-stage PFC to force the line current to track the line voltage. Second DC/DC converter is used for the output voltage regulation process. Generally, it is clear that many researches in modelling power electronics circuits have been directed toward arriving at a handy linear model that can be fitted in a frequency domain analysis with the limited validity being the price to pay [4]. The assumption of a very large capacitance in the output of the pre-regulator PFC stage was result in constant output voltage. Then, the feedback signal became time-invariant that reduced the nonlinear system to a linear system. Also, they replaced the input voltage by its rms value, neglecting the effect of its time varying. Under these assumptions, small-signal equivalent circuits were introduced [5)−10)]. Stability problems were explained on the basis of the linear system. However, there was no explanation for the instability waveforms and their frequencies on these linear models. Moreover, the huge output capacitance assumption is not acceptable in industry because it results in a high price and a large size from the viewpoint of high

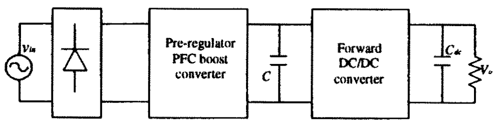

Fig.1 Conventional two-stage PFC block diagram.

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output capacitor voltage rating.

The price that must be paid is the inaccurate results and the disappearance for non-linear phenomena that can found in practical systems. Thus, it is very essential to investigate the active PFC with its non-linearity system and without any assumptions or limitation. Recently, there is more intention to two-stage PFC converters to improve the dynamic regulation and to decrease the bulk capacitance size. A new scheme for the two-stage PFC using series-switching post-regulator to improve the efficiency of the conventional two-stage (PFC + conventional DC/DC) converter was introduced [11], but it lacked for the stability investigation. It discussed the post-regulator stage depending on the prior conventional linear model although a small capacitance was used and the output voltage of the pre-regulator was time varying.

However, the stability of PFC converter operating at peak current mode control was studied depending on nonlinear models and unstable phenomena were detected [12),13)].

Recently, the PFC converter with average current mode control was discussed from the non-linearity point [14]. Only fast- scale instability was shown that had a small effect on the input power factor values. On the other hand, in this issue, new low frequency instability phenomena in a boost PFC converter have been detected [15)–19)]. These instability phenomena have a drastic effect on the input power factor values. Therefore, the most important questions now are, how to choose the optimum (minimum) value of the output capacitance C that assures the stability of the system, what kind of instability occur, which parameters affect in the instability, are prior linear models still valid or not to explain this instability, and lastly how to discuss the instability problem depending on nonlinear systems? First, let us define the used symbols as follows:-

P_{in}	:	rated input power.
f,f_s	:	line and switching frequency.
v_{in},v_g	:	input and rectified input voltage.
i_{in},i_l	:	input and inductor current.
v_c,v_{vea}	:	output and feedback voltage.
v_{ff}	:	feed-forward voltage.
$\hat{v}_c$	:	small-signal output voltage.
$\hat{v}_{vea}$	:	small-signal feedback voltage.
V,V_{vea}	:	input and feedback DC voltage.
L,C,R	:	inductor, output capacitor,
	:	and output load values.
R_{vi}, R_{vd}	:	feedback divider resistors.
R_{vf},C_{vf}	:	feedback resistor & capacitor.

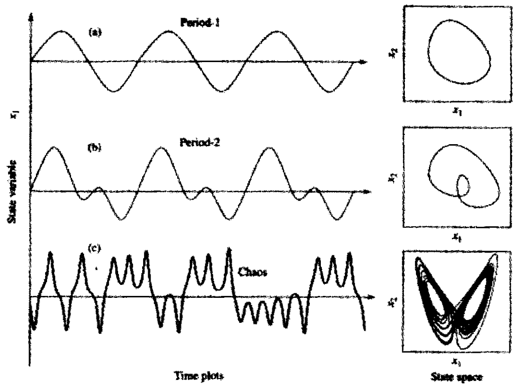


Fig.2 The appearance of period-1, period-2, and chaos waveforms in the time domain and in state space, for a system of order greater than 3 [20].

G_{vea}, G_t	:	feedback & total gain.
R_{vac}	:	programming resistance.
R_{mo}, R_s	:	multiplier & sense resistance.
d, $\acute{d}$	:	on and off time duty cycle.
V_{ref}	:	reference voltage.

2. Stability Definition

The definition of stability is different from one application to another. Thus, the main purpose of this paper is to examine the stability of boost PFC circuit with average current mode control from the bifurcation perspective. PFC stability is interpreted as a condition in which the operation of the system is the expected periodic regime. All those subharmonic, quasi-periodic, period doubling and chaotic operation are considered as unstable operation, being undesirable and should be avoided. Therefore, a periodic operation with line frequency for the input current and double line frequency for the output voltage ripple is the stable operation. All other regimes result in unstable operation (unexpected operation). Also, a clear definition for stability of periodic systems is reported in [20]. Suppose a nonlinear dynamical system has a periodic operation in the time domain, corresponding to the state-space trajectory that shows a single loop. When some parameter is varied, the waveform can change to the type shown in **Fig.2**(b), which has twice the period of the earlier periodic waveform. One interesting possibility opens up in systems of order 3 or greater: bounded aperiodic orbits, as shown in **Fig.2**(c). In such a case the system state remains bounded within a definite volume in the state space, but the same state never repeats. In every loop through the state space the state traverses a new trajectory. This situation is called chaos.

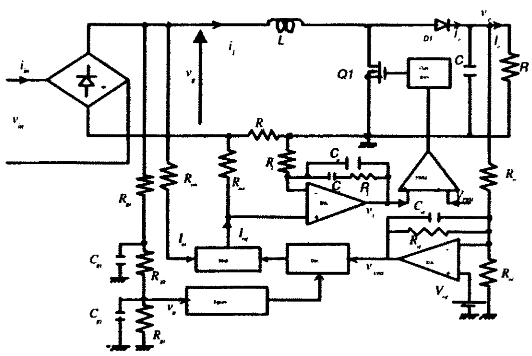


Fig.3 Boost PFC converter with average-current-mode control circuit

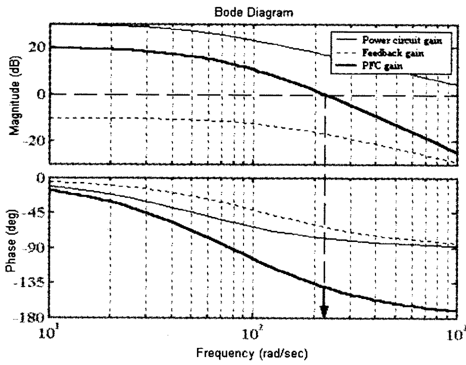


Fig.4 PFC Gain transfer function (unstable case) appears stable according to the prior conventional linear model.

3. Conventional Linear Methods

The most concern is to determine the PFC system stability. Here, the PFC pre-regulator with resistive load will be examined by the prior conventional linear method to prove its invalidity. **Figure 3** shows the boost PFC converter with average current mode control circuit. Stability of this circuit was explained by the prior researches depend on a simple linear model. They assumed a huge capacitance at the output terminal, replaced the time-varying input voltage with its rms value to ignore the nonlinear terms, and derived a small-signal equivalent circuit.

In the small-signal equivalent circuit based analysis and control system design for PFC converters, the nonlinear system is linearized around an operating point and the derived equivalent circuit is valid only for small deviations from that operating point. Therefore, it has a shortcoming to apply to PFC circuit with the large variation in the input voltage. Results obtained in prior design regimes [5)6)8)] showed that the total transfer function for the boost PFC converter with resistive load is as follows:

1) The converter power-stage transfer function to the feedback voltage was:

$$\frac{\hat{v}_c}{\hat{v}_{vea}} = \frac{V}{\sqrt{KV_{vea}R}}\frac{R}{2+sCR} \tag{1}$$

2) The feedback voltage to the output capacitance voltage function (Feedback equation) was:

$$\frac{\hat{v}_{vea}}{\hat{v}_c} = -\frac{R_{vf}/R_{vi}}{1+sC_{vf}R_{vf}} \tag{2}$$

Then, the total system transfer function was:

$$G_t = -\frac{\frac{VR_{vf}R/R_{vi}}{\sqrt{KV_{vea}R}}}{(2+sCR)(1+sC_{vf}R_{vf})} \tag{3}$$

Where

$$K = \frac{R_{mo}/R_s}{V_{ff}^2 R_{vac}} \tag{4}$$

K could be assumed a constant. From equation (3), it is clear that this system is stable for all cases and conditions. The PFC circuit parameters are tested at 50% load first by these equations (1)-(4) to examine the invalidity of this conventional linear model. A phase margin of +40 degrees is resulted as shown in **Fig.4**. This assures the system stability; however, this test point is experimentally unstable as will be shown later in the following sections. Therefore, it is cleared that these linear model is not valid because it cannot detect the real nonlinear phenomena and appears it as stable. Therefore, PFC circuit must be studied from the non-linearity as point of view.

4. Two-Stage PFC

A two-stage PFC consists of a pre-regulator boost PFC stage and a forward DC/DC converter. The boost PFC uses the average current mode control with UC 3854A [21)]. The conventional voltage mode control is used for the forward DC/DC converter. Test circuit conditions are 70-120 ac volt/60 Hz input, 180 dc volt at pre-regulated boost PFC output, 48 V / 2A at the forward converter output. The switching frequency for the two stages is 100 kHz. Circuit parameters are selected according to the Unitrode application note [5)21)]. The pre-regulator

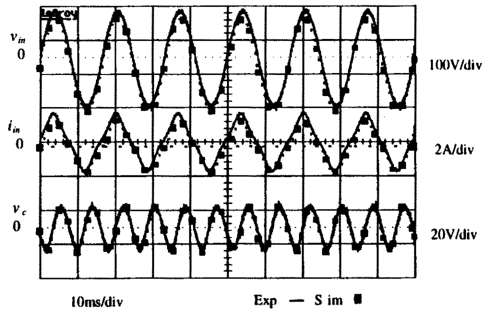


Fig.5 Response of input voltage, input current, and output voltage ripple in stable case. At C = 60 μF, C_{vf} =47 nF & full load two-stage PFC. (PF=0.98).

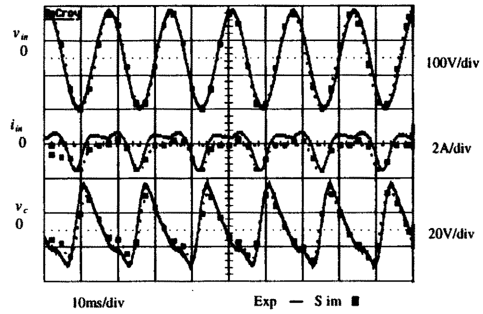


Fig.6 Response of input voltage, input current, and output voltage ripple in unstable case. At C = 60 μF, C_{vf} =47 nF & 50% load two-stage PFC. (PF=0.67).

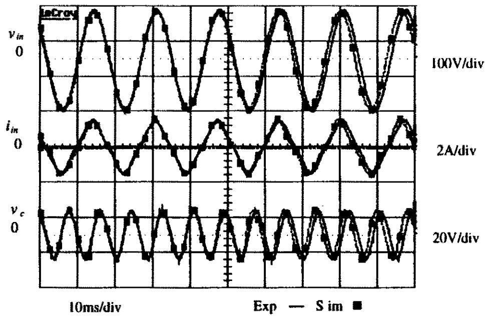


Fig.7 Response of input voltage, input current, and output voltage ripple in stable case. At C = 60 μF, C_{vf}=47nF & full load PFC.

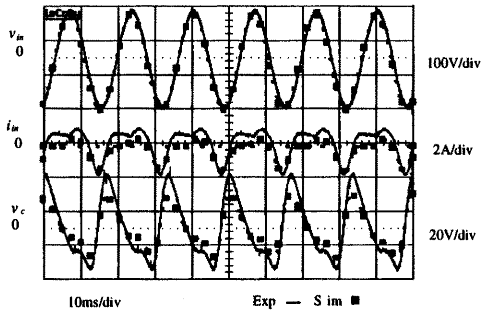


Fig.8 Response of input voltage, input current, and output voltage ripple in unstable case. At C = 60 μF, C_{vf} = 47nF & 50% load PFC.

boost PFC output capacitor C and the feed back capacitor C_{vf} are varied from small to large values to examine the stability of the system. The stability of the system is examined for all loads (from full load to very light load). Results are summarized in **Fig.5** for stable case where the input current and the input voltage are sinusoidal and emphasized; also the output voltage ripple is sinusoidal with double input line frequency. Good matching between simulation and experiment is obtained. Although this operation point has heavy loads and a relatively small output capacitance, a very high power factor (0.98) is obtained. On the other hand, **Fig.6** shows the instability phenomenon with the same test conditions as the above stable case with decreasing the load current only. The input current becomes asymmetrical (PF =0.67) and the output voltage ripple v_c changes its shape and frequency with increasing its amplitude. Thus, the load has a major effect on the PFC stability, and as the load becomes lighter, the system goes toward instability. However, the instability points do not depend only on the load conditions, but also on output capacitance C and feedback capacitance C_{vf}. This examination guides us to new instability phenomena that must be made clear or at least their region must be determined to be avoided.

Now, the important question is (what is the main cause of this instability? Is the pre-regulator power-factor-correction converter itself or the effect of the second stage ,forward DC/DC converter, on the pre-regulator PFC converter?) Therefore, the operation of the pre-regulator alone must be checked under the same condition as the two-stage case.

5. Pre-Regulator Boost PFC

The pre-regulator circuit is tested experimentally and verified by simulation with variable resistive loads under the same conditions of output capacitance and the feedback capacitance as the two-stage case. **Figure7** shows the stable case with the full load and the low output capacitance. The instability phenomenon is shown in **Fig.8**. This selected parameters for **Fig.8** is the same tested point by the linear model that shown as stable (**Fig.4**) that clears the invalidity of the prior linear model.

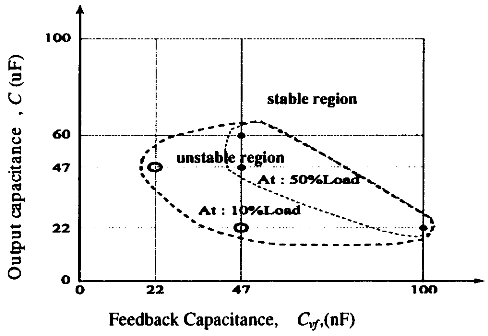


Fig.9 Estimated PFC instability map at different loads.

Figure9 shows the instability map. It is clear that the instability area increases as the load decreases.

It is evident that there is a light enhancement of the second stage on the PFC system instability. Therefore, it can be summarized that the cause of instability is the pre-regulator converter. Therefore, in any conventional or new two-stage PFC topology that uses a boost PFC circuit as the first stage, the above-mentioned instability phenomena can occur. Also, it is cleared that a good designed PFC with a very good power factor near unity (0.98) at full load can move to the unstable region by only lessen its load to the 50% and operate with a worse power factor than the diode bridge-capacitor case (0.67). Therefore, this forces us to investigate these phenomena in details to understanding its dynamics and determines its region and effected parameters.

6. PFC Instability Phenomena

Although studying the instability phenomena have some inherent difficulties, it is very important to investigate the dynamic behavior of PFC converters at the instant of instability phenomena. The stable operation of the boost PFC converter is a periodic input current with the line frequency and a periodic output voltage ripple with double line frequency. Then, periodic waveform reports the stable operation. However, when some parameter is varied, the waveform can change to have twice the period of the earlier periodic waveform. This is called period-doubling (period-2) bifurcation and as the load is lessened again, the period-doubling bifurcation moves to chaos. Chaos is a bounded system with random waveforms and is characterized by non-repeating waveforms and extreme sensitivity to the initial conditions. These phenomena are detected in boost PFC operation when the load is moved towards light loads as shown in **Fig.10**. In this example, the output capacitance ($C = 47\ \mu$F)

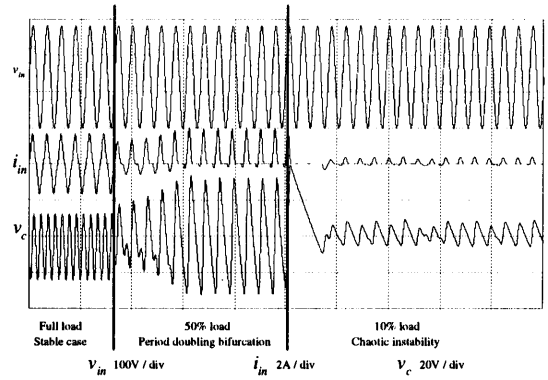
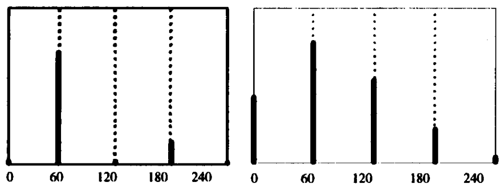


Fig.10 The response of the input voltage, input current, and the output voltage ripple at $C = 47\ \mu$F and $C_{vf} = 47\ n$F when the load is changed from 100% load (stable case) to 50% load (period doubling bifurcation) then to 10% load (chaotic instability) to explain the various operation cases (Simulation result).



(a) Stable case. (b) Unstable case

Fig.11 The harmonic components of the line current.

and the feedback capacitance ($C_{vf} = 47\ n$F) were chosen.

First, the operation is stable at full load; the input current is periodic at the line voltage frequency and the output voltage ripple is periodic at the double line frequency (the expected regime). The power factor is very high (0.98). As the load is changed to 50% load, the operation moves to be unstable; the input current move to be asymmetrical and the output ripple, v_c increased and became periodic with the double period in stable case. This is period doubling bifurcation instability. The important point that is highlight for industrial view is the low result power factor (lessens to 0.67) that means that the PFC converter operation is broken. The harmonic component is recorded in **Fig.11**(a) for full load and in **Fig.11**(b) at 50%load. It is clear that at stable case, only the fundamental and a low percentage of the third harmonic component are found. On the other hand at period doubling bifurcation the second harmonic is appeared clearly with a very high percentage due to the asymmetry in the line current. Also a dc component and some low per-

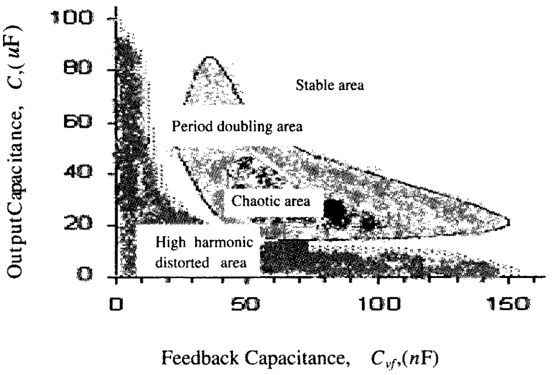


Fig.12 Estimated instability map at 10% load.

centages of high harmonic components are found. All these harmonics and especially the second harmonic cause the low power factor. In conclusion, as the load is decreased, we can expect unstable phenomena. A chaotic phenomenon is the most common known unstable phenomena in DC/DC converters [20]. Here, the boost AC/DC PFC converter has also chaotic operation at some specific parameters. Chaotic phenomenon appears after the period-doubling (Period-2) phenomenon when the load is lessened toward light load (10% load), a random operation is appeared and the input current and output voltage have bounded aperiodic waveforms as shown in **Fig.10**.

The known equations for any boost PFC circuit are:

$$\frac{di_L(t)}{dt} = d\frac{v_{in}(t)}{L} + \acute{d}\frac{v_{in}(t) - v_c(t)}{L} \quad (5)$$

$$\frac{dv_c(t)}{dt} = -d\frac{v_c(t)}{RC} + \acute{d}\frac{Ri_L(t) - v_c(t)}{RC} \quad (6)$$

The control equation that establishes the sinusoidal current is:

$$i_{in}(t) = \frac{|v_{in}|}{k} v_{vea} \quad (7)$$

The equation that describes the feedback loop is:

$$v_{vea}(t) = f(v_c(t)) = G_{vea}(v_c - V_{ref}) \quad (8)$$

Prior linear analysis methods assume the output voltage to be constant (dc value only). This is not true, as equation (8) explains that the output voltage is time varying and then the feedback voltage varies in time. Thus, the analysis must deal with these equations without any assumptions. (This summarizes that the output ripple of the voltage error amplifier in feedback process is a major contribution to the input line current.

On the other hand, the most important point for industrial is to determine the instability area for each phenomenon. **Figure12** shows the instability map at 10% load. Chaos instability area is centered at some specific area. Period doubling bifurcation area is located around chaotic area. This boundary is sensitive and changed with load. Stable area is located out of period doubling phenomena. The low parameters (very low output capacitance and very low feedback capacitance) area is called high harmonic distorted area. It is stable area but it has high voltage ripple and high input current distortion. Therefore, it is not practical and cannot use for industrial operation.

Here, let us try to explain how to choose one point for stable operation in brief. For a 100 watt, 100 input voltage, 60 Hz, 180 output dc voltage, and 100 KHz switching frequency. The output capacitor can be chosen for many requirements such as hold-up time or output voltage ripple values. Also, the feedback capacitor can be chosen depending on the required response of the PFC system. Choosing 100nF for the feedback capacitor. As it is explained that the PFC converter become more susceptible to instability at light loads. Therefore, the candidate value for output capacitor must be chosen at light loads. From the instability map at light load (10% load) in **Fig.12**, 50 μF or more can achieve the PFC system stability.

7. Phase Plane Curves

The experimental results assure the simulation result and we can detect the same two unstable phenomena experimentally. The phaseplane curves (lissajous curves) between the output voltage ripple on the vertical axis and input current on the horizontal axis can explain these phenomena easily. The stable, period-doubling bifurcation, and chaos can be observed from these planes. **Figure13** shows the phase plane for the stable case at full load and same parameters (output capacitance $C = 47$ μF and feedback capacitance $C_{vf} = 47$ nf). The phase plane has two equal and symmetrical loops. Then stable operation establishes two symmetrical and equal cycles. On the other hand, **Fig.14** shows the period-doubling bifurcation case at 50% load. It is clear the asymmetrical case where one loop is different than the other loop. This proves the same simulation result and clears the asymmetry case by using the phase plane. Also, it is shown that the output ripple voltage is increased in case of period doubling

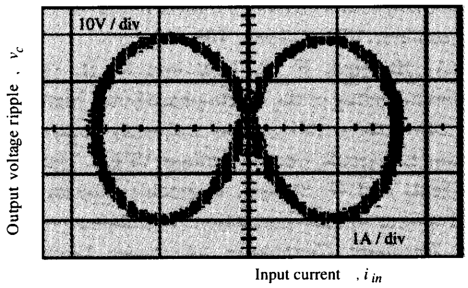


Fig.13 Phase plane trajectories for stable operation from experimental results.

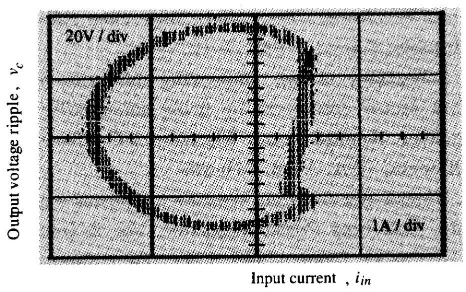


Fig.14 Phase plane trajectories for period doubling bifurcation from experimental results.

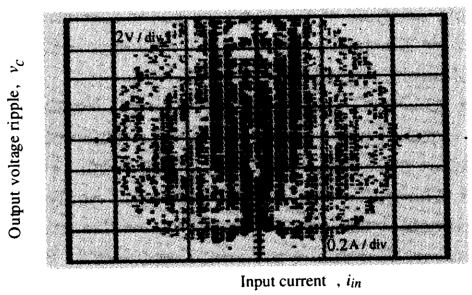


Fig.15 Phase plane trajectories for chaotic operation from experimental results.

bifurcation instability. Chaos case has random operation that means many points and many different loops as appears in **Fig.15** at 10% Load. **Figure16** shows another different phase plane shape for the same chaotic point. This proves the bounded aperiodic regime and sensitivity of chaos phenomena.

It is known that chaotic phenomena are sensitive to the parameter changing. **Figure17** shows one case of experimental operation when the load is 20% and the operation is stable. This point seems to be the borderline between the stable and unstable operation. With decreasing the load to 18% only (2% change), the system moves to the unstable operation. The output ripple voltage increased drastically and the two loops changed to multi loops as

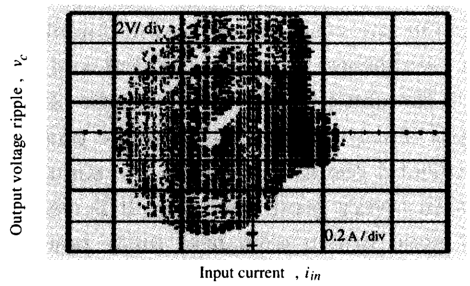


Fig.16 Another shape of chaos instability of **Fig.15** at the same parameters.

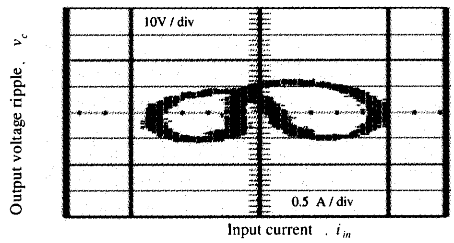


Fig.17 Stable operation at 20% load.

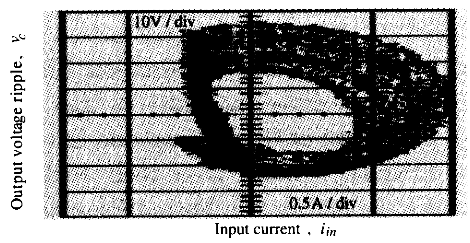


Fig.18 Unstable operation when a small load change is applied to **Fig.17** (from 20% to 18% load).

shown in **Fig.18**. These experimental results assure the simulation results and highlight novel unstable phenomena in PFC converter with average current mode control. Also, it is clear the effect of the feedback control that was assumed to be constant in the previous researches.

8. Conclusion

The instability of the pre-regulator and the two-stage PFC is investigated experimentally. Simulation has been performed to verify the experimental results with a very good agreement. New instability phenomena have been detected in the stable region obtained by prior linear models. Two new unstable phenomena in boost PFC converter with average current control are detected: Period-doubling bifurcation and chaos. Phase plane trajectory curves are introduced to clarify the stable, doubling-period bifurcation and chaos phenomena. Stable case establishes symmetrical and equal two loops in the phase plane. On the other hand, period-doubling bifurcation establishes two asymmetrical and different loops in the phase plane. Then, chaotic phenomena establish multi different loops in the phase plane. Experimental results agree with the simulation results with a very good matching. It is cleared that a very good design with near unity power factor at full load can move to be unstable at 50% load and its power factor lessen to be worse than conventional passive filters. Results highlight that the feedback output voltage ripple is a major contribution to the input current. This contribution results in the nonlinear system that established these instability phenomena. Finally, the results recommend to deal with the nonlinear systems rather than to reduce it to a linear system and to ignore the nonlinear phenomena found in this issue. Experimental results prove the simulation results with a very good matching.

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