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LC Clamp Circuit for Fast-Response VRM Requirements

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Abstract: In this paper a new fast-response voltage regulator module (VRM) design is presented that will meet the requirements and features of the new generation of microprocessors and digital systems. It is able to produce high slew rate of load current and capability to keep constant the output voltage in case of severe load changes. The proposed fast-response, LC clamp topology is theoretically lossless and is able to produce high slew rate of output current. It is low cost and easy to implement with simple control scheme. This is modified from a basic buck topology by replacing the output inductor with two magnetically coupled inductors in different inductance value. The inductor with small inductance will take over the output inductor during step-up load transient. It speeds up the output current slew rate and reduces the output voltage drop during step-up load transient. The additional capacitor, which is connected in parallel to the coupled inductor, will suppress the over-shoot of output voltage during the step-down load transition. In steady state, the inductor with large inductance takes over the output inductor and keeps the substantially small ripple current. The design, simulation and experimental results are presented to verify the proposed topology.

Keywords: Fast-response, LC clamp, Voltage regulator module, DC-DC converter, Current amlification, Current absorption

1. Introduction

1.1 Motivation

The switching voltage regulators known to be an efficient type of DC-DC converter are used to provide stable voltage sources for electronics systems, particularly needed for low voltage devices. Voltage regulator Modules (VRMs) for microprocessors are subject to ever more stringent performance requirements. One trend is to operate at higher currents e.g.,30 100A or more. Another trend is to turn on and off different parts of the microprocessor in each cycle in order to conserve power. This requires that the voltage regulator react very quickly to changes in the load, e.g., several nanoseconds to transition from the minimum to the maximum load or vise versa. In addition to these specific trends, the voltage regulator module is place close to the microprocessor in order to reduce the parasitic capacitance, resistance and inductance in the connecting lines and avoid the current losses. However, in order to place the voltage regulator close to the microprocessor, the voltage regulator needs to be small. Also high efficiency is generally desirable in order to avoid thermal overload at high load. These trends impose severe issues to the design of voltage regulator modules for modern microprocessors.

1.2 Review of Existing Solutions

The basic or synchronous buck converter topology shown in **Fig.1** has received great attention in VRMs for microprocessors in recent years due to their high efficiency. The transient waveforms at VRM output voltage, subject to the fast load change are in **Fig.2**. These waveforms show that the deviation at the output voltage due to the par-

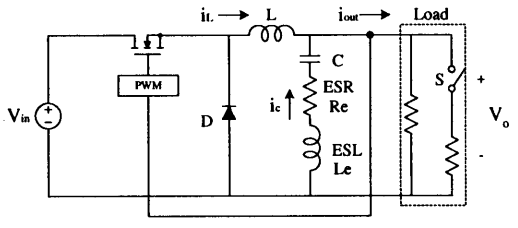

Fig.1 Conventional buck topology.

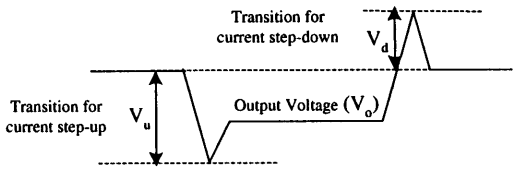

Fig.2 Wave forms at sudden load change.

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asitic elements of the circuit. Generally, during the load transient output current iout is partially supplied by the VRM output filter capacitor C, until the inductor current i_L reaches the load current iout. The capacitor current i_C shows a pulse that strongly affects output voltage (V_o) due to the Effective Series Resistance (ESR) and Effective Series Inductance (ESL) of the output capacitor[1]. Large number of high quality capacitors in parallel are needed to meet the future requirements, it is impractical due to limited space and link impedances [2]. Therefore, power supply requirement for future processors are very hard to meet with the conventional buck topologies.

Many researches have been introduced, various modifications to the basic buck topology to address the above challenging trends [1)–9)]. The simple way to improve the transient response of VRM is decreasing their output filter inductance. The trade off for this solution is a lower efficiency due to a need for a higher switching frequency, which is not acceptable. It is possible to parallel several converters and each converter has a relatively large output inductance. This parallel converter approach can flexibly increase output current slew rate by increasing the number of parallel converters. Interleaving parallel converter [10),11)] is one special form of parallel converter configuration, which produces equivalent small output inductance. This approach can help solve the higher ripple voltage by using complicated control circuit. It gives good performance during transient condition, however the steady state performance is still not satisfactory due to higher losses. To overcome the above draw backs the LC clamp circuit with current amplification and absorption techniques is proposed. The benefit obtained from the proposed topology is less output energy storage capacitance for achieving the same amplitude of transient response as with conventional voltage regulator module.

2. Proposed Solution

2.1 Circuit Description

The proposed converter consists of following functional blocks as shown in **Fig.3**. Switching converter block uses a basic synchronize buck topology and the LC clamp circuit block consists of an inductor, a capacitor, and the two MOSFETs.

2.2 Circuit Operations

Figure.4 shows complete circuit operations of the proposed converter and **Fig.5** shows essential

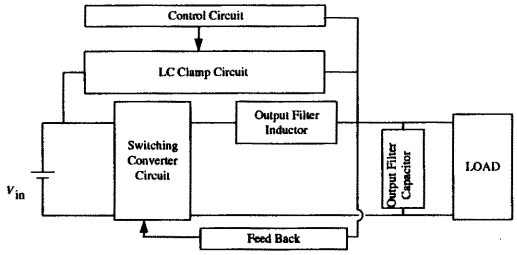


Fig.3 Functional block diagrams of the proposed converter circuit.

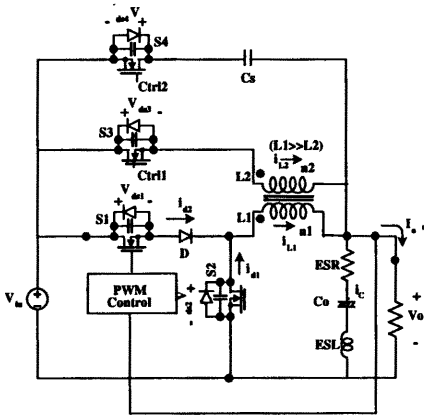


Fig.4 Complete proposed converter circuit

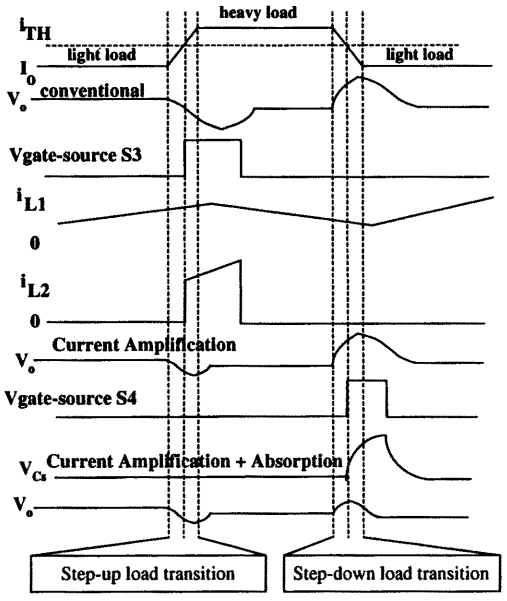


Fig.5 Key waveforms during fast load change.

key waveforms of the converter circuit. The two switches S3 and S4 perform the duties of current amplification and absorption during the step load transitions. The diode D prevents the reverse current flow during step-up load transition, when switch S3 is activated.

2.3 Circuit Analysis

As shown in **Fig.5**, the switch S3 is only activate during the step-up load transition and switch S4 is only activate during step-down load transition. The current amplification and absorption is occurred according to the switch actions of S3 and S4 in the LC clamp circuit.

2.3.1 Current Amplification

When the load current (Io) change suddenly from light to heavy, the output voltage (V_o), drops below a certain reference level, switch S3 is turned on by the control signal (Ctrl1). There are two possible states of the main switch (S1) at this transition. **Figure.6** shows the topological states of simplified circuit during the step-up load transition.

State1: Switch S1 ON, S3 ON; **Fig.6(a)** Shows the state1. According to the equation 5, diode D is reverse bias, and only small inductor L2 is conducting. Equivalent circuit is shown in **Fig.6(b)**. State2:Switch S1 OFF, S3 ON; **Fig.6(c)** shows the state2. According to the equation 5, resulting equivalent circuit is same as **Fig.6(b)** and only inductor L2 is conducting. From **Fig.6(a)**, following equations can be written;

$$V_{L2} = (V_{in} - V_o) \tag{1}$$

$$V_{L1} = \frac{n_1}{n_2}(V_{in} - V_o) \tag{2}$$

$$V_{L1} > V_{L2}(n_1 > n_2) \tag{3}$$

$$V_{L1} = V_D - V \tag{4}$$

$$V_D > V_{in} \tag{5}$$

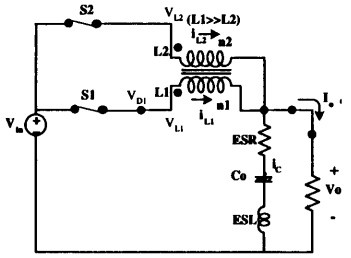
As a results of analysis, the small inductor $L_2(<< L_1)$ takes over the output inductor of the converter. High current through the small inductor L_2 will increase the load current slew rate and reduce the under-shoot at step-up load transition. The general expression for the output voltage drop and load current slew rate can be written as in equations (6) and (7).

$$\Delta V_o = \frac{1}{C_o}\int (i_o - i_{inductor})dt \tag{6}$$

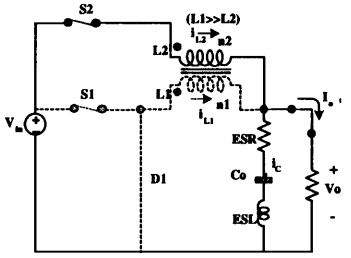
$$\tau = \left.\frac{di}{dt}\right|_{step-up} = \frac{V_{in} - V_o}{L_{inductor}} \tag{7}$$

Using the above equations following expressions can be derived for both cases of conventional and proposed topologies.

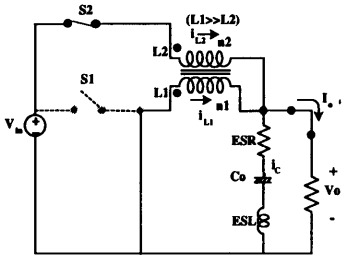
$$\Delta V_o(conventional) = \frac{1}{C_o}\int (i_o - i_{L1})dt \tag{8}$$



(a) Circuit at state1



(b) Equivalent circuit after analysis



(c) Circuit at state2

Fig.6 Simplified circuit diagram during step-up load transition.

$$\Delta V_o(proposed) = \frac{1}{C_o}\int (i_o - \frac{n_1}{n_2} i_{L1})dt \qquad (9)$$

$n1 >> n2$, therefore;

$$\Delta V_o(conventional) > \Delta V_o(proposed) \qquad (10)$$

Derived condition (10) shows that, the output voltage drop at the step-up load transition is reduced by the current amplification method.

$$\tau(conventional) = \left.\frac{di}{dt}\right|_{step-up} = \frac{V_{in} - V_o}{L_{L1}} \qquad (11)$$

$$\tau(proposed) = \left.\frac{di}{dt}\right|_{step-up} = \frac{V_{in} - V_o}{L_{L2}} \qquad (12)$$

Using equations (11) and (12), expression (13) can be written;

$$\tau(proposed) = \frac{L_{L1}}{L_{L2}}\tau(conventional) \qquad (13)$$

where $L_L1 >> L_L2$ The expression (13) shows that the load current slew rate is increased with new topology.

2.3.2 Current Absorption

When load is remove or sudden change from a switching mode power supply with a LC low-pass output filter, the control loop is stop the switching action so, no more energy is taken from the source. The energy that is stored in the output filter inductor is dumped into the out capacitor causing a voltage overshoot. In our proposed model, the capacitor Cs will charge up to $(V_{in} - V_o)$ through the body diode of the switch S4 soon after the power on of the converter. When the load is changed from heavy to light, the output voltage (Vo) over the certain reference level, the switch S4 is turned on by control signal Ctrl2, and excess current flows towards the capacitor Cs from the converter output side. This process suppresses the over-shoot at the step-down load transition. Equation (14) gives the relation of output voltage over-shoot (ΔV_d) and capacitor voltage (V_{Cs}) with considering the ESR.

$$V_{Cs}(s) = \frac{1}{sC_s}\frac{1}{\frac{1}{sC} + ESR}\Delta V_d(s) \qquad (14)$$

2.3.3 Steady state operation

In steady state, switch S3 is always off. The large inductor L2 takes over the output inductor and keeps the substantially small-ripple current.

2.4 Control Scheme

The control scheme shown in **Fig.7**, keeps constant output voltage in case of severe load changes. It can be explained as follows: when the VRM output voltage drops below a certain reference level (Vref1), switch S2 is turned-on by pulse (Ctrl1). When the VRM output voltage drops higher than the certain reference level (Vref3), switch S3 is turned-on by pulse (Ctrl2).

Table1 Specification and circuit parameters of the proposed converter

Symbol	Description	Value
C_o	Output Capacitor	$330\mu F$
ESR	ESR of Output Capacitor	$130m\Omega$
ESL	ESL of Output Capacitor	$10nH$
	CoupledInductor	
L1	Large Inductor	$6.3\mu H$
L2	Small Inductor	100nH
C_s	Filter Capacitor (Over-shoot)	$100\mu F$
V_in	Input Voltage	12V
V_o	Output Voltage	3.3V
	LoadChange	
	Low (3.3Ω)	1A
	High(110mΩ)	30A
f_s	Switching Frequency	100KHz

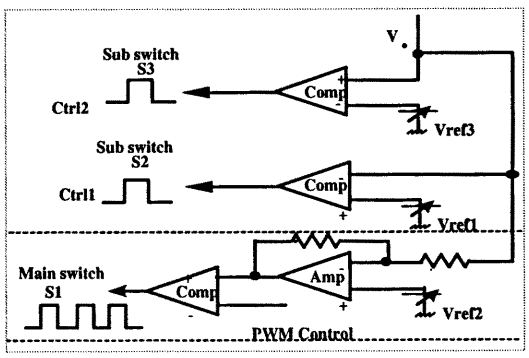


Fig.7 Control Scheme.

2.5 Specifications and Circuit Parameters

Circuit specification and parameters used in the simulation and experiments are in **Table1**.

3. Simulation Results

Based on the specifications and circuit parameters on the **Table1**, circuit simulation is performed using the OrCAD simulation software. The output voltages are measured at the VRM output, during the step load transition from 1A (3.3Ω) to 30A ($110m\Omega$). **Figs.9(a), 9(b)** show the simulation results for conventional buck and proposed topology

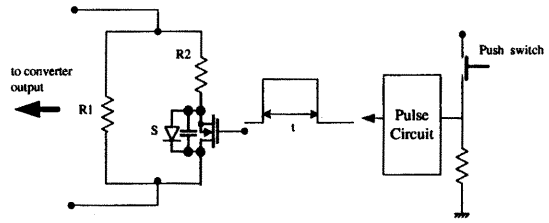
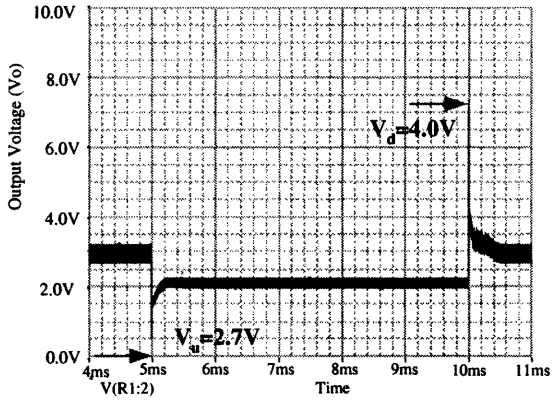
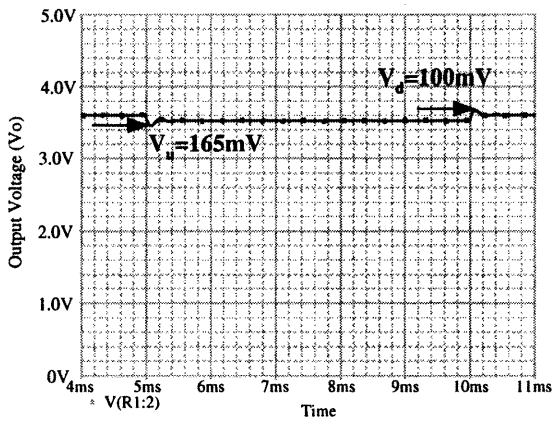


Fig.8 Step Load.



(a) Conventional topology

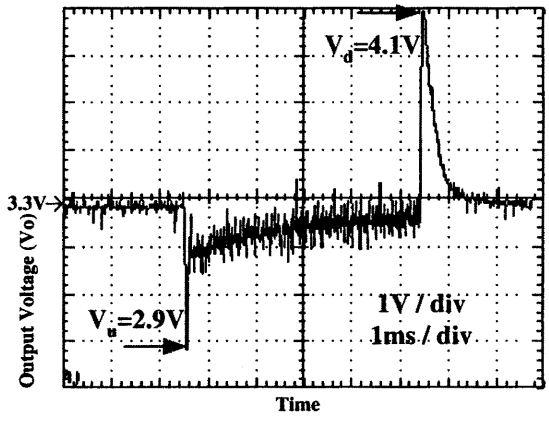


(b) Proposed topology

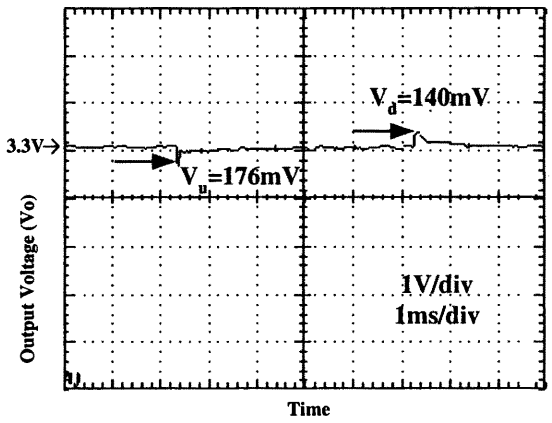
Fig.9 Output voltage variations during step load transition:simulation results(load change from 1A to 30A).

4. Experiment Results

The experimental circuit is built with the specifications and circuit parameters on the **Table1**. The output voltages are measured at the VRM output, during the step load transition from 1A (3.3Ω) to 30A ($110m\Omega$). **Figures10(a), 10(b)** show the experiment results for conventional buck and proposed topology. The simple circuit shown in **Fig.8** is used to imitate the microprocessor load. The R1 is 3.3Ω resistor at light load operation. R2 is on resistance of the MOSFET (S). When push switch is pressed, on resistance of switch S2 is connect parallel to the resistor R1, and total resistance become $110m\Omega$. This method occur, step change of load current from 1A to 30A .



(a) Conventional topology



(b) Proposed topology

Fig.10 Output voltage variations during step load transition:experiment results(load change from 1A to 30A).

5. Conclusion

The basic design of the LC clamp topology has been proposed and experimentally verified. Both simulation and experimental results prove that proposed topology is improved the transient response significantly for both step-up and step-down load transitions. The voltage drops at the step-up and step-down load transitions are only 5% ($\Delta V_u = 176mV$) and 4% ($\Delta V_d = 140mV$) of the output voltage respectively. The proposed converter can be applied to conventional buck converter to much improve transient response with only additional two MOSFETs, and a capacitor. Control circuit is simple and can be implemented with an existing PWM controller IC. Also in steady state, output ripple can be designed to be small as possible using large steady state output inductor. It is believed that the proposed topology is very suitable for fast transient response requirement of present and future microprocessors in a compact size at a very affordable price.

Acknowledgments

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