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Study of Contact Resistance on Organic Thin-Film Transistor with Surface Treatments

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In organic thin-film transistors (OTFT), the fabrication processes such as surface treatment method, substrate temperature and deposition rate give significant effects on TFT device performance. We have investigated the variation of electrical performance on DNTT-based OTFT devices influenced by the fabrication processes. The DNTT films deposited on HMDS-treated SiO_2 substrates at the substrate temperature of 60 °C, resulting in high OTFT performance with mobility greater than 0.56 $cm^2/(V \cdot s)$ and I_{on}/I_{off} greater than of 10^6. In addition, the prominent decrease of contact resistance to almost a one-tenth or less is observed from influence of surface treatment process.

Keywords: organic thin-film transistor, DNTT, surface treatment, self-assembled monolayer

1. Introduction

Organic thin-film transistor (OTFT) devices have been attracting considerable attention and are expected to open up a range of new application opportunities in electronics. The low-cost simplified fabrication process via printing technology has great potential for applications such as flexible displays, flat panel displays, and low-end smart cards.[1-5)]

Numerous research had previously been conducted on the stability of OTFT and by implementing the reported results[6-10)] from literature, the OTFT's fabricated in Kyushu University can be greatly improved by using dinaphtho[2,3-b:2′,3′-f]-thieno[3,2-b]thiophene (DNTT; Nippon Kayaku Co.) as described in references.[11-13)] The fabricated OTFT's show excellent electrical characteristics and high stability in air as will be further discussed in the results and discussion section.[14)]

Optimization of the OTFT fabrication conditions, however, is a far more complex problem to understand, as it is difficult to distinguish the difference between the effects caused by the materials used, and those coming from the conditions of fabrication processes. A literature review of previous work on OTFT show that the electrical characteristics of OTFT is greatly affected by the fabrication conditions such as surface treatment methods,[15-18)] substrate temperature,[19-20)] grain size[21)] and other parameters. The interaction between each parameter however is still not fully understood and requires further investigation to determine the relationship between each process.

In this paper, we intensively investigated the effects of resistance of DNTT-based OTFT under the conditions of surface treatment process, the surface morphology of organic semiconductor thin-film, different substrate temperature during deposition and the contact resistance revealed with the modified transmission-line method (TLM).

2. Experimental Methods

We fabricated bottom-gate top-contact OTFT where the gate and gate-insulator are located underneath the active layer and the source and drain are placed just on the top of active layer. The active layer was made of

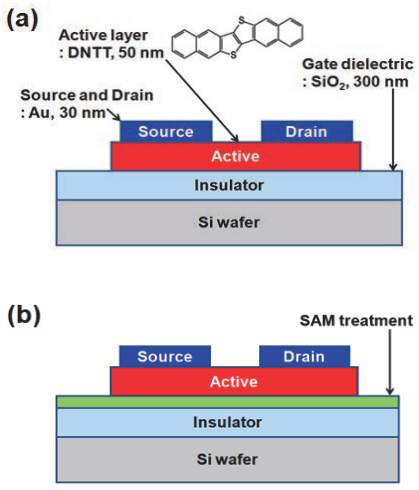

Fig. 1. (a) Cross section of DNTT-based OTFTs, (b) cross section of OTFTs on surface treatment.

evaporated DNTT on a silicon wafer with thermal insulator. The cross-sectional view of structure for top-contact DNTT-based OTFTs is schematically shown in Fig. 1(a).

In this device, we used an n-type silicon wafer substrate as the gate electrode with a thermally oxidized layer of SiO_2 (300-nm) as a gate insulator. This n-type silicon substrate was ultrasonically cleaned in acetone and isopropanol (IPA), then further cleaned by UV-ozone (UV/O_3) and spin-coated with hexa-methyl-di-silazane (HMDS). The active layer was then deposited with a thickness of 50-nm by thermal evaporation of DNTT at room temperature (RT), using a shadow mask to define the coverage area. Finally, a 30-nm-thick Au layer was deposited by thermal evaporation to provide the source/drain (S/D) electrodes, these being patterned using a shadow mask with a defined channel width and length of 2000 and 50 μm, respectively.

Preliminary OTFT study was carried out using top-contact type devices, which were fabricated on Si/SiO_2 substrates whose surface were treated with UV/O_3 or HMDS or octadecyltrichlorosilane (OTS). The schematic view of the device with self-assembled monolayer (SAM) treatment is shown in Fig. 1(b). For this device, the fabrication process was completely the same as that for the top-contact structure, with the exception that the surface treatments were performed before the active layer deposition process.

In the case of the UV/O_3-treated, the surface of the SiO_2 was cleaned with UV/O_3 for 5 min. In the case of the HMDS-treated, the surface of the SiO_2 was cleaned with UV/O_3 for 5 min, and then spin-coated with HMDS. Moreover, in the case of the OTS-treated device, the surface of the SiO_2 was cleaned with UV/O_3 for 5 min, and then dipped into a SAM solution of OTS in IPA for 30 min at RT. After picking up the sample from this solution, it was immediately cleaned with IPA and N_2 gas blowing. Finally, a layer of DNTT and S/D electrodes was deposited by thermal evaporation at RT.

The current-voltage (*I-V*) characteristics were measured in the ambient environment using an Agilent E5270B and E5281B module. The studied OTFTs exhibited good field-effect transistor behaviors. Atomic force microscopy (AFM) measurements were performed using a SPI388N + SPA400-AFM Scanning Prove Microscopy (Hitachi Co. Japan).

For contact resistance extraction, we employ the modified transfer-line method which has shown better accuracy.[22-23] The total drain-source resistance (R_{Total}) is given as a sum of the contact resistance ($R_{Contact}$) and channel resistance ($R_{Channel}$) and it is expressed as

$$\frac{R_{\mathrm{Total}} \times W}{L} = \frac{1}{\mu C_i (V_G - V_T)} + (R_{Contact} \times W)\frac{1}{L}, \quad (1)$$

where W is the channel width, L is channel length, C_i is the unit area capacitance of the dielectric. The contact resistance thus can be extracted as the vertical intercept by fitting the channel length dependent total resistance.

3. Results and Discussions

Preliminary OTFT studies were carried out using top-contact type devices fabricated on Si/SiO_2 substrates whose surface were treated with either UV/O_3, HMDS or OTS.

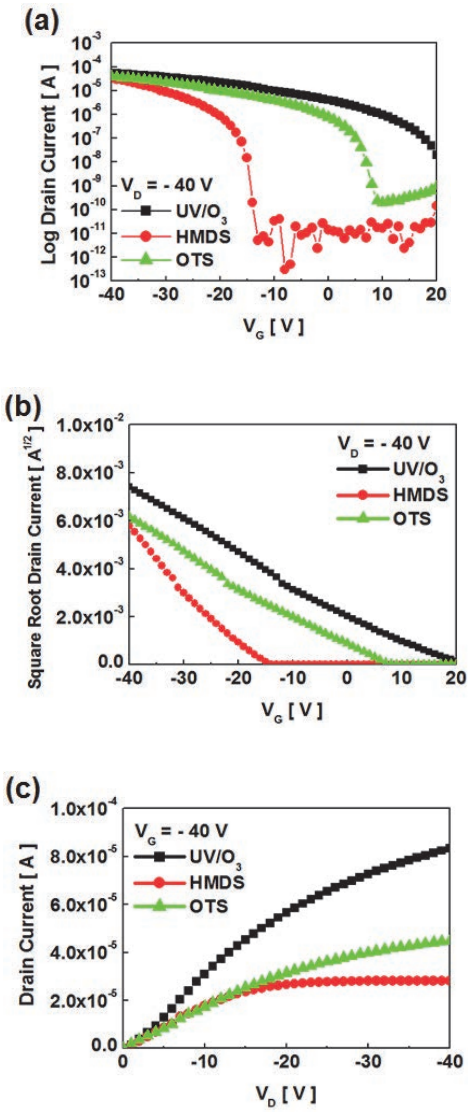

Fig. 2. TFT characteristics of DNTT devices with different surface treatment; (a) Transfer characteristics in log scale, (b) in liner scale, and (c) output characteristics.

Figure 2 shows the electrical characteristics for DNTT-based OTFTs depending on the surface treatments. Figures 2(a) and 2(b) show the transfer characteristics of the device in the saturation regime V_{DS} = -40 V at various gate voltages (V_{GS} = 20 to -40 V). From the transfer characteristics of the top-contact structure with UV/O_3-treatment, it was calculated that μ_{FE} = 0.08 $cm^2/(V \cdot s)$, V_{th} = 13.9 V, and I_{on}/I_{off} is on the

order of 10^3. Similarly, the transfer characteristics of the top-contact with HMDS-treatment were μ_{FE} = 0.35 cm^2/(V·s), V_{th} = -19.5 V, and I_{on}/I_{off} ~ 10^7, whereas those of the top-contact with OTS-treatment were μ_{FE} = 0.11 cm^2/(V·s), V_{th} = -1.0 V, and I_{on}/I_{off} ~ 10^5. Figure 2(c) shows the output characteristics of an OTFT device in the saturation regime at V_{GS} = -40 V, within a voltage bias range of V_{DS} = 0 to -40 V.

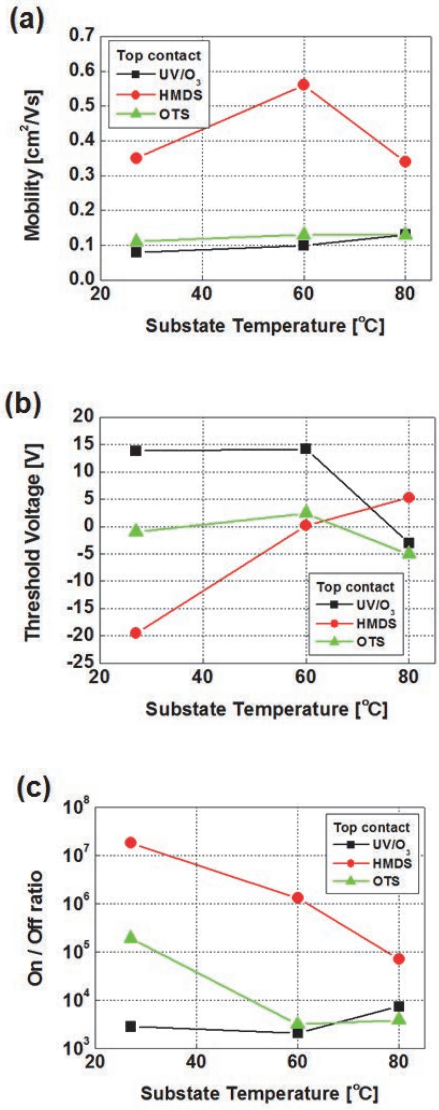

Fig. 3. TFT characteristics of DNTT devices with different surface treatment and under different T_{Sub}; (a) mobility, (b) threshold voltage, and (c) on/off ratio.

In addition, the DNTT-based OTFTs were also fabricated under different substrate temperatures (T_{Sub}) during deposition (RT, 60, or 80 °C) as shown in Fig. 3. Figure 3(a), 3(b), and 3(c) show the mobility, threshold voltage and on/off ratio of OTFTs fabricated to different surface treatments. All the devices fabricated under various substrate temperature during deposition showed typical DNTT-based OTFT characteristics with μ_{FE} higher 0.1 cm^2/(V·s), and I_{on}/I_{off} of around 10^5 under ambient conditions (Figure 3 and Table 1). In particular, the best TFT characteristics with μ_{FE} higher 0.35 to 0.56 cm^2/(V·s), I_{on}/I_{off} of around 10^6 and V_{th} higher -19.5 to 0.2 V were observed in DNTT-based device fabricated under different substrate temperature during deposition at around 60 °C with film deposited HMDS-treated surfaces.

The transistor characteristics were degraded significantly when the substrate temperature was increased above 80 °C during the deposition process. Key device performance parameters, such as field-effect mobility, on/off ratio, threshold voltage, and on-current, were extracted using standard procedures. The results are summarized in Table 1.

Table. 1. TFT characteristics of DNTT devices fabricated on Si/SiO_2 substrate with different surface treatment and under different T_{Sub}.

Surface-treatment reagent	T_{Sub} [°C]	μ_{FET} [cm^2 V^{-1} s^{-1}]	I_{on} / I_{off}	V_{th} [V]	On-current [A]
UV/O_3	RT	~0.08	2.8 X 10^3	13.9	5.5 E-05
	60	~0.10	2.1 X 10^3	14.2	6.7 E-05
	80	~0.13	7.4 X 10^3	-3.0	4.2 E-05
HMDS	RT	~0.35	1.8 X 10^7	-19.5	3.4 E-05
	60	~0.56	1.3 X 10^6	0.2	2.1 E-04
	80	~0.34	7.1 X 10^4	5.3	1.6 E-04
OTS	RT	~0.11	1.9 X 10^5	-1.0	3.8 E-05
	60	~0.13	3.1 X 10^3	2.4	5.4 E-05
	80	~0.13	3.9 X 10^3	-5.1	3.8 E-05

The analysis of grain size and crystalline microstructure are often used to evaluate the surface morphology of organic semiconductor thin-films. The film morphology of DNTT films grown on SiO_2 substrates were characterized by AFM, and the results highlight the effects of surface treatment, and substrate temperature, as shown in Fig. 4. For all present experiments, the grain size increases as T_{Sub} is increased. Although a hydrophobic surface usually results in large grains, the trend is not obvious in the present DNTT semiconductor.

In the case of DNTT, the films deposited on SiO_2 surface have quite different film morphology compared to the films deposited on UV/O_3-treated surfaces as shown in Figs 4(a), 4(b) and 4(c). The size of these void structure increases with the grain size when the films are deposited at higher substrate temperatures. Alternatively, the films on HMDS-treated substrates in Figs 4(d), 4(e) and 4(f), and those on OTS-treated substrates in Figs 4(g), 4(h) and 4(i) have similar film morphologies. At different substrate temperatures during deposition, the film morphology changed significantly.

DNTT films deposited on HMDS-treated substrate at T_{Sub} = 60 °C exhibit both large grain and good grain interconnectivity, resulting in TFTs exhibiting the highest performance metrics (Table 1). However, the grain sizes of the DNTT films are far smaller than that of OTS-treated films.

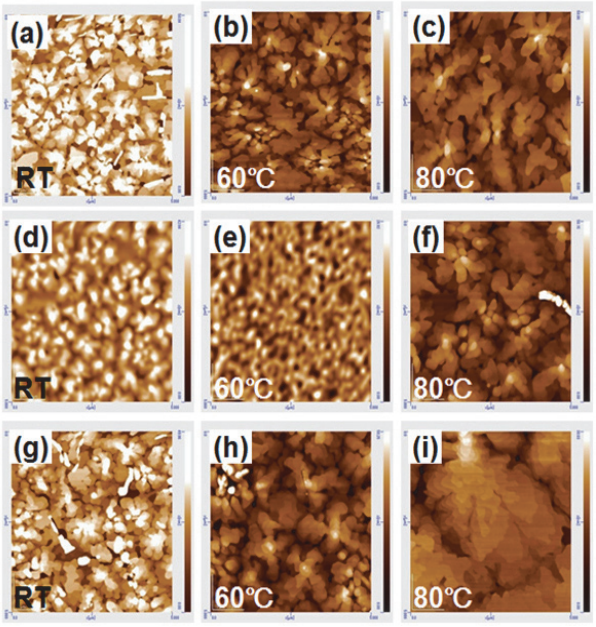

Fig. 4. AFM image of a DNTT film with different surface treatment and under different substrate temperature (T_{Sub}); (a) UV/O_3 (RT), (b) UV/O_3 (60 °C), (c) UV/O_3 (80 °C), (d) HMDS (RT), (e) HMDS (60 °C), (f) HMDS (80 °C), (g) OTS (RT), (h) OTS (60 °C), and (i) OTS (80 °C) in the scale of 5 μm × 5 μm.

Also, the surface condition of the insulator film affects the performance of the TFT. The surface-treatment process often causes damage to functional groups at the surface of the polymer insulator that leads to a change from a hydrophobic to a hydrophilic surface. Figure 5 shows the dependence of the water contact angle at the insulator surface on the surface-treatment process. As we can see from the figure, the contact angle is decreased from 45° to 16° after the exposure to UV/O_3-treatment, to

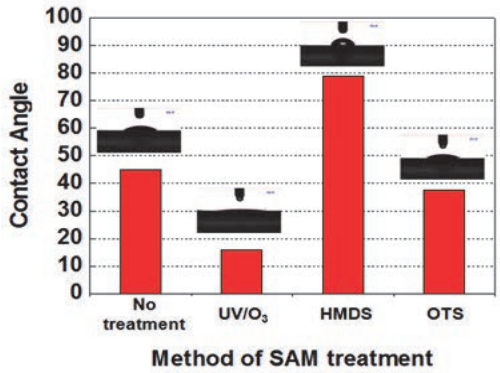

Fig. 5. Dependence of the water contact angle at the SiO_2 surface in the surface-treated process.

79° after the HMDS-treatment and to 37.5° after the OTS-treatment.

Finally, the performance of the TFT is not only affected by the surface condition but also the S/D contact resistance. To further investigate the various surface treatment effects, the analysis on total resistance of TFT channel (R_{Total}) was made by employing the method of modified TLM. Typical liner relationship of the total resistance to the channel length is demonstrated for a DNTT-based OTFT in Fig. 6. The channel-length dependence of R_{Total} for different surface treatments in Fig. 6(a) can be well-linearly fitted and thus the contact resistance can be obtained by the method descried in Eq. 1. The extracted total resistances under different substrate temperature during deposition are shown in Fig. 6(b) with black square (UV/O_3-treatment), red circle

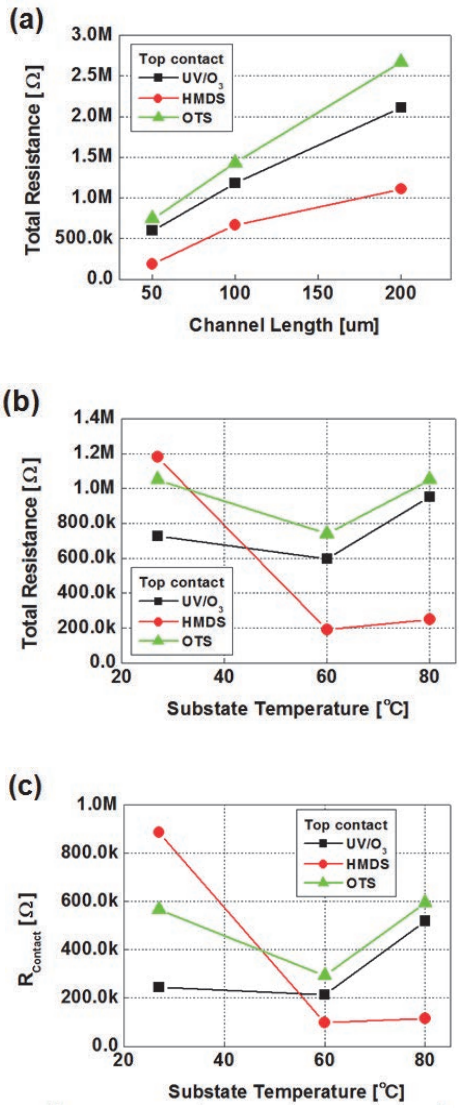

Fig. 6. TFT characteristics of DNTT devices with different surface treatment and under different T_{Sub}; (a) the extracted total resistance with channel length(T_{Sub} = 60 °C), (b) the extracted total resistance, and (c) the extracted contact resistance with various surface treatment processes.

(HMDS-treatment), and green triangle (OTS-treatment).

In addition, the extracted total resistance shows a big difference at the substrate temperature of 60 °C. The extracted contact resistances under different substrate temperature during deposition are shown in Fig. 6(c).

The total and contact resistance of DNTT-based OTFTs were compared at different substrate temperatures. Figure 6 shows the surface treatment dependent resistance of OTFT characteristics on different substrate temperatures.

It clearly shows a prominent decrease of total resistance by almost half as observed by the effect of various surface treatment process (HMDS-treatment) with the different substrate temperatures as shown in Fig. 6(b). Also, a prominent decrease of contact resistance by almost one-tenth is observed by the effect of surface treatment (HMDS-treatment) as shown in Fig. 6(c).

4. Conclusions

In this paper, we intensively investigated the channel resistance of DNTT-based OTFTs devices under the influence of the surface treatment process, the surface morphology of organic semiconductor thin-film, different substrate temperature during deposition and the contact resistance through the modified TLM. The DNTT films deposited on HMDS-treated SiO_2 substrates at a properly adjusted substrate temperature results in high OTFT performance with mobility greater than 0.56 $cm^2/(V \cdot s)$, and I_{on}/I_{off} greater than that of around 10^6.

In addition, a prominent decrease of contact resistance is observed through the influence of surface treatment process.

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