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Safety Operation Area Based Design Methodology for Gate Controlled Power Semiconductor Device

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Safety Operation Area Based Design Methodology for Gate Controlled Power Semiconductor Device

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I. Introduction : SOA and other fundamental characteristics

At least one power semiconductor device is used in every electrical facility. In the field of power supply network, traction, automotive and motor control in factory automation, the amount of electrical power is very high. Once trouble occurs, the damage could not be limited in device itself. There is not so small possibility that the damage would extend to the entire facility or system. It would costs both economically and socially expensive. It is necessary not only to minimize the power dissipation but also to specify the device characteristics of SOA (Safety Operation Area) with sufficient margins. The improvement of power losses, which corresponds to the thermal dissipation, is the first priority of the R&D (Research & Development) of power semiconductor chip. From this point of view, a large number of theoretical and experimental studies have discussed deeply inside of the device operation about the design indexes and methodologies. For example, it is well known that an IGBT (Insulated Gate Bipolar Transistor), which is widely used in power electronic systems, has a strong tradeoff relationship between a conduction loss and a switching loss. The improvement of this tradeoff is the one of the most important index[(1)] of the R&D phase. Moreover, it is necessary to visualize the SOA as the device's operational boundary. Before discussing the SOA related complex relationship[(1)], the category and the application of power semiconductor devices are overviewed in the following section I-1.

I-1. Application range of power semiconductor devices in power electronics systems

In the Eco-Green stream, recently power devices are highlighted. But it seems that power devices' functions are little known in case of comparing with LSI's (Large Scale Integration circuit) applications as a signal device, such as memory, logic and micro-processor. It is not easy to define the applications of power devices, because power devices have an extremely large territory in the map of a rated voltage and current range according to its operational frequency, as shown in Fig. I-1[(2)(3)]. In addition, power devices have a large structural variation depending on application as shown in Fig. I-2[(2)(3)].

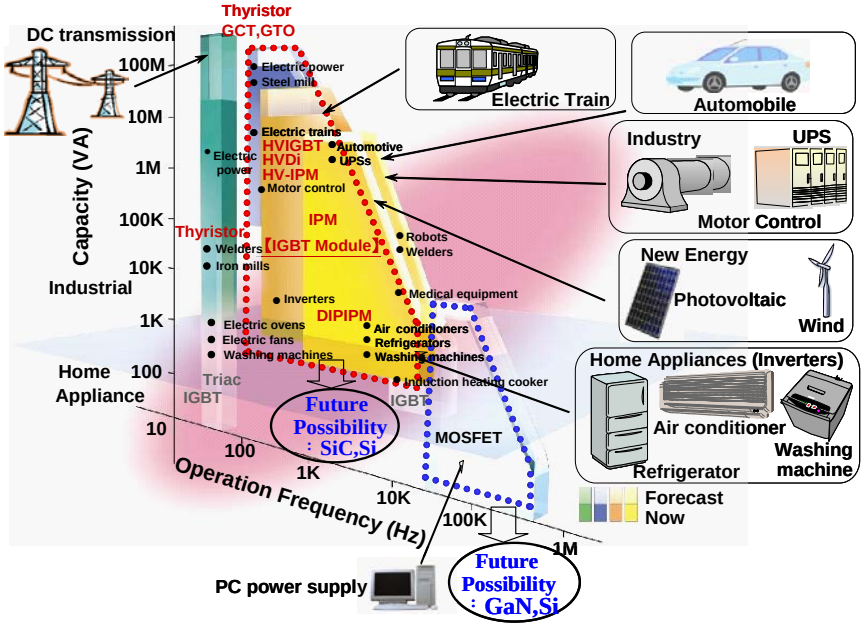


Fig. I-1. Power handling capability and Operation frequency of power semiconductor devices[(1)]

The rated voltage of the power device is defined as the following, corresponding to the commercial AC (Alternative Current) supply voltages. The power device's 600V and 1200V *BV* (Breakdown Voltage) classes correspond to the commercial AC 100V and 200V power lines, respectively.

Saving energy to keep sustainability of the earth requires high efficiencies in each step of the electric energy conversion process, including the generator, the supply, the converter and the inverter. The number of nodes in the above supply-chain of electric power flow has been increasing more and more.

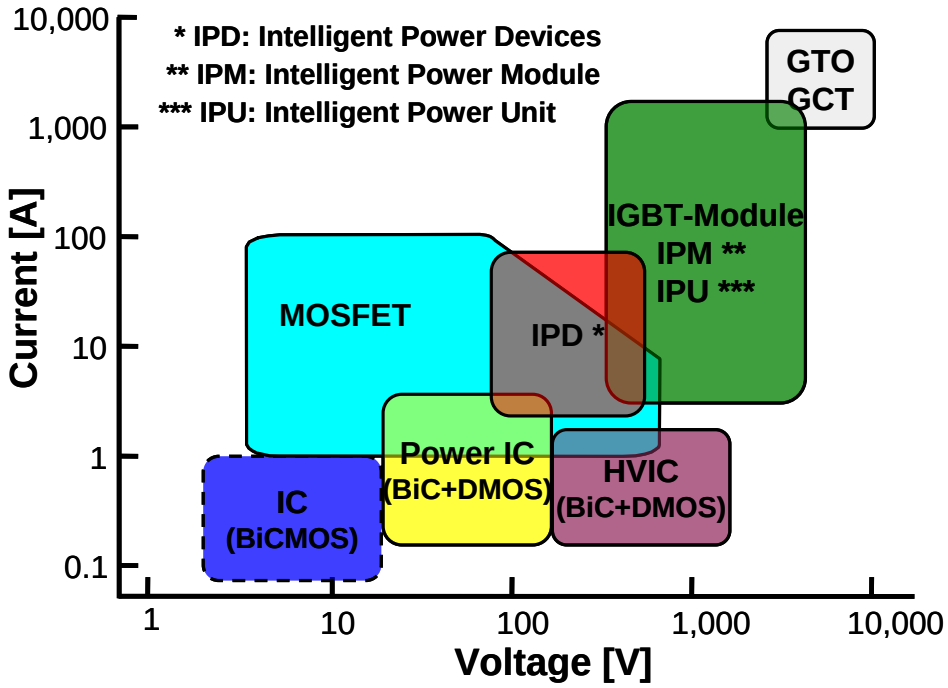


Fig. I-2. A territorial map of power devices as a function of the voltage class (not an AC plug voltage) and electrical current[(1)(2)(3)]

A lateral power device as a family of ICs (Integrated Circuit), such as Power IC and HVIC (High Voltage IC), is categorized in the low voltage and low current range as shown in Fig. I-2 and/or in the relatively high frequency region in Fig. I-1. A MOSFET (Metal Oxide Semiconductor Field Effect Transistor) as a unipolar device is the largest product in the market owing to the various applications which utilizes its high frequency operation characteristics and simplicity of gate drive. So the MOSFET is used in the low power and high frequency region, e.g. Office Automation, Personal Computer and wireless communication applications as shown in the Fig. I-1. The combination of the IGBT and the associated diode covers the major part in this territorial map. It offers a wide application in the middle and high power range, e.g. a motor control usage for home appliance, industrial equipment, automotive and locomotive. The historical standard thyristor and the GTO (Gate Turn-Off thyristor) or GCT (Gate Commutating Thyristor) are still major in high voltage and high current but low frequency region, e.g. traction and power plant.

For examples, stand-alone power generators, a wind power or a photo-voltaic power system are constituted of an individual power conditioner to regulate the bidirectional electrical power flow, a converter and an inverter (and a break). Such system is known as smart-grid system. The smart grid system has gradually

spread while recently accelerated. The system of this kind requires both power module parts and smart parts, which are combination of low voltage (5V or less) LSIs as the signal processor and HVICs (600-1200V) as the interface of LSIs and power modules.

IGBT and diode are roughly categorized into three voltage classes according to their operating voltages, i.e. low, medium and high voltage classes corresponding to 200-600V, 1200-1700V and 1700-6500V, respectively. The 6500V class devices are dedicated to the power supply and the traction application.

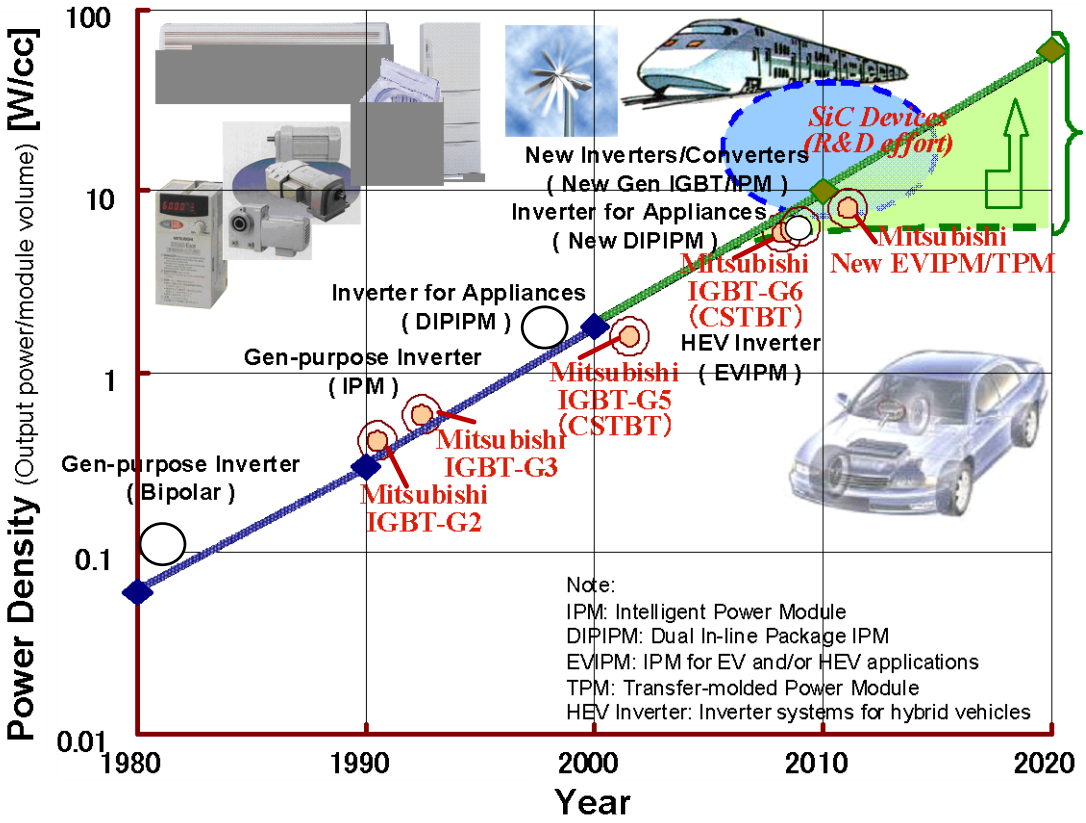


Fig. I-3. Power density enhancement for medium power range of PE (Power Electronics) Equipment[(2)(3)]

In the PE (Power Electronics) field, the power density is defined as the amount of output power per volume unit of the element of power electronics. This is one of the most important indexes and has increased in the ratio of approximately 5 times in a decade as graphically illustrated in Fig. I-3[(2)(3)]. The definition of the generation of IGBT is not standardized for all the companies in this PE field. For example, Mitsubishi Electric's latest generation is 6th, while other companies have other naming rules for the generation and the product nickname. But the above ascending tendencies of the power density are almost identical in the power electronics field. This will be maintained in the next generation concept of power module planned in the very near future. From this fact, it is easily inferred that, towards a higher power density, IGBT and diode chip and package technologies have played an important role to realize the reduction of cost, foot print, volume and the weight of power electronics systems.

In the next section I-2, the fundamental function of power device is described to explain what SOA is.

I-2. Fundamental switching function of power semiconductor device

The power device is a switch, which is directly located in the main current flow line as shown in Fig. I-4[(1)]. The current-flowing path of an ideal switch is considered to be an electric conductor in the ON state and to be an insulator in the OFF state mode. If the ideal switch is replaced with a transistor made of semiconductor material like silicon, R_{on} (the ON state Resistance) is higher than that of a metal and $I_{leakage}$ (leakage current in the OFF state) is higher than that of an insulator. Ideally R_{on} and V_{on} (ON state forward Voltage drop) is expected to be zero, and an $I_{leakage}$ is expected to be zero. Its switching energy losses are also expected to be zero. In the practical device, V_{on} is several volts at the rated current of a hundred amperes. Both E_{on} (turn-on Energy loss) and E_{off} (turn-off Energy loss) are large enough values to heat up the devices itself.

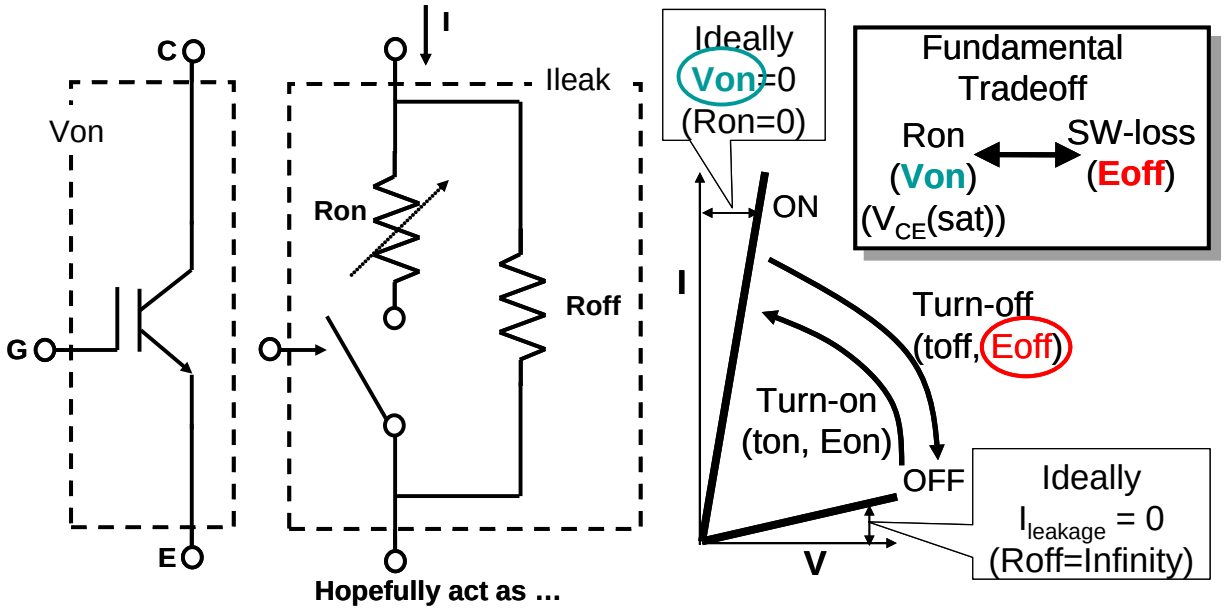
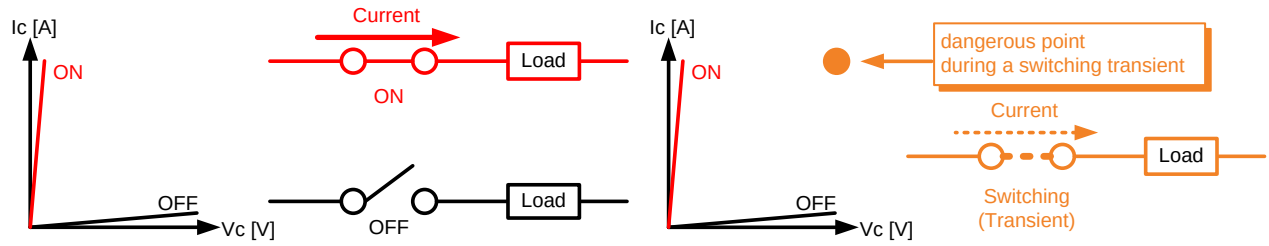


Fig. I-4. Power chip as a switching element, and the fundamental tradeoff relationship between V_{on} and E_{off}[(1)]

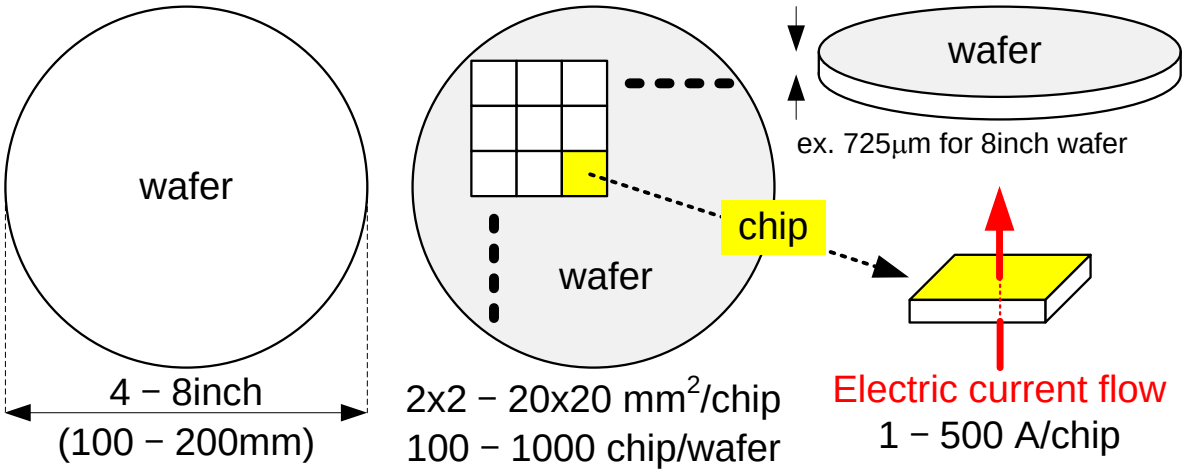
There exists a very tight tradeoff relationship between V_{on} and E_{off}. The low V_{on} means that electrical current easily conducts, but E_{off} tends to increase, vice versa. So, for IGBT, this fundamental tradeoff between the $V_{CE(sat)}$ (ON-state Collector-Emitter saturation Voltage) or simply V_{on} and E_{off} is used as the index of the device characteristic and the generation. Using the 1st quadrant of this V_c-I_c plane expression in Fig. I-4, the next chart Fig. I-5 explains the necessity of the SOA concept. Here, V_c and I_c stand for the voltage and electrical current in a positive biased direction at a device collector terminal.



(a) Static ON and OFF state (safety) (b) Dangerous point during the switching transient

Fig. I-5. The schematic idea for a dangerous point during the switching transient against the static ON and OFF states as the safety position

To grasp the SOA concept, as the first step, a certain dangerous operational point is assumed to be during the transient moment in comparison with the static ON state and OFF state. Fig. I-5. shows the schematic idea for a dangerous point during the switching transient against the static ON and OFF states as the safety position. Referring Fig. I-5 (a), when the switch is connected tightly, the electrical current flows from the power supply (not shown) through the switch part to a load as shown in the upper part as the red line. This is "ON" state. This is also described as the steep red line very close to the y-axis I_c, but it is not to be identical the *Ic* axis itself because of a certain resistance of switch itself as the semiconductor material. When the switch is disconnected, the electrical current dose not flow as shown in the lower part as the black line. This is "OFF" state. This is also described as the very low angled black line very close to the x-axis V_c, and it seems to be almost identical to the V_c axis in the same measurement range of the ON state Ic, because the leakage current of the semiconductor switch is small as the range of mA or less. As shown as the orange colored filled circle mark in the V_c-I_c plane of Fig. I-5. (b), There sexist a certain dangerous point during a switching transient in both "ON to OFF" and "OFF to ON". The time period of this transient point is short as the order of micro-second, but the power as the product of the voltage (*V*) and current (*I*) is extremely high. Moreover, the real position strongly depends upon a kind of load type, resistive and inductive, and other various driving condition of device. And the operational temperature is also taken into account. Even in such a dangerous moment, device would be survival. The SOA is the area where the device can survive in the V_c-I_c plane all the moment when the device faces to.



(a) Wafer dimension (b) Chips' array placement in an wafer (c) Wafer thickness
(d) Electric current flow through the power chip

Fig. I-6. Dimensions of the power semiconductor device, the chip in the wafer

To grasp the dimensions of the power semiconductor chips in the wafer, schematic features are described in Fig. I-6. As the mentioned above, according to the rated voltage class and electric current class, there are many varieties for the chip in their size and thickness. The wafer size is also independently chosen by each manufacturing company from the mass-production efficiency point of view.

(a) MOSFET example (1) (b) MOSFET example (2) (c) Diode example (front view) (d) Diode example (backside view)

Fig. I-7. Destruction examples of MOSFET[4] and Diode[5] to evaluate the SOAs in the laboratory
All the hole size is around 0.2mm by using the rapid shut-down protection circuit.
Chip sizes are several millimeters square but different for each other.

To show how dangerous the switching failure, several optical photo images are shown in Fig. I-7[4][5]. These kinds of figures are usually not disclosed about the real failure mode in the field, and the most of cases are literally exploded and could not remain any small portion of chip through the extremely large electrical power of more than kW order. Using the recent rapid shut-down protection circuit in the laboratory, the destruction size has been controlled to be relatively small in the R&D phase as shown in Fig. I-7. But the energy was still large enough to melt through the Si chip form the top surface to the bottom as shown in Fig. I-7 (d). These are "good" destruction examples, which mean that position of the destruction are located as the design expected.

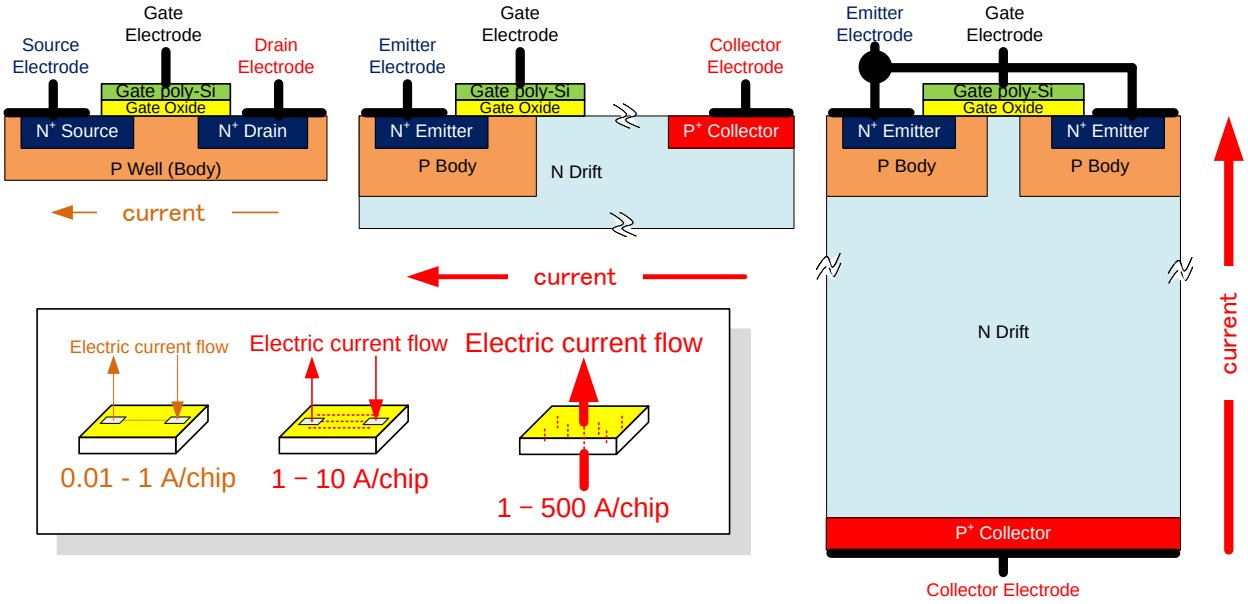
It is the most important to estimate the SOA. So, this study focused on how to estimate the SOA.

Further detail description is in the later part of the next chapter II after reviewing the traditional step-flow of the design methodology of the medium-high power semiconductor device including several theoretical and analytical descriptions about the fundamental characteristics.

I-3. Vertical device for large current usage

As shown in Fig. I-8 (c), A major power device such as the N-channel IGBT is a vertical device, in which a main current from the collector in the backside of the device to the emitter in the front side indicated as the thick arrow beside the IGBT cell. An entire thickness of the Si wafer is an active region. All the cells in a single chip operate simultaneously to handle the large electrical current of 100A, which requires 1cm^2 as an active area in a single chip in case of the rated collector current density Jc of 100A/cm^2. Moreover, there is no redundancy. In case of 1200V class device whose rated switching voltage is 600V, simple math of the electrical power reaches 60,000W at the "dangerous" point in Fig. I-5 (b), which is 600V multiplied by 100A

A lateral IGBT shown in Fig. I-8 (b) is widely used in HVIC as one of the functions of a circuit element with the electrical isolation portion (not shown). If this lateral IGBT handled the same large current of 100A, both the device thickness and width would be 1cm each but the length (distance) between the emitter and collector would be about 0.1mm or less. Of course, another geometry is possible, but it also needs a large and complex isolation region for the coexistence of the ground potential of emitter and the high voltage collector in the same front side. So the lateral device's rated current is roughly limited several amperes.



(a) Lateral MOSFET in LSI (b) Lateral IGBT (c) Vertical IGBT

small distance between S-D |--- long distance between E-C ---|

independently parallel operation synchronously parallel operation

Fig. I-8. Lateral devices and a vertical device

In contrast, a lateral MOSFET as a core element of LSI is shown in Fig. I-8 (a). The lateral MOSFET is fabricated in the very surface region of the Si wafer, its total depth is generally less than several micro-meters, which occupies only the several percentage of the wafer thickness. Basically, all the bit of MOSFET operate independently to memorize or calculate. They need only 5V or less, and the total current of the whole chip reaches 1A or so, it means the electrical power loss is less than 5W.

I-4. Recent progress of the improvement for fundamental tradeoff characteristics of V_{on}-E_{off} in IGBT

The following discussion is for the vertical N-channel IGBT device to handle the large current of 100A or more, and its chip size is around 1cm^2. And V_{on} is described as $V_{CE(sat)}$ for IGBT as the saturation voltage between Collector and Emitter after the bipolar transistor notation.

As shown in Figure I-9[1][6], the generation of device proceeds only at the moment when the fundamental tradeoff relationship between V_{on} and E_{off} shifts to the closer position to the origin of the graph. In Mitsubishi Electric case, the generation of IGBT proceeds from the planar gate designed by a 3 micro-meter rule to the planar gate of the sub-micron design rule[7], further to the trench gate type[8][9] and CSTBT™[10][11], to the current generation 7th of 600V class IGBT[12][13], which has the same concept as the 5th generation 1200V class LPT (Light Punch Through) type device[14][15]. The LPT type device structure, which uses the thin bulk wafer instead of the conventional Epitaxial crystal-growth on the thick bulk wafer, had simultaneously arisen around year of 2000 using thin wafer process technology, and several variations for its naming like a FS (Field Stop)[16][17] or SPT (Soft Punch Through)[18][19].

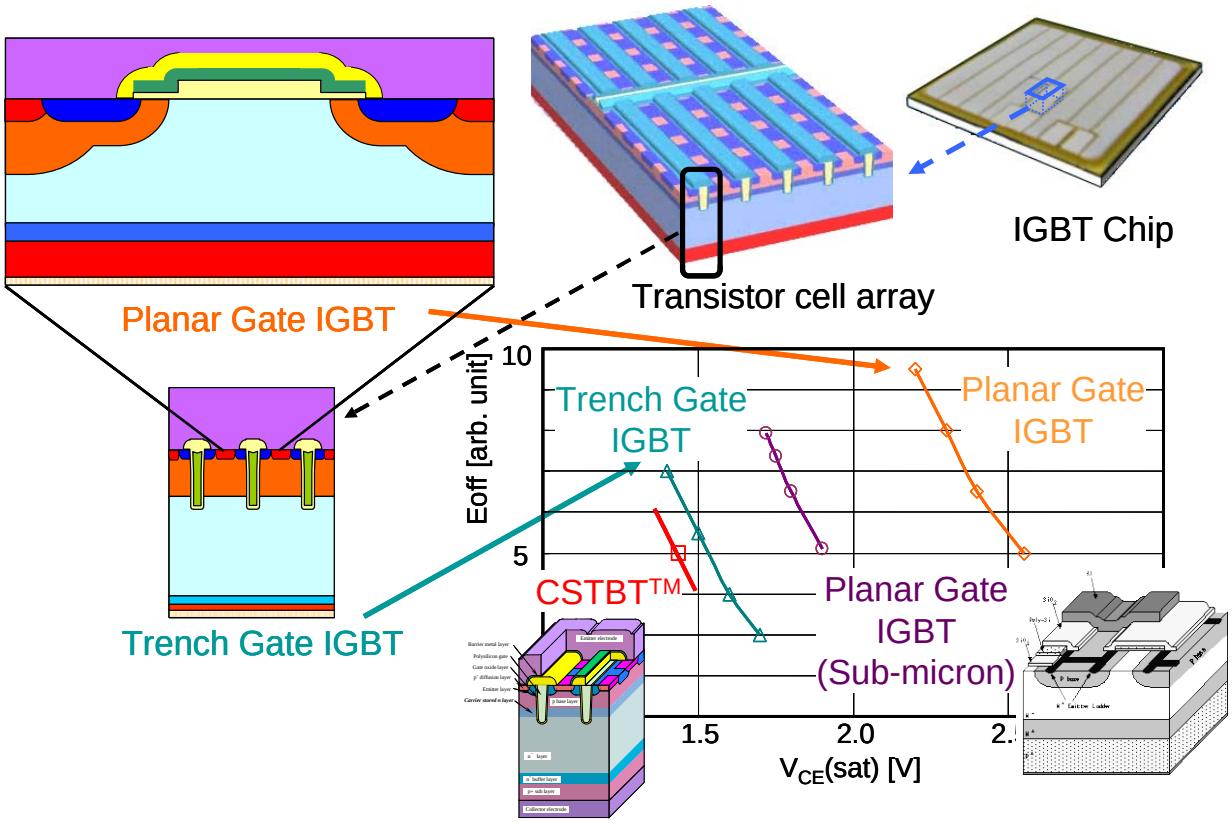


Fig. I-9. IGBT's structures for the each generation and their fundamental tradeoff characteristics[(1)(6)]

As the mentioned above, to handle 100A order large current, the IGBT chip contains IGBT unit cells of the order of mega in a parallel connection to control its current conduction by MOS (Metal Oxide Semiconductor) gate for all the unit cells simultaneously as the transistor cell array shown in Fig. I-8. Increasing its cell density is a direct way for increasing a handling current density. But, in a planar gate type device, there very strong effect to limit the cell shrinking, it is called the JFET (Junction gate type Field Effect Transistor) effect for both a unipolar device MOSFET and a bipolar device IGBT. The JFET effect is defined as an electric current path squeezed effect, when the depletion regions extend from the surrounding p-type MOSFET body regions arranged in a very narrow distance. This JFET effect in the planar gate type IGBT was overcome by its well tempered counter doping technique.

The trench gate type IGBT[(20)] had been developed to improve V_{on} characteristic towards the concept of the ideal ON state model of IGBT described as the combination of "MOSFET + PIN diode"[(21)], originally coming from the MOS controlled Thyristor idea[(22)]. Here, "MOSFET" means the MOS gate control with the negligible small channel resistance, and "PIN diode" means the hole injection part as the bipolar device to cause the conductivity modulation.

Only form this V_{on}-E_{off} tradeoff point of view, the fine patterned device seems to be good approach same as LSIs. But another tight regulation of "SOA" exists as the third direction as mentioned in section I-2.

I-5. SOA as the third direction against the fundamental tradeoff of V_{on}-E_{off}

In addition to the above fundamental tradeoff between V_{on} and E_{off}, there is the third orthogonal

direction to the fundamental tradeoff, i. e. SOA, as shown in Figure I-9[6]. The SOA are consisting of three types, i.e. FBSOA (Forward Bias SOA), RBSOA (Reverse Bias SOA) and SCSOA (Short Circuit SOA). The FBSOA is an index how large current can be handled without any latch-up phenomenon, which is the common name of the thyristor action in case of losing its gate control to regulate its current conduction. The RBSOA is another index representing the current turned-off capability under the relatively high collector voltage in an inductive load switching. The SCSOA is the most important characteristic. The SCSOA is defined as either the short circuit time endurance t_w (time endurance width in a load shorted circuit operation mode) or the energy amount E_{SC} (Energy of a load shorted circuit operation mode) as an index how long a device can be survival until the protection circuit shutting off an extremely large current during a load-shorted a dangerous mode, but device still has been preventing from losing the gate controllability.

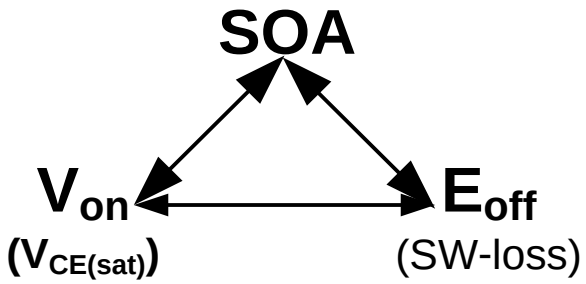


Fig. I-10. The fundamental triangular tradeoff relationship of power device[6]

This Fig I-10 means if SCSOA improved being the device generation fixed, that device would sacrifice both V_{on} and E_{off} at the same time. For example, reducing V_{on} increases a saturation current I_{sat}. To improve the V_{on}-E_{off} tradeoff, reducing N-type drift layer thickness is very effective, but it simultaneously reduces the margin of SOA and *BV*. Finally, the reduction of N-drift thickness leads to less SC endurance. In addition, different from LSIs, the voltage scaling-down is never allowed for power devices, because the AC supply voltage are fixed in 100V or 200V and the gate-emitter voltage are also fixed in 15V (from the noise point of view), in spite of an increasing tendency of the rated current for all the applications. It seems there is no exit to escape from this tight regulation of the triangular tradeoff V_{on}-E_{off}-SOA, but we should improve simultaneously.

So, the mentioned above, estimating SOA is the first priority in the recent R&D phase. Unfortunately, since the traditional design flow as the method of the power semiconductor device had not been so sophisticated, there were many "cut and try" phase, especially for SOA estimation procedure. In the next chapter II, this traditional design flow as the method of the medium-high power semiconductor device is described to clear the problems to be solved.

II. Traditional design flow of the medium-high power semiconductor device

The traditional and empirical design steps for the power semiconductor device like the IGBT are the followings.

The first step is choosing the N-drift layer's thickness and doping concentration suitable for the requirement of *BV* characteristic, such as 600V or 6500V, along the theoretical calculation with a little

modification by using the database of the previous generations.

The second step is finding out the optimum point from the V_{on}-E_{off} tradeoff curve through the test run's structural parameter variations such as the carrier lifetime adjusted by the carrier lifetime control process, N-emitter concentration or P-collector concentration.

And the final step is the evaluation of FBSOA, RBSOA and SCSOA. This step is only based upon the measurement to categorize and analyze which kind of structural parameters are major factors and their order of sensitivity.

In the next section II-1, from the above first, the theoretical calculation part is discussed.

II-1. Estimation of BV - $R_{on,sp}$ (V_{on}) of unipolar MOSFET: Si limit

Before discussing about the bipolar device like an IGBT, the unipolar MOSFET characteristics are explained. This process is necessary to understand the reason why IGBT is major is the medium and high voltage region, and why the E_{off} is the good index in case of IGBT. And it is also need to define the silicon limit as the limitation of the unipolar device's V_{on} characteristic, because the SJ (Super Junction) device will be discussed in the later chapter as the candidate of the V_{on} improvement.

The tradeoff characteristic of BV and $R_{on,sp}$ (specific ON Resistance) as the unipolar Si limit is calculated by the following equations, and the result is shown as the black line of the Fig. II-1. The first equation, in which BV is calculated as the function of N_D, is direct integration[23] of the ionization coefficient[24] for the entire region of thickness using the closed form[25].

$$BV = 5.34 \times 10^{13} N_D^{(-3/4)},$$
$$W_D = 2.67 \times 10^{10} N_D^{(-7/8)} \quad \text{is proportional to} \quad BV^{(7/6)},$$
$$\rho_D = 4.596 \times 10^{15} / N_D,$$
$$R_{on,sp} = R_{on} A = \rho_D W_D \quad \text{is proportional to} \quad BV^{(5/2)},$$
$$V_{on} = R_{on,sp} Jd,$$

where N_D, W_D and ρ_D are a doping concentration [cm^{-3}], a thickness (width) [cm] and a resistivity [Ωcm] of the N^- drift region which supports a reverse biased blocking voltage BV, respectively. $R_{on,sp}$ is the specific ON state resistance [Ωcm^2], i.e. a product of an absolute resistance and an active area (A) of device. J_c is the drain current density [A/cm^2]. There are several variation of the current density of J [A/cm^2] suffix such as J_c, J_e, J_d, J_s, J_a and J_k, and each stands for the current density of the collector and emitter of IGBT or bipolar transistor, drain and source of MOSFET, anode and cathode (k from German word of Kathode) of diode, respectively. And the figure of merit of MOSFET is generally defined by the product of this $R_{on,sp}$ and the total gate charge Q_g [C].

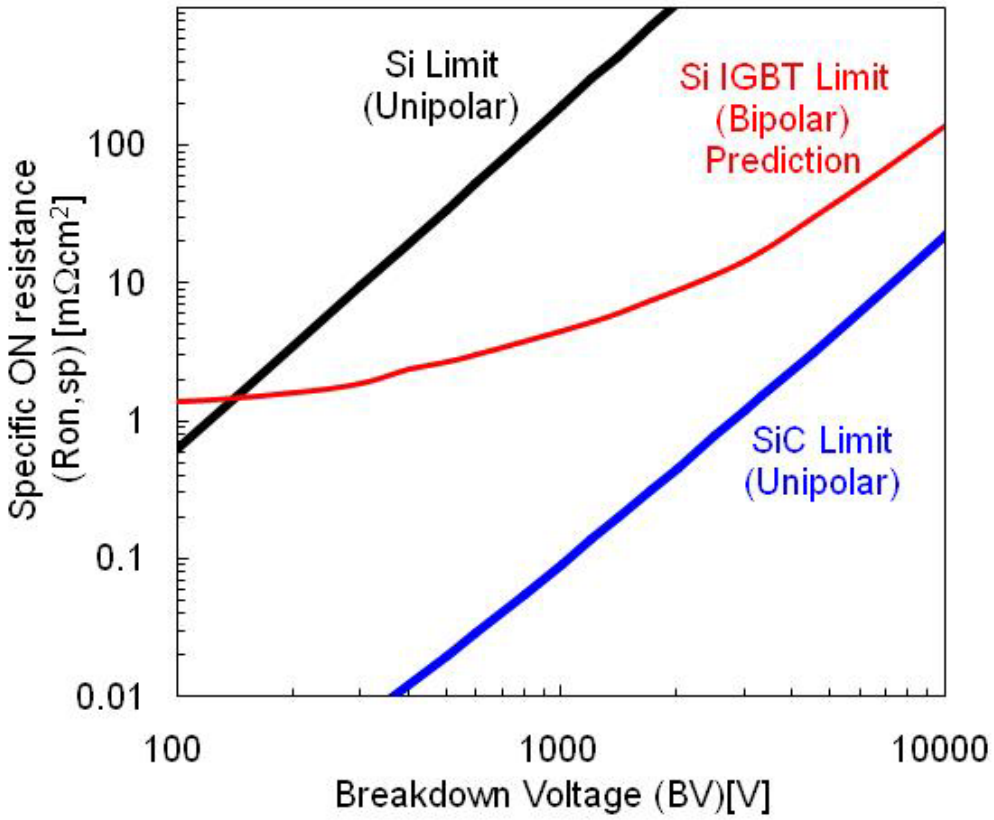


Fig. II-1. BV-$R_{on,sp}$ (V_{on}) : Si limit for the unipolar Si, SiC and the bipolar Si IGBT

On the other hand, there is no analytical description for the bipolar device limit. This is not only because $R_{on,sp}$ is not simply defined by the ohmic output V_c-I_c characteristic, but also because it is freely adjusted as the function of switching characteristics. The IGBT limit of V_{on} as $R_{on,sp}$ in Fig. II-1 is predicted from Mitsubishi Electric's road map including two more advanced generation devices. There are analytical approaches for the IGBT limit[26][27] of the V_{on} characteristics, but those could not consider both E_{off} and SOA.

Before the V_{on} characteristic, the detail expression about R_{on} components of the unipolar MOSFET and the bipolar IGBT, which are shown in Fig. II-2, is discussed as the following equations.

$$V_{on}\,(\mathrm{MOSFET}) = R_{on}(\mathrm{MOSFET})\, I_d = R_{on,sp}(\mathrm{MOSFET})\, J_d$$

$$R_{on}\,(\mathrm{MOSFET})$$

$$= R_{ch} + R_{acc} + R_{JFET} + R_{drift} + R_{N^+n} + R_{sub}$$

In the Si MOSFET, R_{ch}, R_{acc}, R_{JFET}, R_{drift}, R_{N^+n} and R_{sub} stand for the resistance of channel, accumulation layer underneath the MOS gate (not shown in figure), JFET effect, drift region, junction of N^- drift / N^+ substrate and thick N^+ substrate, respectively.

$$V_{ch} = R_{ch,sp}\, J_c = R_{ch}\, I_c\,,$$

$$R_{ch} = L_{ch} / \{Z\, \mu_{ns}(\mathrm{inv})\, \mathrm{Cox}\, (V_g - V_{th})\}\,,$$

$$R_{ch,sp} = R_{ch}\, \{(W_{cell} / 2)\, Z\} = L_{ch}\, (W_{cell} / 2) / \{\, \mu_{ns}(\mathrm{inv})\, \mathrm{Cox}\, (V_g - V_{th})\}\,,$$

$$\mathrm{Cox} = \varepsilon_0 \cdot \varepsilon_{ox} / t_{ox}\,,$$

$\varepsilon_0 = 8.854 \times 10^{14}$,

$\varepsilon_{ox(SiO2)} = 3.9$,

$\varepsilon_{Si} = 11.9$.

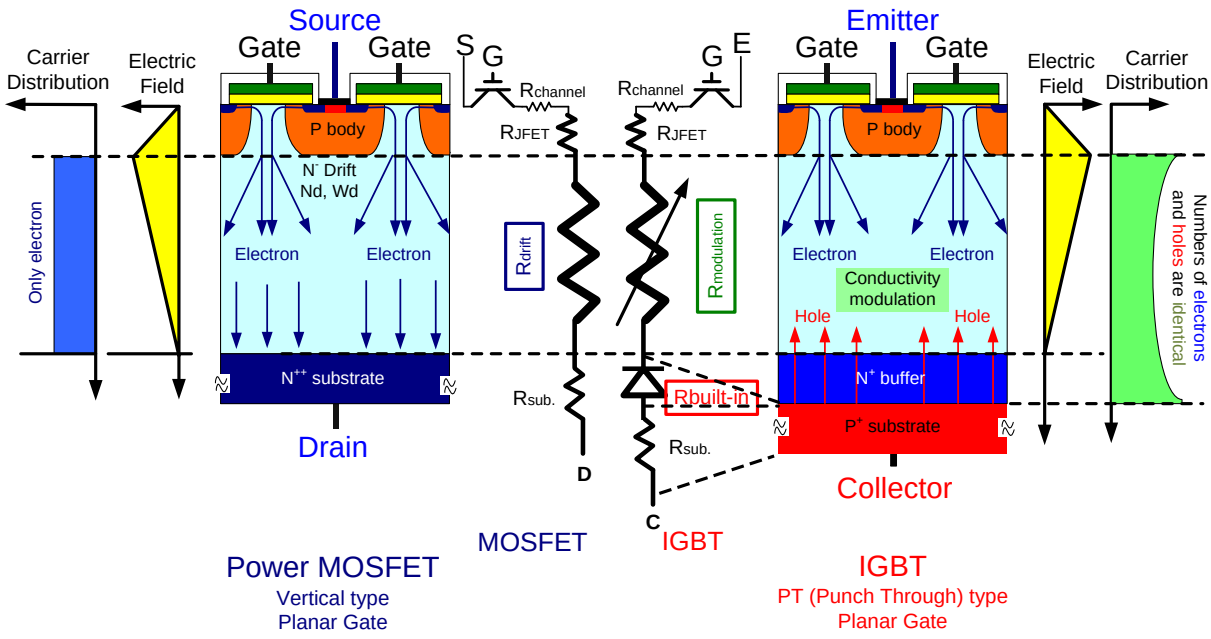


Fig. II-2. The MOSFET and IGBT operation models

The above descriptions are for the relationship between the *BV* and unipolar device's V_{on}, which has the lower limit called "Si limit" as far as the drift current flowing in the ON state. In the next section II-2, why the IGBT and other bipolar device have much lower V_{on} than the unipolar MOSFET even in the very high voltage range from the conductivity modulation effect point of view, where the current flowing in the N-drift layer is not a drift current but a diffusion current.

II-2. IGBT's N-drift part of V_{on} based on the conductivity modulation effect

For the middle and high voltage class devices, all the terms are simply proportional to the current density and the largest two factors of R_{on}*(MOSFET)* are R_{drift} and R_{JFET}, as discussed in the previous section. Especially for 600V and higher voltage class, V_{drift} is assumed to be the net V_{on}, and it is estimated by using the same equation of $R_{on,sp}$ as the function of *BV*. V_{JFET} is characterized by a geometry and size of each portion as far as using the planar gate structure. Therefore applying the trench gate, device is practically free from the JFET effect. There is almost same situation in the IGBT as long as the gate structure is concerned.

V_{on}(IGBT)

$= V_{ch} + V_{acc} + V_{JFET} + V_m + V_{pn} + V_{sub}$

$V_m = 3 (k T / q) (d / L_a)^2$, for $d < La$,

$V_m = (3 \pi / 8) (k T / q) \exp (d / L_a)$, for $d > La$,

$$d = W_D / 2 ,$$
$$L_a = (D_a \tau_{HL})^{(14)} ,$$
$$1/D_a = 1 / D_n + 1 / D_p ,$$
$$D_n = (k T / q) \mu_n ,$$
$$D_p = (k T / q) \mu_p ,$$
$$\tau_{HL} = \tau_n + \tau_p ,$$

where, D_n, D_p and D_a are carrier diffusion constant [cm^2/s] of the electrons, holes and those under the ambipolar operation, L_a is the ambipolar carrier diffusion length [cm], k is Boltzmann constant, T is the absolute temperature [K], q is a elementary charge [C], μ_n and μ_p are carrier mobility [cm^2/Vs] of the electron and hole, τ_n, τ_p and τ_{HL} are the carrier lifetime [s] of the electron, hole and their ambipolar state, respectively.

Accurately, the channel current is the remaining portion of the subtraction the parasitic PNP bipolar transistor current from the total collector current, so V_{ch} needs a factor of this ratio as the following.

$$V_{ch} = (1-\alpha_{pnp}) J L_{ch} (W_{cell} / 2) / \{\mu_{ns(inv)} Cox (V_g - V_{th})\}$$

But in the IGBT operation, the channel electron current is the major part, roughly the two thirds of the total current is this channel current, as the ratio of the electron and hole mobility ratio.

So, the comparison of the main terms of V_{on} for IGBT and MOSFET are the following equations,

$$V_{on}(IGBT) = V_{ch} + V_{JFET} + V_m + V_{pn}$$
$$V_{on}(MOSFET) = V_{ch} + V_{JFET} + V_{drift}$$

The differences are V_m and V_{pn} in the IGBT and V_{drift} in the MOSFET.

The V_{drift} is a function of a drift thickness W_D of MOSFET. The V_m of IGBT is also a function of W_D, but it is not explicitly proportional to a current density, different from MOSFET's case. V_m is the function of the carrier lifetime of a high level injection, in which both the carrier lifetime of electrons and holes are equal and long enough to maintain the conductivity modulation effect. So V_m value is apparently smaller in the medium voltage class of 600V, and it is roughly estimated around 0.2V much lower than V_{drift} of 5V and more in the same voltage class MOSFET.

In contrast, IGBT's V_{pn} is also quite larger than MOSFET's $V_N{}^+{}_n$, which is negligible small value in the medium and high voltage class. The V_{pn} as the built-in potential of the PN junction is in a range of 0.55 to 1.1V for Si material

Although R_{drift} is uniquely defined as the function of the N-drift doping concentration and thickness for the BV voltage class, V_m is freely designed along the application requirement as the function of carrier lifetime in the V_{on}-E_{off} tradeoff. The condition of $d = L_a$ makes the almost symmetric catenary shaped carrier distribution. For both electron and hole, the ratio of the ascending slope is equal to be balanced. This condition is one of the well-balanced cases for the V_{on}-E_{off} tradeoff. And, it is easy to choose the optimum point from the V_{on}-E_{off}

tradeoff curve to fit the application usage.

Mathematical calculation for an inductive load E_{off} is not so important to discuss here. The most major part of Eoff is the tail period, which strongly depends upon the carrier lifetime. So, only I_{tail} (tail collector current of IGBT) and t_{tail} (tail time of IGBT) are described as the followings.

$$I_{tail} = Ic\ \alpha_{pnp}\ ,$$
$$t_{tail} = \tau_{HL}\ \ln(Jc_{(judge)}\ \alpha_{pnp})$$
$$\alpha_{pnp} = \alpha_T\ \gamma\ ,$$
$$\alpha_T = 1 / \cosh\ (W_{undepl} / L_a)$$

where, α_{pnp}, α_T and γ are a transistor gain and a base transport factor of the parasitic PNP transistor (but up-side-down configuration comparing with IGBT operation) and their correlation factor, which seems to be a unity as the convenience, respectively. I_c is the starting absolute current value [A] to be turned-off, but $Jc_{(judge)}$ is the current density [A/cm^2] defined as the criterion for turn-off completed so as to be 1/10 or 1/100 for the convenience. W_{undepl} is an undepleted thickness [cm] of a neutral charge region being applied the V_{cc} (constant collector voltage supply) during the turn-off time period in case of an inductive load. And, the easy approximation is supposed to be W_D (N-drift thickness) is twice of L_a, and W_{undepl} is a half of W_D.

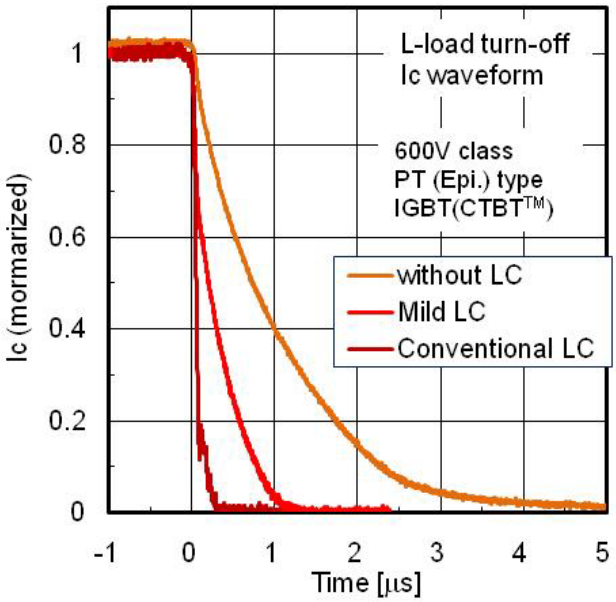


Fig. II-3. Turn-off Ic waveforms of PT type IGBT with/without LC (carrier Lifetime Control)[28][29][30]

Experimental Itail characteristics of 600V class IGBT (CSTBT™) of PT type are shown in Fig. II-3[28][29][30]. In PT-type IGBT, N-buffer and N-drift layers are epitaxially crystal grown on the highly doped P-type substrate. Without carrier lifetime control, IGBT has a large and long tail current shown in Fig. II-3. This I_{tail} is almost same as the start Ic and t_{tail} is very close to 10μs, which is the standard value of the "just after" wafer process. The conventional LC (carrier Lifetime Control) condition reduces I_c down to almost zero during 0.2μs or so. So the carrier lifetime of both electron and hole would be 0.2μs corresponding to t_{tail} down to zero.

As the mentioned above, I_{tail} also strongly depends upon the carrier lifetimes of electrons and holes, which are basically uniform but sometimes locally controlled through the special carrier lifetime controlling

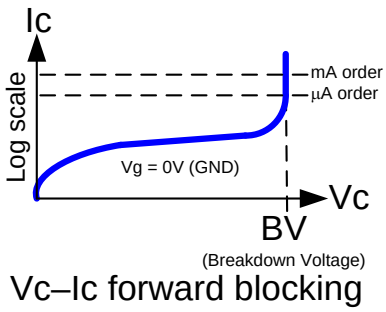
methods. The carrier lifetime control has been the main stream until now. Recently adjusting the p-collector dosage of the wafer/chip backside comes to be major for the LPT type devices because of the backside ion implantation technology easily applying.

This is the explanation of the step two. Before discussing about the SOAs as the very hard condition of the dynamic characteristics, the more moderate condition of the standard switching test and specification as the dynamic characteristics is explained in the next three sections II-3,4,5. It is started from the standard DC static characteristics of II-3.

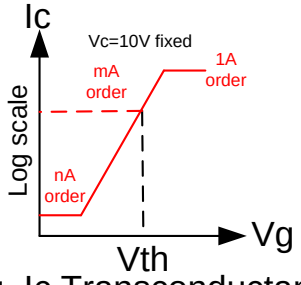
II-3. Static characteristics : BV, V_{on} and V_{th}

The followings are the industrial specifications for the static (DC) and dynamic (transient) characteristics in the measurement of three terminal power semiconductor device such as IGBT, which has N-type Emitter (E), P-type Collector (C) and MOS control gate (G). In this paper, basically all the MOS gate devices are treated as the N-channel type device, in which Gate is both structurally and electrically located close to the N-emitter to open and close the channel.

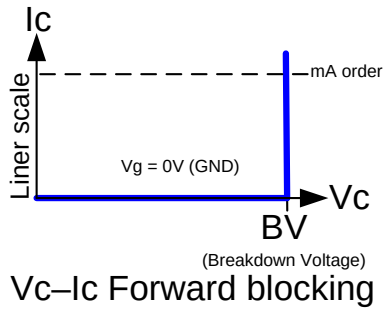
Three major static characteristics are shown in Fig. II-4. These characteristics are commonly called as *BV*, V_{on} and V_{th} (gate threshold Voltage).



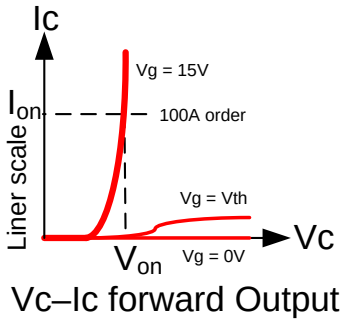
(a-1) BV in logarithmic scale



(c) V_{th} usually in logarithmic scale
E:GND, C:+10V fixed, G:swing



(a-2) BV usually in linear scale
E & G:GND



(b) V_{on} in linear scale
E:GND, G:0 to +15V fixed

Fig. II-4. Three major static characteristics of three terminal power device such as IGBT

BV is the V_c-I_c forward blocking characteristics, and its main pn junction of P-body / N-drift is reverse

biased. So, *BV* is sometime called as the reverse characteristics. But strictly speaking, the reverse blocking capability is characterized by the backside P-collector / N-drift (or N-buffer) junction.

BV characteristic is usually described in a linear scale like Fig. II-4 (a-2). So the breakdown seems to be abrupt and straight. In a manual method of using a "curve tracer" machine, *BV* is measured by a method of "V-force / I-measure", which is the successive measurement of a device leakage current as the function of increasing the applied voltage. In this manual case, when the applying voltage accurately reached the physical *BV* point, the chart like Fig. II (a-2) would be obtained. The power supply as a measurement facility is also limited for a supplying electrical power for DUT (Device Under Test), and the limit of power supply for kV class is usually very low around mA range. So the measurement rage is limited very close to the horizontal axis of V_c. And, all the mass production devices have a little larger *BV* value defined by the voltage class such as 1200V in the specification sheet. Physically, *BV* curve is divided into two part at least, the diffusion current region before *BV* point and the avalanche current caused by the impact ionization effect close to and at *BV* point. Even in the avalanche phenomenon, its state is steady and reversible as far as isothermal condition is maintained. So, the device never breaks or is destroyed "at" the *BV* point.

V_{on} is the forward voltage drop as shown in Fig. II-4 (b). V_{on} is commercially defined at the rated current with the gate bias of +15V. But, strictly speaking, the definition of this rated current $I_{c(rated)}$ is not standardized. One of the reasons is the $I_{c(rated)}$ strongly depends upon the chip size and rated voltage class. For the convenience, the $I_{c(rated)}$ or simply I_{on} of this study is supposed to be 100A in $1cm^2$ chip active area, which corresponds to the rated current density $J_{c(rated)}$ or J_{on} being $100A/cm^2$.

V_{on} is usually characterized as the Vg = +15V curve in Fig. II-4 (b), and the reason is the following.

The curve at V_g = 0V in Fig. II-4 (b) is identical to *BV* curve. The $V_g = V_{th}$ curve is schematically described in Fig. II-4 (b). But, in the real measurement, the $V_g = V_{th}$ curve is not clearly seen in the real linear scale, because the ON state current of $Vg = V_{th}$ is in the range of 10mA as shown in the next Fig. II-4 (c). Same kind of the power supplying limitation as the *BV* case exists in this V_{on} measurement, in which 100A class current source usually cannot supply higher voltage than 10V. So the measurement rage is limited very close to the vertical axis of I_c. So, V_{on} is measured in case of V_g = +15V at Ic(rated).

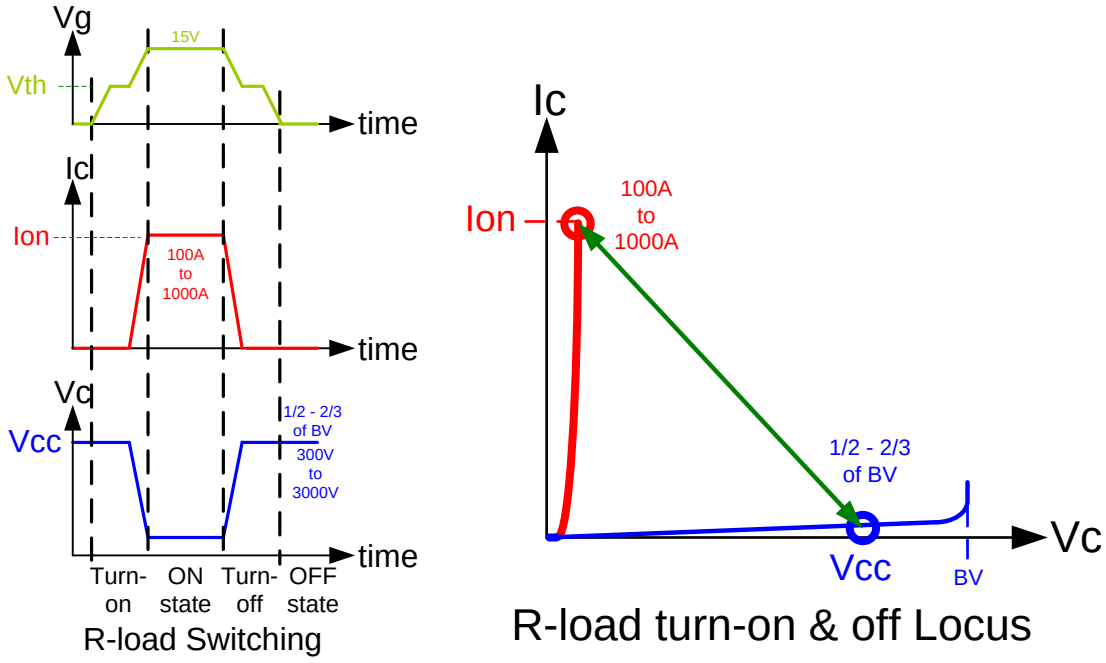
Furthermore, the shape of V_{on} curve of V_g = +15V is neither ohmic (constant resistance) nor saturated (resistance increasing with current increasing). The higher the current density is, the lower the resistance is. This is because a conductivity modulation effect.

V_{th} definition has a variety in the commercial phase, one of the standard way is V_c = 10V fixed and V_g sweeping from zero to until the ON state current value reaching the 1/10000 of the rated current $I_{c(rated)}$ or I_{on}. As shown in Fig. II-4 (c), V_g-I_c transconductance characteristic of MOS gate device IGBT is logarithmically simply increasing. In this V_{th} measurement, same kind of effect as the *BV* case is observed in the linear scale (not in figure). So V_{th} seems to be the turning point between ON and OFF states.

These are all of the static (DC) characteristics with physical meanings. The next sections of II-4, 5, 6 will explain the dynamic characteristics.

II-4. R (resistive) load switching

Under the constant DC voltage supply of V_{cc}, the rated current I_{on} is simply turned on and off by the gate signal as shown in Fig. II-5 (a). In the turn-on, once V_g goes up to the V_{th} value, the N-channel starts to be created. After a gate charge Qg charged by V_{th} reaches the enough value to allow the electron to fill the drift region though the channel, the main current flow corresponds to the V_g value. The turn-off sequence is simply opposite action. So, the switching locus is also simple as shown in Fig. II-5 (b). Both turn-on and turn-off locus go and back along the same load curve directly connecting the V_{cc} point in the *BV* curve of Fig. II-4 (a) and the I_{on} point in the V_{on} curve of Fig. II-4 (b). As long as stray inductances in the R-load switching circuit are small to be negligible, the switching device in the R-load circuit does not care about SOA at all as far as all the DC test listed in the above section II-3 being cleared.



(a) (b)

Fig. II-5. Resistive (R) load switching characteristic of IGBT

The most part of the power MOSFETs, which are in the 3 terminal package such as TO-220 or TO-3P of the low and medium power range, are used in this R-load switching category, shown in Fig. I-1 and I-2, for example, power supply and DC-DC converter. And the low power IGBTs are also in the same R-load switching category. So, there is no need to certify the RBSOA and/or SCSOA for the power MOSFET in this R-load switching usage category. Actually, the word of RBSOA and SCSOA are not in the specification sheet of power MOSFET. They only have a UIS (Unclamped Inductive Switching) capability instead of RBSOA, but the definition is apparently different from each other. This UIS capability is sometimes called as "Avalanche" capability, which is very similar naming of the avalanche break down for all the power devices or the avalanche endurance of diode device. This confusing situation of "Avalanche capability naming" and "without RBSOA and SCSOA description" is one of the reasons why, even in the power device users, technical

terms are not standardized and different from each other between power MOSFET users and IGBT module users.

This R-load switching is the fundamental characteristic, but it is not necessary to be intensely discussed for the power module application as the IGBT device.

The next section II-5 of the inductive load switching is the major usage and very important category of IGBT.

II-5. L (Inductive) load switching

The L (inductive) load switching, which stands for the motor drive circuit (Fig. II-7) as the main usage of medium to high power IGBT module, is very important category of IGBT, because this switching locus are tightly correlated to the FBSOA and RBSOA as shown in Fig II-6.

L-load switching waveform is quite different from R-load case, because the inductance L has 3 strong characteristics comparing with resistance R.

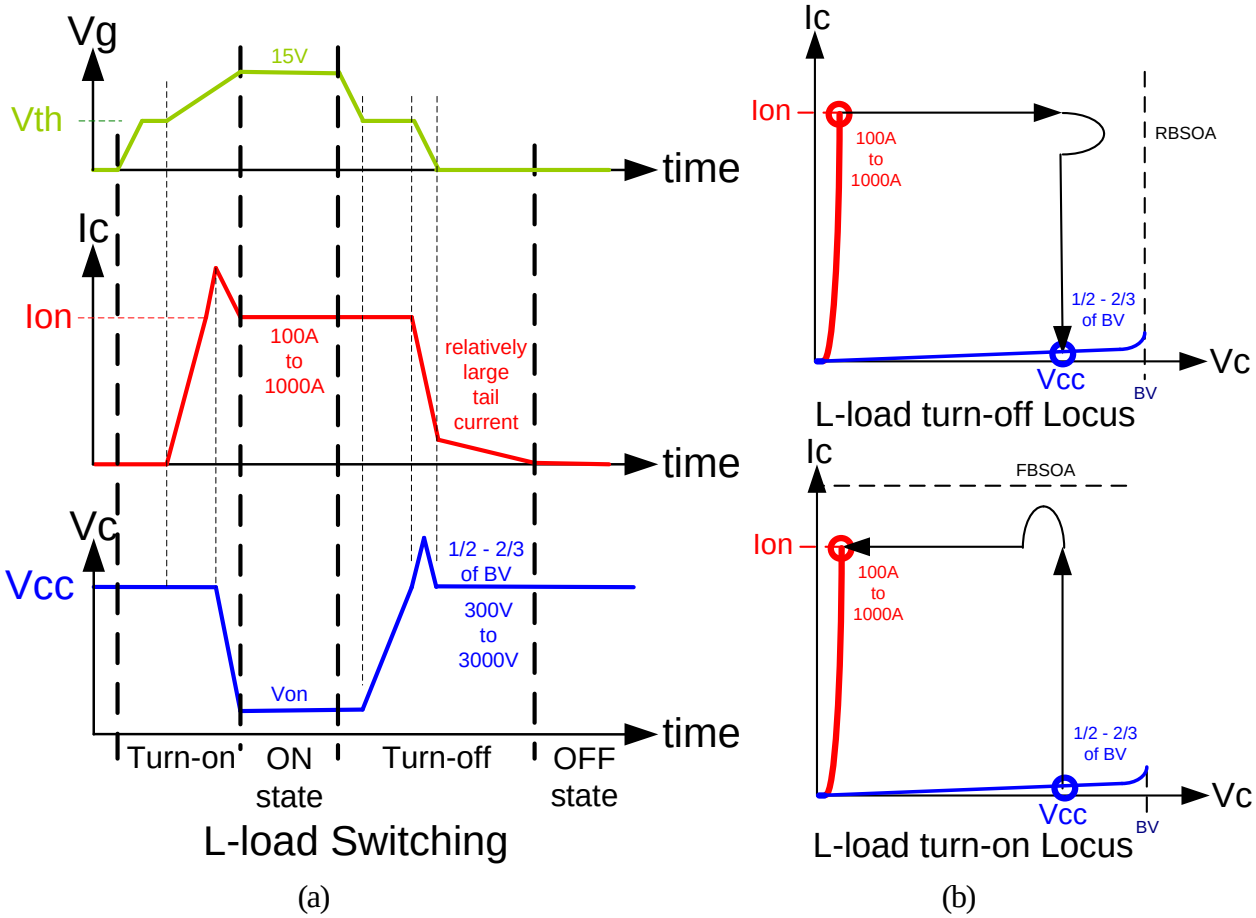


Fig. II-6. Inductive (L) load switching characteristic of IGBT

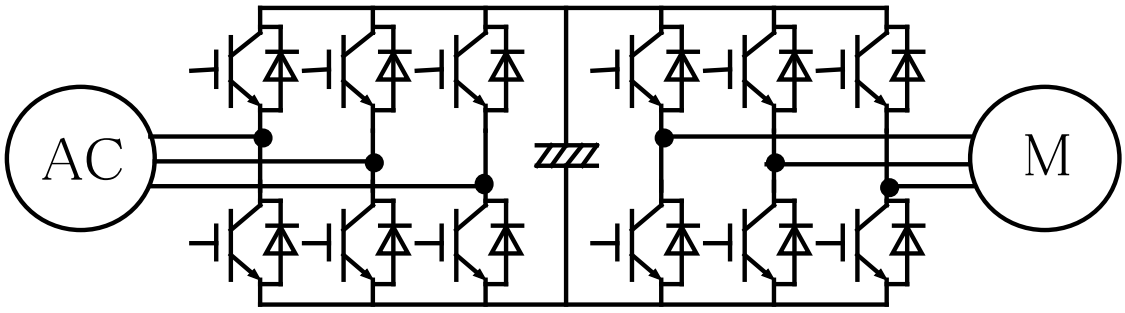


Fig. II-7. Converter/Inverter circuit consist of IGBT and FWD (Free Wheel Diode) as the motor drive usage

The first inductance characteristic is causing a time phase shift between V_c and I_c, as shown in Fig. II-6 (a). During the turn-on time period, after the V_g reaching the V_{th} and starting to ascend, Ic rises up to the I_{on} and more, and then *Vc* starts to descend down to the V_{on}. During the turn-off period, after the *Vg* goes down to the V_{th}, V_c starts to rise up to V_{cc}, and then Ic starts to descend.

The second inductance characteristic is electrical energy storage, I^2L. Even after the turn-off moment of the IGBT, an L still has some large electrical energy stored in itself. So the bridge circuit or inverter circuit has a ventilation part or circulating part such as a FWD (Free Wheeling Diode), which is coupled with IGBT in an anti-parallel for all the inverter arms, as shown in Fig. II-7. Just after the Ic reach through the I_{on} in the turn-on sequence, I_c goes up to one more large value originated from the FWD's reverse recovery. So, the large over-shoot current successively appears in the turn-on I_c waveform as shown in Fig. II-6 (a). So, the turn-on locus (Fig. II-6 (b)) has a hump in the direction of Ic increase. If this I_c over-shoot value will touch a certain large value, the device will be unable to come back to the normal track of turn-on locus. This dangerous I_c value is defined as the FBSOA boundary (I_c), which is called as the "ON state blocking voltage" in the LSI field.

The second inductance characteristic is "induction" voltage serge V_s, V_s = - L dIc / dt. During the turn-off sequence, an average value of Ic decreasing slope creates a relatively large V_s as shown in Fig. II-6 (a). In the turn-off locus (Fig. II-6 (b)), V_c curve also has a hump in the direction of *Vc* increase. Same as the turn-on locus, If the this voltage serge will reach a certain value, the device shall be unable to be survival. This V_c value is the RBSOA boundary.

Here rise questions whether the RBSOA boundary (V_c) of the transient characteristic is same as the *BV* of the static characteristic or not, and whether the FBSOA boundary (I_c) of transient characteristic is same as the I_{sat} of the static characteristic or not. This idea is going to be the purpose of this study.

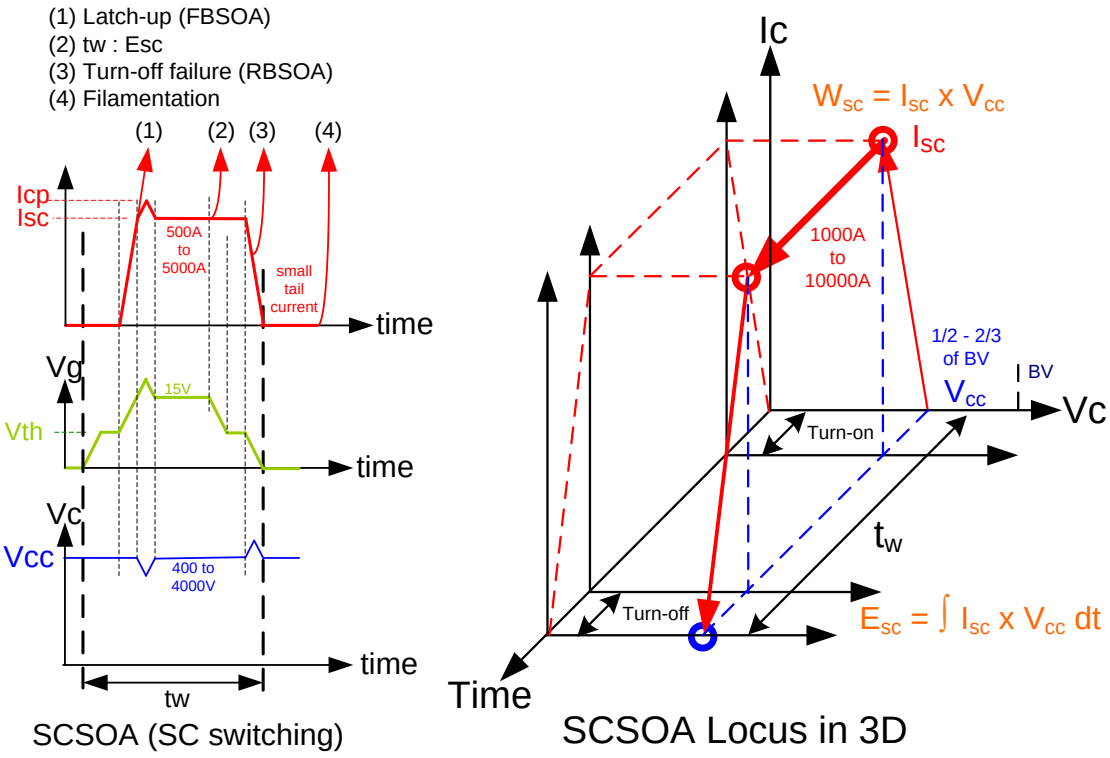
In the next section II-6, the third and hardest SOA, SCSOA, is explained as the combination of FBSOA and RBSOA with one more factor of the time integral.

II-6. SCSOA

SCSOA is the hardest category of SOA, therefore SCSOA is the most important characteristic of power semiconductor device to handle the large electrical power.

I_{sc} is I_{on} when V_{on} is V_{cc}, 2/3 of *BV* class. In Fig. II-8 (a), I_{sc} is the constant collector current after the peak current of I_{cp} (collector current peak during load shorted circuit operation) induced by the small stray L.

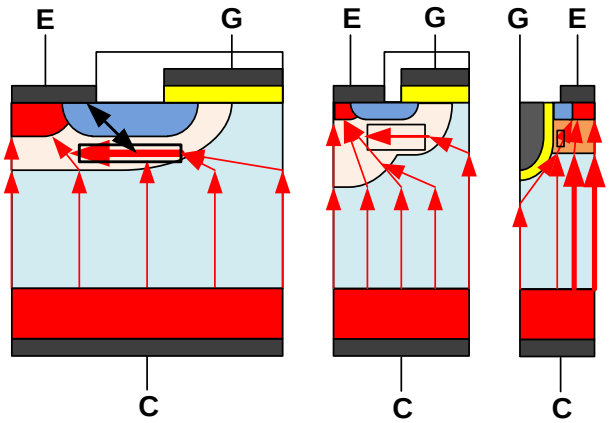
The SCSOA has a more complex situation than FBSOA and RBSOA, as shown in Fig. II-8 (b). As a load shorted case, there is one more tough regulation for SCSOA to maintain t_w (an endurance time width). t_w is usually 10μs for the enough time length to be cut off the main power flow by an independent protection circuit from the power module gate drive circuit.



(a) Four failure modes of SCSOA (b) SCSOA Locus in 3D description

Fig. II-8. SC (Short Circuit) switching characteristic of IGBT

There are four fundamental destruction modes in the SC mode switching. In addition to the combination of FBSOA and RBSOA, it should have a sufficient energy endurance E_{sc}, which is a time integral of the product I_{sc} x V_{cc}, or an enough time endurance t_{sc} as shown in Fig. II-8 (b). From the energy endurance point of view, SCSOA is not an area of power (W) but a time integral of energy (J) as shown in Fig. II-8 (b).



(a) Coarse patterned planar gate (b) Fine patterned planar gate (c) Trench gate

Fig. II-9. FBSOA failure mechanism : the parasitic NPNP thyristor action, "latch-up"

In the power module structure, the heat dissipation is strictly limited by the assembly structure such as a solder die-bonding between the power chip and the base plate. Duration of 10μs is not so long to propagate E_{sc} from the semiconductor chip to the heat sink in the power module structure. As an adiabatic condition, this E_{sc} of Si device is almost uniquely limited by the silicon material characteristics. So it is also directly regulated by the thickness of chip. As far as the supply voltage V_{cc} is constant in the general application, there is an only solution to enlarge t_w for devices to maintain I_{sc} (current flowing during SC mode switching) sufficiently low.

About the FBSOA category, schematic models for the thyristor mode "latch-up" phenomena at the initial stage of SC switching (Fig. II-8 (a)) are shown in Fig. II-9 for three structures of IGBT, the coarse patterned planar gate (a), the fine patterned planar gate (b) and the trench gate (c). To simplify the operational model, only the hole current of SC-mode $I_{h(SC)}$ is described as the red arrow. The thicker arrows correspond to the higher current density. When the large $I_{h(SC)}$ (hole current in SC mode switching) flows underneath the N^+-emitter region inside P-body (P-type Channel Dope region) of MOS gate structure, it causes the $V_{p\text{-}body(SC)}$ (Voltage drop cause by hole current flowing inside a P-body underneath the N^+-emitter) by the product of the current and resistance $R_{p\text{-}body}$. When $V_{p\text{-}body}$ rises up to $V_{built\text{-}in}$ (= 0.55Vor so), the N^+-emitter and P-body junction are forward biased to be turned-on without the MOS gate control.

$$V_{p\text{-}body} = R_{p\text{-}body} \text{ X } I_{h(SC)} > V_{built\text{-}in}$$

Once this direct electron current flow occurs from the N^+-emitter to the P-body, the SC-mode large current $I_{h(SC)}$ also directly flows into N^+-emitter without gate control. This N^+-emitter, P-body, N-drift and P^+-collector direct current flow is the NPNP thyristor action. The current is uncontrollable. This abnormal state is called "latch-up". If the current flow length is short or the P-body doping concentration is high enough, $V_{p\text{-}body}$ could not reach $V_{built\text{-}in}$ during the SC current flowing. In case of the fine patterned planar gate (b), the $R_{p\text{-}body}$ is smaller than the coarse patterned planar gate because the small length of P-body region and is also partially highly doped by the superimposed of another deep P-well diffusion. In the trench IGBT structure, the length of hole current path inside the P-body region is much shorter than the fine patterned planar gate case, as shown in Fig. II-9 (c). Moreover, in the trench gate structure, the vast majority of Isc directly flows into P^+ region through the P-body avoiding the path underneath the N^+-emitter also shown in Fig. II-9 (c). So the optimized trench gate IGBT of the present generation never shows the "latch-up" action, and is free from the first destruction mode even during the SC switching.

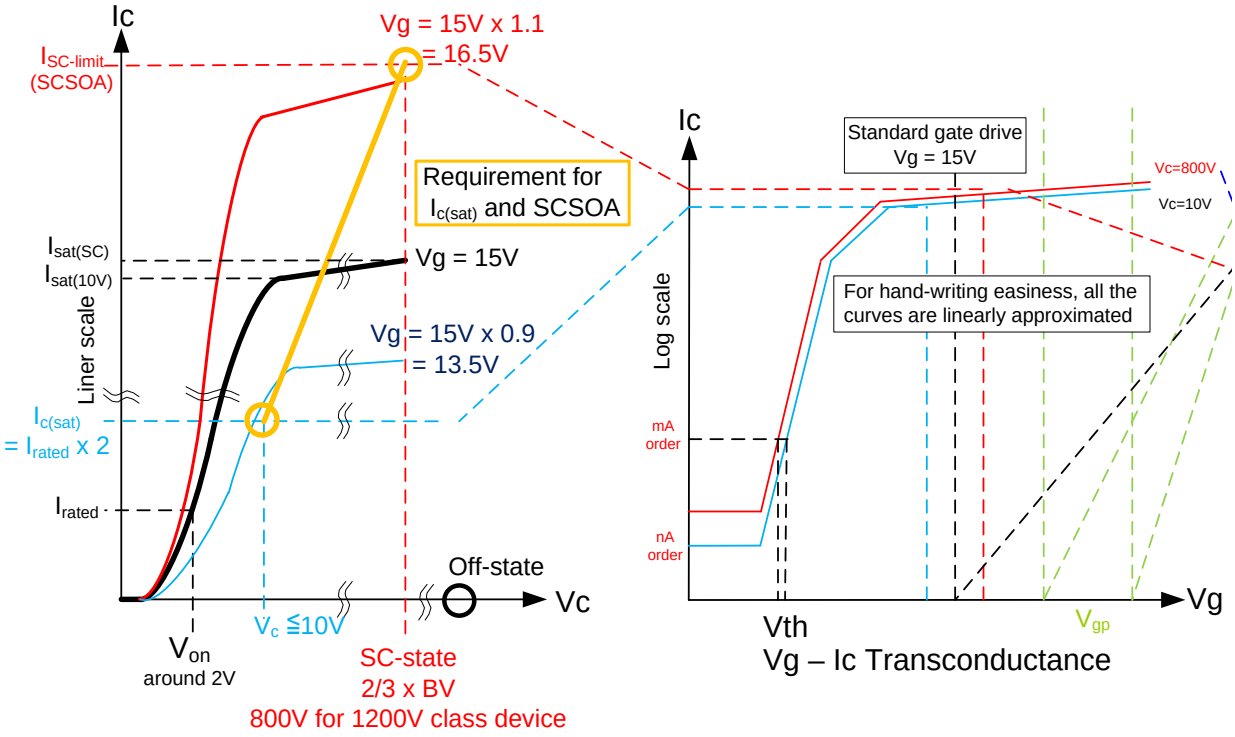
During this load-shorted SC mode switching (Fig. II-8), the mode (3) turn-off failure has a slight chance to hit the RBSOA boundary, because the stray inductance is very small not to induce large voltage serge as far as the load-shorted. The turn-off failure current simply might exceed the RBSOA boundary with set V_{cc}.

Considering above two modes of "latch-up" or "turn-off failure" (Fig. II-8 (a)) being not so severe problems in the T-IGBT, the present issue of SCSOA is simply the interpretation as the E_{sc} limit as far as device is uniformly fabricated without any defects in the fabrication wafer process.

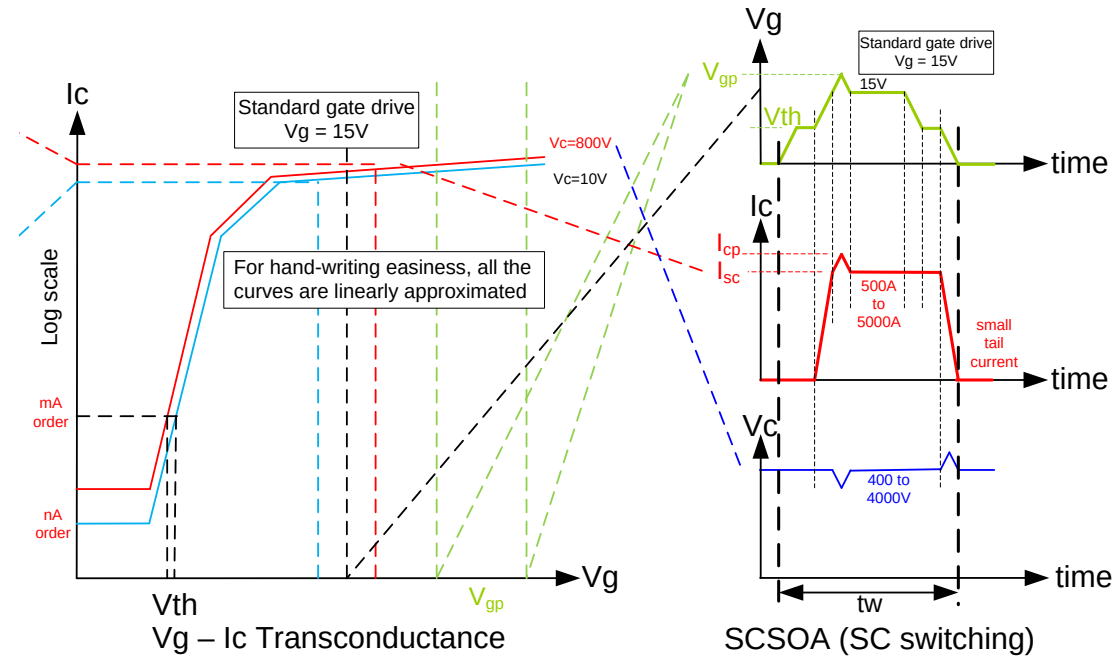
The described above is an overview of SC mode switching, and the index of the direct measurement is t_w. And the interpretation from t_w or E_{sc} as the dynamic characteristics to the DC characteristic of I_{sat} would be used to maintain the sufficient SCSOA. This issue is discussed in the next section II-7.

II-7. I_{sat} as the index of SCSOA

To guarantee this heavy characteristic of SCSOA, there are some efforts to find out the static measurable characteristics as the index. One of the major items is I_{sat}. This category is too complex. The explanation will be done step by step using Fig. II-10. Chart (b) is used in both rows to explain the relationships.



(a) Forward output V_c-I_c characteristics up to SC state (b) Vg-Ic transconductances for low and high V_c



(b) same figure as the above (b) (c) same SC switching figure as II-8 (a)

Fig. II-10 Isat is the index of SCSOA

In Fig. II-10 (a) (b) (c), correlation between SCSOA as the dynamic (transient) characteristics and I_{sat} as the static (DC) characteristics are described. The physical meaning of I_{sat} (saturation current) is same as the FBSOA boundary at a certain V_c value. In contrast, as the test result, I_{sat} is usually measured at the condition of V_g = 15V (standard gate drive voltage) and V_c = 10V (standard voltage coming from the traditional IC standard). But even in a low V_c value of 10V, I_{sat} is several times larger than the rated current value, because V_{on} of the rated current is only 2V for 1200V class device, as shown in Fig. II-10 (a). IGBT's I_{sat} will never saturate up to *BV*. Of course, the increasing rate is small in high voltage region over V_c = 10V. But, strictly speaking, I_{sat} of IGBT never saturates because of its bipolar action, which is strongly affected by the backside P-collector's hole injection, which causes both the conductivity modulation and the direct hole current flow from P^+-collector to P^+-Contact portion of P-Body in the MOSFET region. This IGBT's unsaturated characteristic is very different from the unipolar device MOSFET, in which only the majority carrier electron is provided through the MOS channel region without any backside injection. However, mentioned above, over V_c = 10V range, I_{sat} has a very strong saturation tendency, so it is no problem to suppose that I_c value at V_c = 10V is I_{sat}, which is twice or less smaller than the real I_{sat} value in the SC operational mode. In addition, V_c = 10V is traditionally standardized value and easy for the standardized measurement equipments for the traditional IC and power devices.

V_{gp} (V_g peak) is induced by an extremely large dIc/dt during the beginning time period of the SC mode. Both I_{cp} and I_{sc} should also be inside of the FBSOA and RBSOA.

So, one of the practical solution to reduce E_{sc} is to control I_{sc}. But I_{sc} is a result and not a cause. In the mass-production phase, $I_{sat(10V)}$ as $I_{sat(SC)}$ is measured in the low current density of DC test mode. For example, I_{sat} is defined the current value, when V_{ce} is fixed at low enough value 10V, and V_g is set forth a certain value of higher than V_{th} but lower enough than the usual operational voltage of 15V, as shown in Fig II-10 (a) and (b).

This is the reason why IGBT, which is usually used in the L-load circuit, has the specifications of FBSOA, RBSOA and SCSOA. In contrast, MOSFET, which are mostly used in R-load, does not intentionally care about these SOA characteristics.

As the translation result from the dynamic characteristic of SCSOA to the static characteristic, I_{sat} is good index to evaluate SCSOA. But, it needs one more step to be translated from I_{sat} to another easily measurable characteristics listed as the static characteristics in the section II-3, only the three characteristics are there, *BV*, V_{on} and V_{th}. In the next section II-8, using V_{th} as the index, I_{sat} measuring and controlling method is explained.

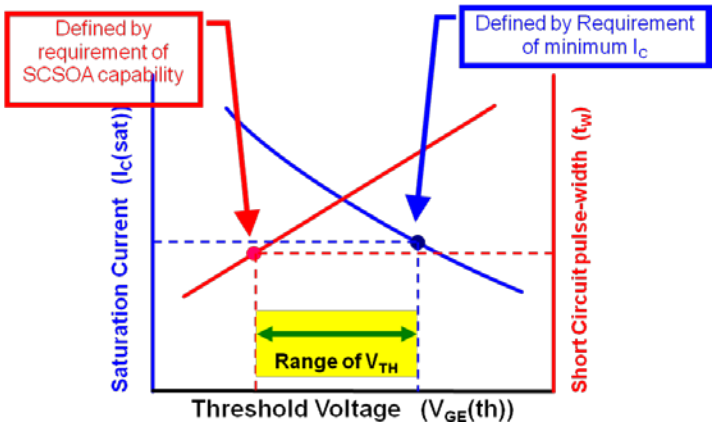


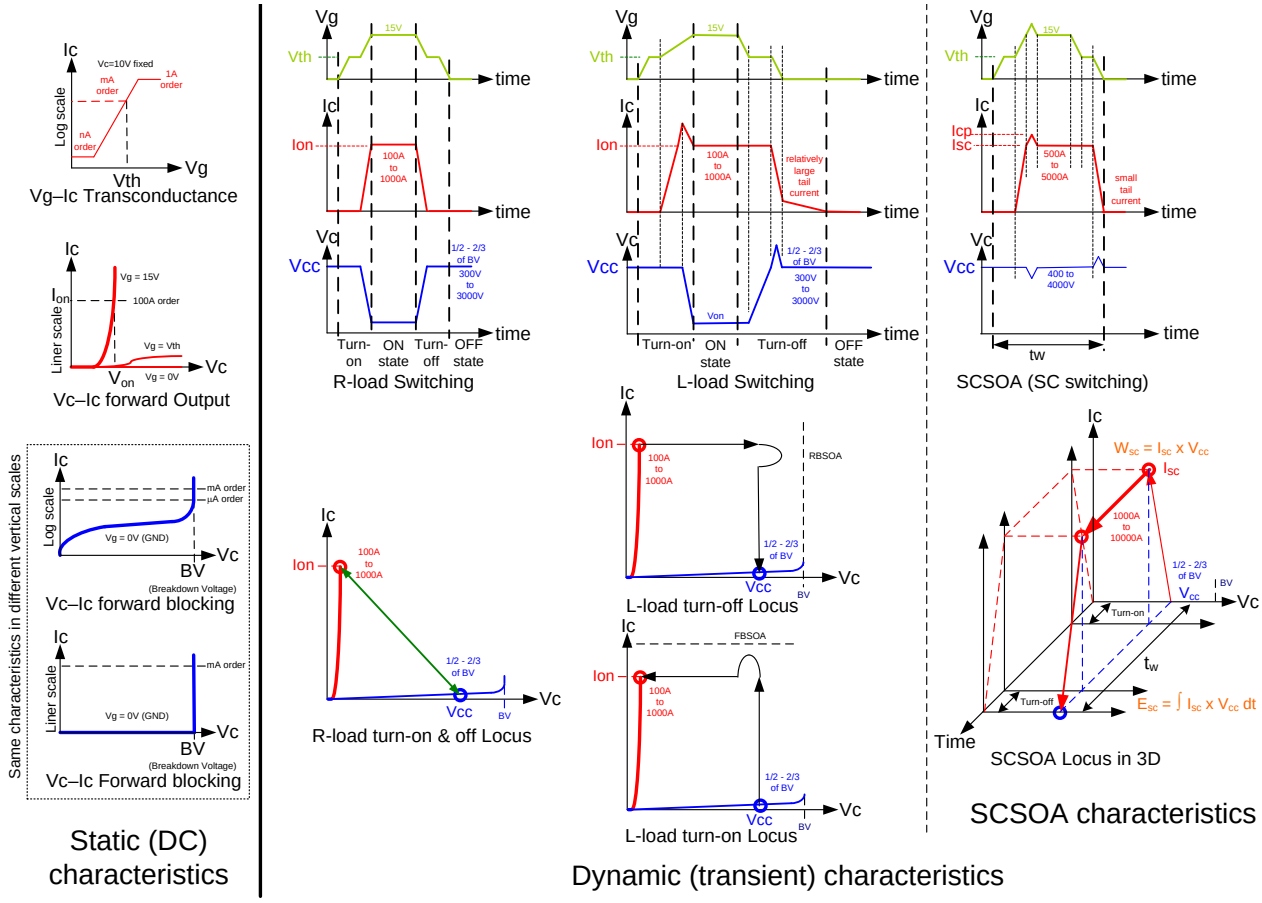
Fig. II-11. Schematic description for the acceptable range of V_{th} ($V_{GE(th)}$) in the mass production phase

As the index of SCSOA, V_{th} is also used as the index of I_{sat} as the measurable characteristic. It needs one more explanation about the I_{sat} as the IGBT module product specification. I_{sat} has another confliction to maintain I_{sc} as low as possible. The conventional users of the power modules require the $I_{c(sat)}$ to maintain twice the rated current Ic(rated) or I_{on} even at the condition of the 90% of V_g (= 13.5V) applied. There is another independent tradeoff I_{sc} (or t_w) and $I_{c(sat)}$ as shown in Fig. II-11.As the mentioned above, I_{sat} should be as small as possible to maintain SCSOA t_w being longer than 10μs. But here is another regulation for I_{sat} to be large enough to maintain a certain value.

One of the good "measures" is V_{th}, as shown in Fig. II-11 for both SCSOA (t_w) and $I_{c(sat)}$. According to this relationship, the minimum – maximum range of V_{th} was defined for the mass-production phase. This Fig. II-11 is the interpretation of the I_{sat} of Fig. II-10 (a) to the V_{th}. So, V_{th} is good "measures" for both SCSOA and requirement of $I_{c(sat)}$..

II-8. Summary of the static and dynamic characteristics

The characteristics discussed in this paper are summarized in Fig. II-12 to catch the entire relationship each other at a glance. Fig. II-12. is composed of 4 parts, static characteristics, R-load switching, L-load switching and SC-mode switching, as explained in the previous sections.



(a) Static (b) R-load (c) L-load (d) SCSOA

Fig. II-12. Schematic charts as the summary for the fundamental characteristics of the power semiconductor devices

II-9. Triangular tradeoff, V_{on}, E_{off}, and SOA

As explained in the above sections, FBSOA and RBSOA are closely related to the forward conducting characteristics and the turn-off characteristics, respectively. For easy example, if the device were thick enough to have one rank large *BV* characteristic, the device would have larger SOA and worse V_{on}-E_{off} tradeoff than the conventional device. The optimization of SOA is sometimes opposite to improve this fundamental tradeoff of V_{on}-E_{off}. FBSOA is defined as how large current could turn on without any latch-up phenomenon, and RBSOA is defined as how large current could turn off as far as the serge voltage has not reached the *BV* value. So, the whole relationships are shown in Fig. II-13.

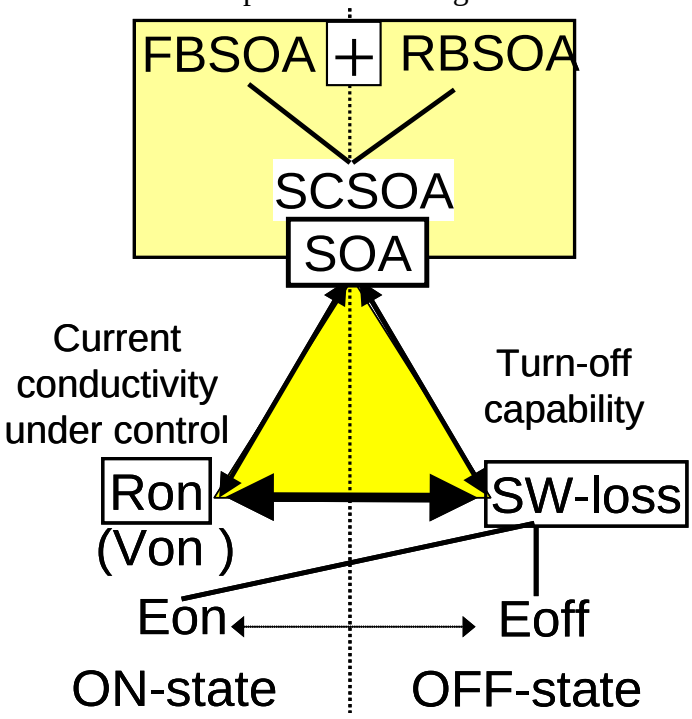
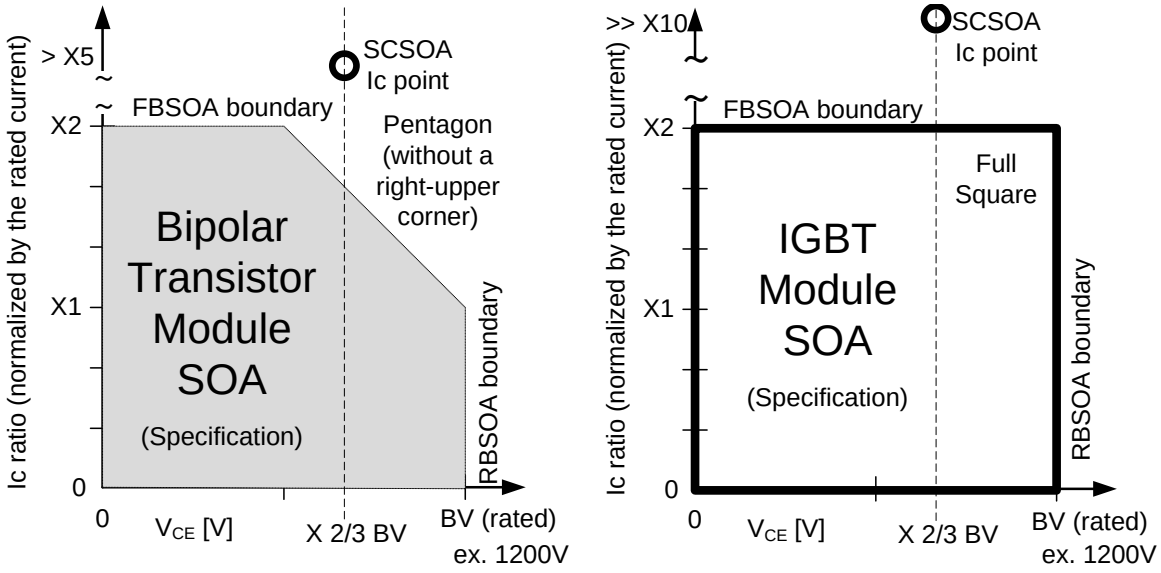


Fig. II-13. A detail of the "Triangular tradeoff relationship" for in the L-load usage[6]

II-10. SOA on the definition between the physical meaning and the industrial specification

Returning back to SOA on the definition between the physical meaning and the industrial specification, it should be considered how large the power semiconductor devices handle the electrical power (P = V x I). So the non-destructive characteristic, "tough", is the first priority before the fundamental characteristics of the saving the electrical power losses. As an industrial standard, an SOA is strictly defined in an individual specification sheet. In the V_c-I_c plane as shown in Fig II-14, the SOA is literally specified as an area described by the FBSOA boundary and RBSOA boundary, which are named after the bipolar transistor module's definition of the previous era. Strictly speaking, even now, there are several naming (dialects) for these SOAs, and measurement conditions are not standardized and have been still under consideration.

Traditionally, maintaining the sufficient SOAs, it has been usual to add a large margin of *BV* characteristic with not a small sacrifice of the fundamental power loss characteristic. Corresponding to the tight requirement for cost and performance, a tough situation arises to improve the power loss characteristics to maintain the same SOA levels as the previous generation having a large margin for its design.



(a) A traditional bipolar transistor power module case **(b)** an IGBT module case

Fig. II-14. Schematic example of the SOA for power module (not a chip specification)

Industrial definitions for both FBSOA and RBSOA are the historical indexes for the traditional discrete NPN or PNP bipolar transistor, which has a large voltage decreasing portion in the high current density region because of the secondary breakdown phenomena. That is easily overcome by the recent bipolar device like IGBT. The specification is the turn-off the twice of rated current. From the following points of view, however, that RBSOA test has been still effective. The first one is the excess serge voltage induced by the inductance, - L x dI/dt against *BV* of device. The second is the operational temperature elevation by the large power loss caused by the self clamping mode in the parasitic PNP transistor's sustaining mode operation. Taking account into all the cases, the turn-off capability in the inductive load should be evaluated to define the current rating for a certain structure of device in the R&D phase. It has been expected to estimate that kind of turn-off capability through the numerical simulation especially in the R&D phase.

As shown in Fig. II-14 (a), the bipolar transistor module's SOA is described as the pentagon shape cutting the "right-upper" corner of a square shape. The IGBT module as the new comer in the power electronics field does not have such a degradation area (Fig. II-14 (b)), and is very SOA-tough product as a catch-copy. This is true as the industrial point of view, and the well-tempered latest IGBT chip is clearly tougher in all the directions than the conventional bipolar transistors. It is also emphasized that this schematic SOA description is for the large current scale module taking account a chip parallel usage and module parallel usage not as the naked power chip.

In the late 1990's, a numerical device simulation had been slowly applying for power devices almost ten years later than a LSI region, because the following complexities lay down, for example, an extremely wide range of the voltage and the electrical current from the OFF state (kV and nA) to the ON state (V and kA), a floating N-buffer region and an extremely large aspect ratio of the unit cell structure (μm wide and several hundred μm depth).

In frontier of the device R&D, a steadily but slowly "cut and try" method has been still major for the evaluation of various SOAs. There is a high risk of the device destruction or the literally explosion in case of a

failure during an inductive load turn-off, which contains a large electrical energy stored in an inductive load. The large V serge also appears during RBSOA evaluation. The huge electrical power of SCSOA evaluation reaches beyond kilo-watts to mega-watts during the stand-still time of ten micro-seconds, in which device would endure. Usually there is no evidence left behind in case of switching failure. Only the practical way to find out the point of no return is increasing the voltage and/or current and/or time step by step as fine as possible. After this dangerous effort to evaluate the destruction limit in a certain condition, only a single point could be obtained in the V_c-I_c plane. This is not only ineffective but also dangerous for a DUT, measurement facilities and especially for a person who engages in this evaluation procedure.

In addition, the test specification, which would be the preliminary selection procedure for the fair chip from the NG chip, was not so clearly fixed because of difficulties of a super-perspective sight from the low power static characteristics to the high power dynamic characteristics such as an inductive load switching and SOA. Moreover, there are many hindrances of the various kinds of defects during the fabrication steps or inside a crystal itself.

If there were no dusts and no defects in the power chip, how large the SOA would be ? First of all, what kind of shape the SOA would have ? Is there any way to estimate SOA, which is a summation of a transient characteristic during the extremely short instance, through static characteristics ? At least, it is necessary to certify the SOA as the literal area in the first quadrant of the V_c-I_c plane. Without obtaining the description of SOA, the "traditional" evaluating procedure of SOA for a single chip is extremely inefficient.

It was necessary to find out the exit from this compromising situation. Using the numerical simulation, the SOA should be estimated at least semi-quantitatively.

There are several analytical approaches to estimate the maximum controllable current density J_{mcc} and very detail experimental approaches for the high voltage device being used in the special application like a HV power line from the device user's point of view. There is no analytical expression for the shape of the SOA in the V_c-I_c plane not only because of being under-covered by the industry but also because of too large power (W) and energy (J) experimentally not avoiding the burst condition. So, the method of guarantee the SOA has been strongly depending upon the experiences.

But it might be possible to visualize the SOA shape and to find out a method to improve SOA.

The numerical simulation shall calculate until any large current density as far as an operator will not give up. Of course, there is a know-how to continue the unusual calculation, but it is not impossible.

One of the most important characteristics of power semiconductor device is “not to fail”, to withstand without destruction in any emergency condition in the real circuit operation. Sometimes, a small hang-up is acceptable for personal computer usage, but an interruption is not acceptable for the home appliance facility like a washing machine or refrigerator. The author would never like to assume the emergency interruption for the automotive, train and especially airplane. Before the long term reliability, even a single event should be strictly prohibited for all the power semiconductor devices. This is the reason why SOA is the most important characteristics for our power semiconductor devices.

II-11. Purpose of this research

If SOA would be a limitation of a dynamic characteristic, it could not be beyond the limitation of a static characteristic. The curve obtained from the numerical simulation up to the high current density would be identical as the SOA boundary of the transient dynamic characteristics. For example, RBSOA indicates the turn-off capability in the condition of high current density and high voltage.

My motivation is to visualize the SOA shape as an area in a V_c-I_c plane, and to make the correlation between dynamic (transient) and static characteristics clear. Measurements of static DC characteristics like BV and V_{on} are limited into a small power region of the V_c-I_c plane, but the numerical simulation would easily expand those static characteristics up to the high power region without any limitation at all.

III. Extended static characteristic in terms of RBSOA

III-1. Correlation between static characteristic and dynamic characteristics

III-1-1. Introduction

In this chapter, a new procedure to obtain the RBSOA (relevant to non-destructive inductive load turn-off condition at high collector voltage and current densities)[31] is presented. As the test vehicle, a 4500V Self-Aligned Trench IGBT (SAT-IGBT)[32] is used. A relation between the high voltage RBSOA boundary and the static locking characteristics of a trench IGBT (extended to very high current densities) is investigated, with the aim of simplifying the procedure to obtain the RBSOA. As mentioned above, the SOA of an IGBT is limited by latch-up of the parasitic thyristor inherent in its structure. Over the years, several methods have been proposed to increase the latch-up susceptibility of planar gate type IGBTs and these have been discussed. Due to smaller cell pitch being possible with trench MOS-gate technology[20], the latch-up susceptibility of IGBT is further reduced. The absence of parasitic thyristor latch-up (under short circuit conditions) at current densities of 2000 A/cm^2, with two thirds the breakdown voltage applied to the collector terminals, demonstrates the wide SOA achieved for 600V trench IGBT[8]. Due to its excellent electrical characteristics, the suitability of trench IGBT was investigated for very high voltage (4500V) applications[33].

A transgression of any switching trajectory outside the SOA limits will result in a destructive failure of the IGBT. This is true for both turn-on and turn-off. Hence, knowledge of the SOA boundary becomes essential. In addition to the tradeoff between V_{on} and E_{off}, the SOA of the trench IGBT can be obtained numerically by extensive dynamic simulations (under inductive load conditions) which require an enormous amount of computation time. Using this procedure, the RBSOA boundary of an IGBT is directly obtained from its static blocking characteristics extended to very high current densities, thereby saving a large amount of computation time and effort required in obtaining the RBSOA through extensive dynamic simulations.

In addition, observation of humps in the collector current waveforms during the inductive load turn-off is also reported and analyzed[31].

III-1-2. Simulated device structures

The 4500 V SAT-IGBT had the following parameter set for a unit cell shown in Fig. III-1. A 550μm thick N^- drift region with a uniform doping level of 2 X 10^{13}cm^{-3} was for a blocking capability of around 4500V. In order to obtain an acceptable ON state voltage drop for these high voltage device, a long enough carrier lifetime for the high level injection (τ_{HL}) of 60μs ($\tau_{n0} = \tau_{p0} = 30\mu s$) is used in the N-drift region. A 15μm deep N-type diffusion having a Gaussian profile was formed on the backside as the N^+ buffer region for this 4500V class Punch Through (PT) device. The peak donor concentration in the 10μm-thick N^+ buffer region was 5.9 X 10^{16}cm^{-3}. The P^+ collector (call Anode in diode structure) diffusion also had a Gaussian profile with a surface concentration of 1 X 10^{18}cm^{-3} and junction depth of 5μm. A shallow anode junction with low surface concentration and an N^+ buffer region were carefully chosen as the optimization of V_{on}-E_{off} tradeoff. The

half-cell and half mesa width of the SAT-IGBT and trench gated diode were 3μm and 1.5μm, respectively. The half-width of the 8μm deep trench gate region was 1.5μm with a MOS-gate oxide thickness of 75nm along the trench sidewalls and bottom. The double diffusion junctions in the SAT-IGBT were obtained using a 3μm deep P-base region with a surface concentration of 2.2 X $10^{17}cm^{-3}$ and 1μm deep, N^+ emitter region with a surface concentration of 1 X $10^{19}cm^{-3}$ These parameters were chosen to have the threshold voltage being around 3V for a oxide thickness of 75nm.

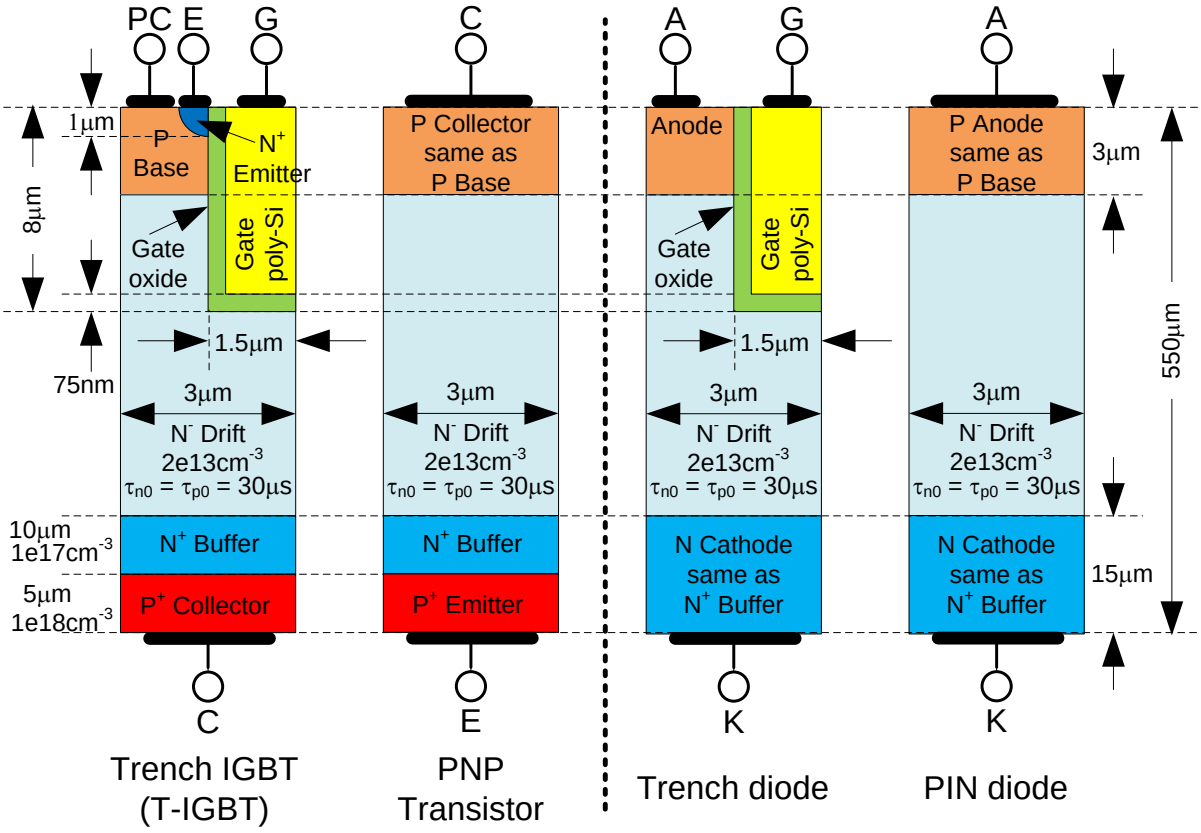


Fig. III-1. Simulation structures of the 4500V SAT-IGBT and related devices[31]

Pin diodes, both with and without trench gates, and a wide base PNP transistor with unit cell parameters identical to those of the SAT-IGBT were also evaluated for understanding the nature of the SAT-IGBT blocking characteristics at high collector current densities. All the total device thickness is fixed at same 550μm.

III-1-3. Static blocking characteristics

The unit half cell cross-section of a SAT-IGBT and a wide base PNP transistor, which is identical to the one inherent in the SAT-IGBT, with parameters indicated in Fig. III-1, were used in the numerical simulations[34]. The static blocking characteristics of SAT-IGBT, extended to high current densities were obtained in order to compare it with the high voltage RBSOA boundary obtained by performing dynamic simulations. The static blocking characteristics of a conventional PIN diode and a trench PIN diode extended to high current densities were also simulated in order to understand the nature of the SAT-IGBT characteristics at high collector current densities.

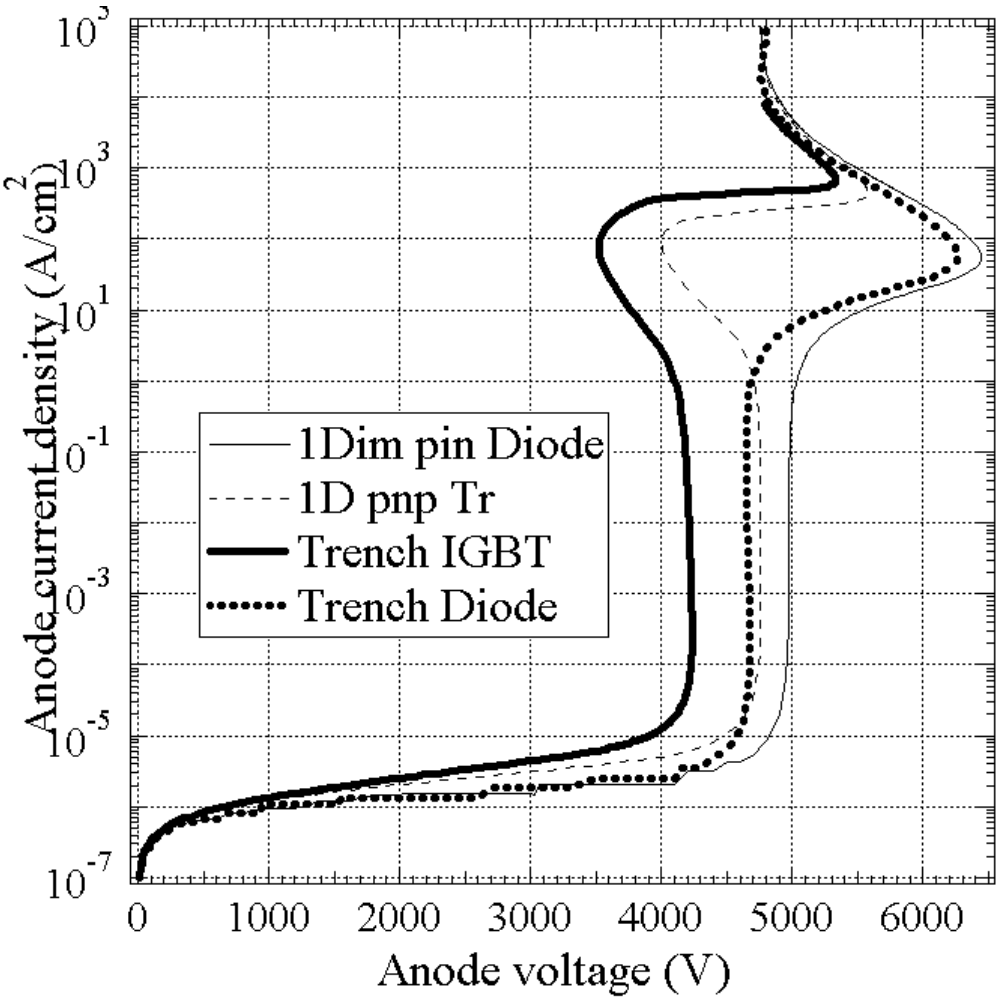


Fig.III-2. The blocking characteristics of SAT-IGBT, a wide base PNP transistor and PIN diodes[31]

III-1-4. T-IGBT and PNP transistor vs. PIN diode

The numerically simulated forward blocking characteristics of a SAT-IGBT and the wide base PNP transistor, extended up to high current densities, have been plotted in Fig. III-2 for a comparison with the blocking characteristics of PIN diodes. The blocking voltage of T-IGBT (BV_{CEO}) is lower than trench PIN diode (BV_{CBO}) due to the open base PNP transistor effects[35]. Although, the blocking voltage of T-IGBT was lower than the open base PNP transistor, the nature of their blocking characteristics was found to be identical at all current densities. This is to be expected because, in the off-state, the T-IGBT can be essentially regarded as an open base PNP transistor. In striking contrast to the PIN diodes, the forward blocking characteristics of the T-IGBT (and the PNP transistor) first exhibit a negative resistance portion for collector current densities between $1mA/cm^2$ to $100A/cm^2$. A positive resistance portion is then observed for anode current densities between $100A/cm^2$ to $800A/cm^2$. Eventually, the *Vc-Ic* characteristics of all device structures merge at current densities greater than $800A/cm^2$. The nature of the *Vc-Ic* characteristics of the T-IGBT is explained with the aid of Fig. III-3, which show the impact ionization rate, the carrier concentration and the electric field profile in the drift region for various of collector current density, respectively.

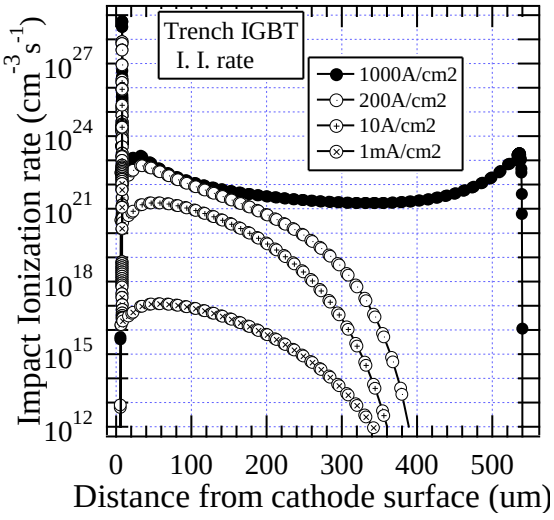


Fig. III-3 (a)

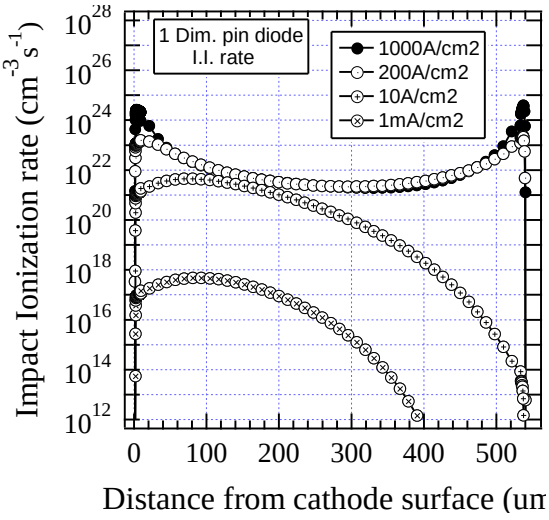


Fig. III-3 (d)

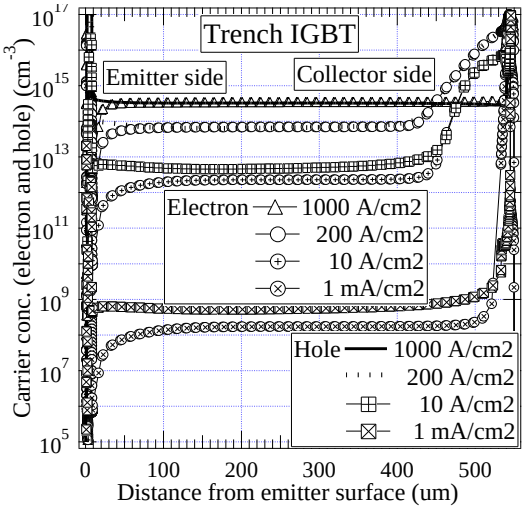


Fig. III-3 (b)

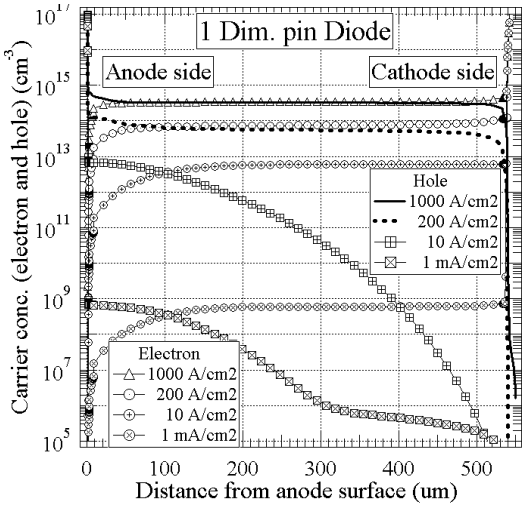


Fig. III-3 (e)

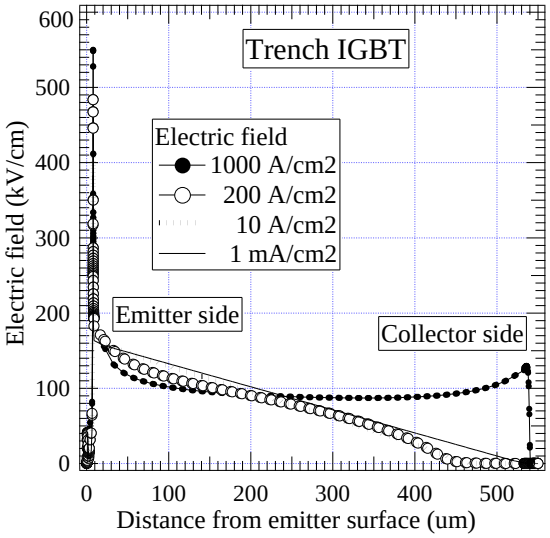


Fig. III-3 (c)

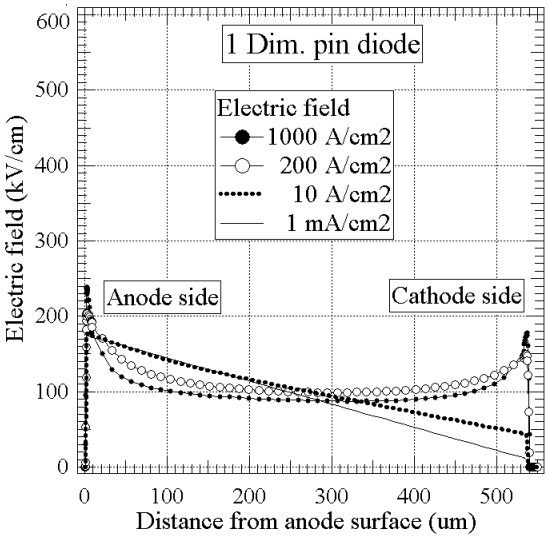


Fig. III-3 (f)

Fig. III-3. The impact ionization rate, the carrier concentration and the electric field profile in the SAT-IGBT and one dimensional diode at various values of the collector current density[31]

At high collector voltages, electrons generated in the drift region by impact ionization (Fig. III-3 (a)), provide base drive for the wide base PNP transistor inherent in the IGBT structure. This promotes hole injection from P^+ collector / N^+ buffer junction into the drift region via the transistor action. A signature of the transistor action is seen Fig. III-3 (b), which shows a higher hole concentration (than electron concentration) in the drift region of the SAT-IGBT. The hole injection (via the transistor action) increases the positive charge in the N-drift region and gives rise to the first negative resistance portion of the forward blocking characteristics of the SAT-IGBT. However, the negative resistance portion of the static blocking characteristics is not discernible at lower collector current densities from $1mA/cm^2$ to $1A/cm^2$. This is because, at these current levels, the hole concentrations established in the drift region (Fig. III-3 (b)) are negligible compared to the background ionized donor concentration ($N_d = 2 \times 10^{13} cm^{-3}$). Consequently the electric field in the N-drift region has the familiar triangular distribution for collector densities between $1mA/cm^2$ to $1A/cm^2$ as seen in Fig. III-3 (c). However, at higher current densities, the concentration of holes established in the drift region becomes comparable to the background donor concentration due to an increased impact ionization rate in conjunction with the transistor action. This increases the net positive charge in the depletion region causing a significant decrease in the blocking voltage of the SAT-IGBT for collector current densities in the range of $1A/cm^2$ to $100A/cm^2$.

Furthermore, with a fall-off emitter injection efficiency at high current densities (Rittner Effect), less amount of holes are injected into the space charge region and more electrons are back injected into the P^+ substrate for collector current densities greater than $100A/cm^2$. This decreases the positive space charge in the drift region causing higher voltage to be supported in the T-IGBT for emitter current densities between $100A/cm^2$ to $800A/cm^2$.

As the collector current density is increased beyond $800A/cm^2$, a significant amount of electron-hole pair generation is initiated by the electrons moving through the high electric fields on the collector side of the SAT-IGBT (Fig. III-3 (a)). Although, the generated electrons are immediately back injected the collector terminal, the generated holes are swept into the drift region by high electric fields. This additional hole injection increases the positive charge in the drift region giving rise to the second snap back observed in the V_c-I_c characteristics of SAT-IGBT. At these current densities, the physics governing the V_c-I_c characteristics of all the devices is determined by the properties of N^- drift / N^+ buffer junction. Since the properties of the N^- drift / N^+ buffer junction is same in all the device structures, their V_c-I_c characteristics were found to merger at very high current densities as seen in Fig. III-2. The physics causing the negative resistance in the forward blocking characteristics of the SAT-IGBT (and the wide PNP transistor) is akin to the process of double-injection, which is believed to produce the snap back in the V_c-I_c characteristics of insulators[36].

III-1-5. Simulation procedure for RBSOA

Inductive load turn-off features were simulated by the following procedure without using circuit modules of MEDICI simulator to be independent from the turn-off conditions such as inductance and ramping rate. It means without using any free wheel diode or any passive circuit elements of actual circuit, i.e. a stray capacitance and inductance. First, the ON state solution file was obtained in a certain current density, ex. $200A/cm^2$. In this case, an applied gate bias is set forth high enough for saturation condition, i.e. V_g = +15V.

Second, the collector voltage V_c was ramping up processes, to get solution file at high enough V_c condition in the same current density as the previous solution, ex. 200A/cm^2. In this case, V_g was changed from +15V to -15V and still using current boundary condition for the collector contact to fix the collector current density. Finally, starting the turn-off process to change the collector boundary condition from "current" to "voltage". V_g is still set forth at -15V. Only the time was traveling following the solution file time which should be used as the initial condition of the turn-off sequence. Note that all the simulation results were obtained at the isothermal condition, which was fixed at the room temperature.

III-1-6. Correlation between dynamic RBSOA and static BV characteristics

In circuits controlling inductive loads, high currents and voltages are simultaneously impressed across the IGBT terminals during turn-off. The locus of current-voltage values across the IGBT terminals during turn-off is described by its turn-off trajectory. A transgression of any turn-off trajectory outside the SOA boundaries causes a destructive failure of the IGBT. Hence, a prior knowledge of the SOA of the IGBT is essential. A typical turn-off trajectory is shown in Fig. III-4 as line A-B-C, for simulation of a clamped inductive switching circuit. For a given collector current density, to determine one point on the RBSOA boundary, the maximum voltage at which the current can be successfully turned-off is obtained by repeating the simulation with small increments of collector voltage until the device fails to turn-off. The simulations must be then repeated for the other values of collector current density. The procedure suggests that it takes a large number of simulations and computation time to obtain the high voltage RBSOA boundary by this method.

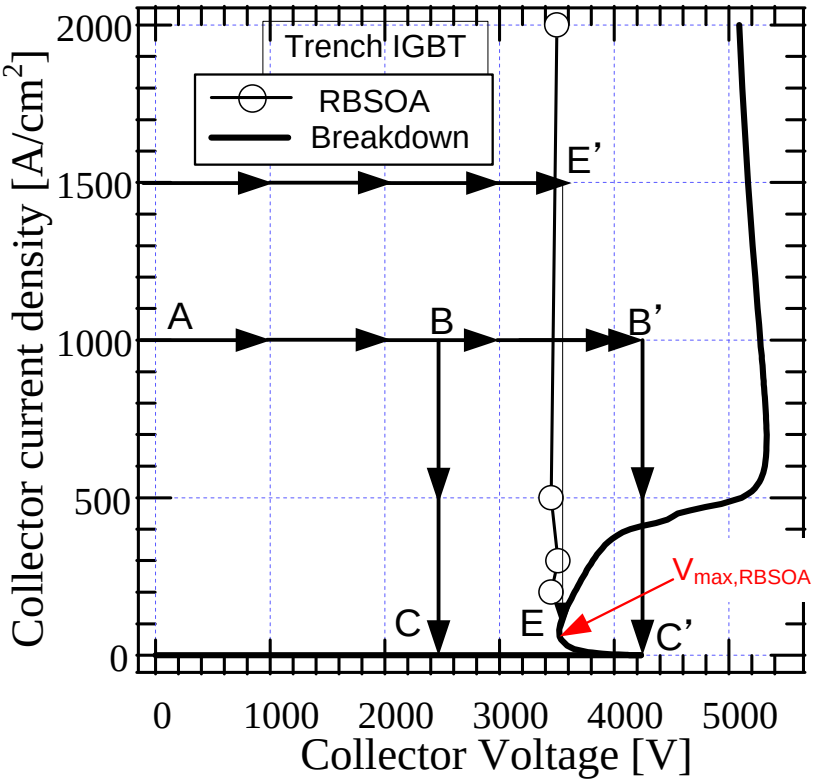


Fig. III-4. A relation between the RBSOA and static blocking characteristics of the SAT-IGBT brought out by inductive load turn-off trajectories[31]

The RBSOA of SAT-IGBT obtained using the above procedure was square shaped and injected that a collector current density as high as 2000A/cm^2 could be turned-off successfully with a collector voltage of about 3400V. It can be seen from Fig. III-4 that the maximum voltage of the RBSOA boundary is nearly the same as the minimum voltage 3500V of the first negative resistance portion of its static blocking characteristics extended to high current densities. The reasons for this observation can be explained by examining the turn-off trajectory A-B'-C' in Fig. III-4. Along the B'-C' portion of the turn-off trajectory, steady state is reached at the point D' and not C'. Due to the large residual current at D', a turn-off trajectory A-B'-C' is regarded to fall outside the RBSOA of the device. Furthermore, the residual current was found to be independent of the initial current density for a fixed collector voltage, but increases with increasing collector voltage. Based upon this analysis, an IGBT with its turn-off trajectory lying to the left of line E-E' in Fig. III-4 will always turn-off successfully because the corresponding turn-off trajectories never intersect the high current portion of the static blocking characteristics. Thus, the minimum voltage $V_{max,RBSOA}$ of the first negative resistance portion of the static blocking V_c-I_c characteristics defines the high voltage RBSOA boundary of the IGBT. Consequently, it is possible to obtain the RBSOA boundary by single simulation of the static blocking characteristics to high current densities to determine $V_{max,RBSOA}$.

III-2. Turn-off oscillations

During the RBSOA simulations of the T-IGBT, a pronounced hump in the collector current waveform was observed after an initial fall of the collector current even in cases when the collector current was successfully turned-off as shown in Fig.III-5. Since this oscillation of the collector current leads to additional switching losses, the physical phenomena responsible for the hump were analyzed. Here, it should be emphasized that, as described above section, these simulations were done in pure device simulation condition without any passive circuit element to induce the oscillation. This hump can be observed in approximately one microsecond after initial fall of collector current and very large up to two-thirds of initial current density. The hump magnitude is increasing as collector voltage rising, reaches the maximum magnitude of 3450V in case of collector current density being 200A and disappears in the condition of being unable to turn-off of 3500V.

By examining the electric fields, carrier concentrations (both electron and hole distribution) and both electron and hole drift velocities (Fig. III-6 (a), (b), (c)), at various time instants when (A) the turn-off starting point (B) the first minimum current density point, (C) the first hump occurring point, (D) the second minimum current density point, and (E) the finally turned-off point at 200μsec after initial point, respectively, indicated in Fig. III-5. The electric field distribution has a maximum value at the bottom corner of trench in the every moment of these figures. As the result of these high electric field strengths, carriers (electron and hole) are generated in very high density, because of over range not shown in Fig. III-5. In the space charge limited region, carrier densities are reflecting the current density of each time points, but only the very slight change can be observed in the neutral region. We conclude that the hump is caused by the impact ionization electron current which serves as a base drive for the PNP transistor. This promotes further injection of holes across the P^+/N-buffer junction via the transistor action. This conclusion was verified by performing simulation under

identical turn-off conditions without the impact ionization parameter. As illustrated in Fig. III-5, the hump disappears under these conditions confirming that impact ionization is responsible for its on-set.

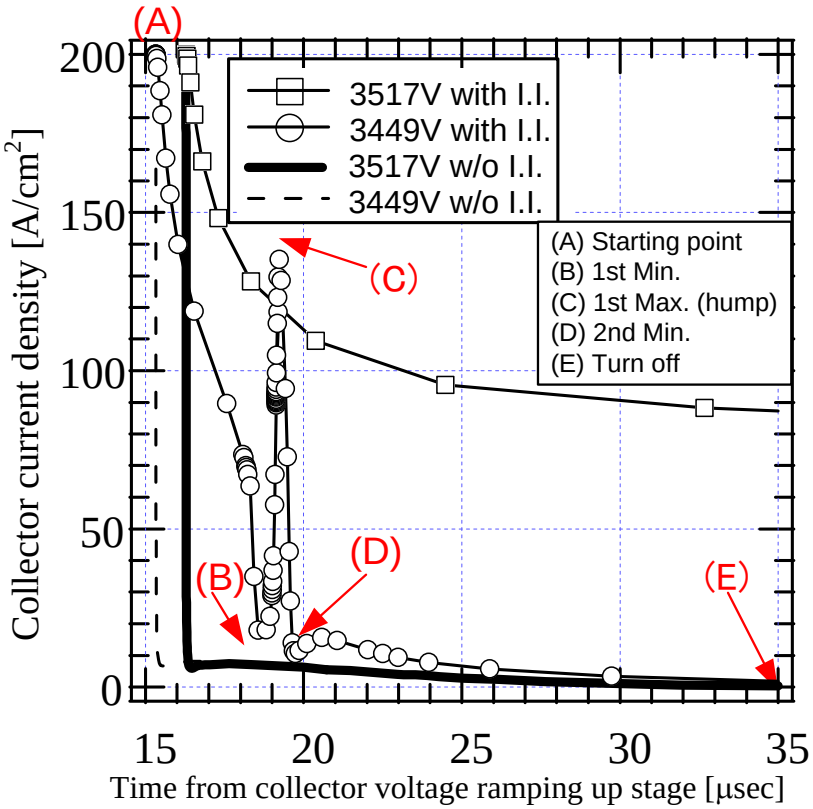


Fig. III-5. Turn-off waveforms under inductive load conditions showing oscillations in the collector current of the SAT-IGBT[31]

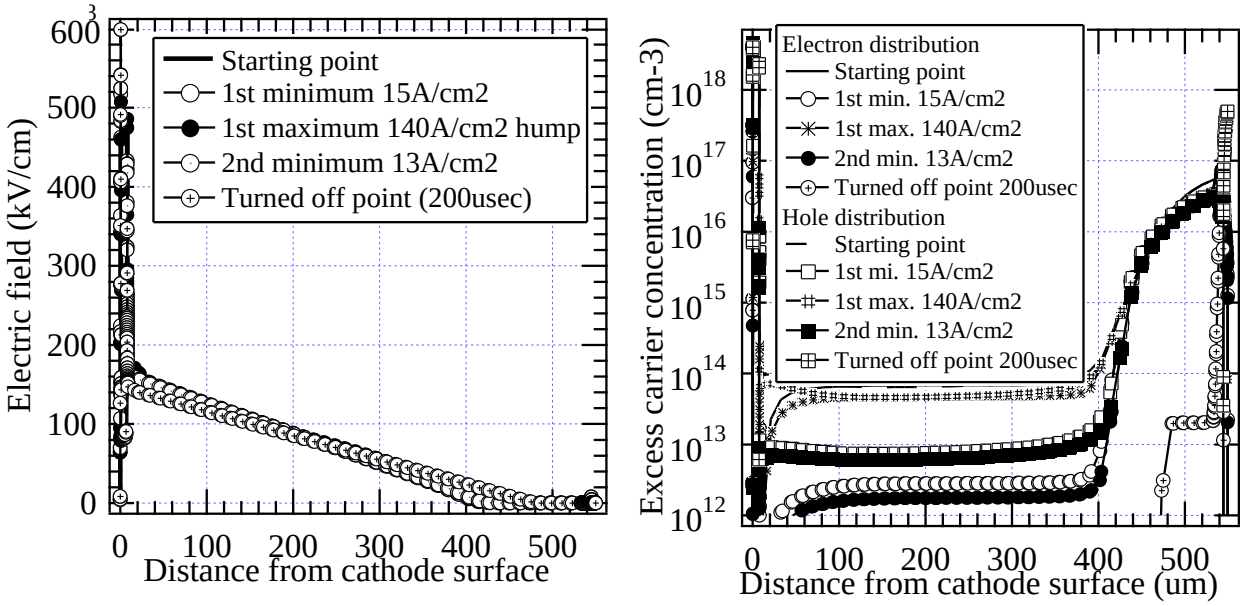
It can be seen form Fig. III-5 that a time lags of about 1.5μs was observed between the current humps. We believe that this time lag τ_l is the time required by the holes (injected from the P^+ substrate) to reach the high electric field region near the trench corners. Therefore,

$$\tau_l = \tau_{sc} + \tau_{Diff} \qquad \text{(III-1)}$$

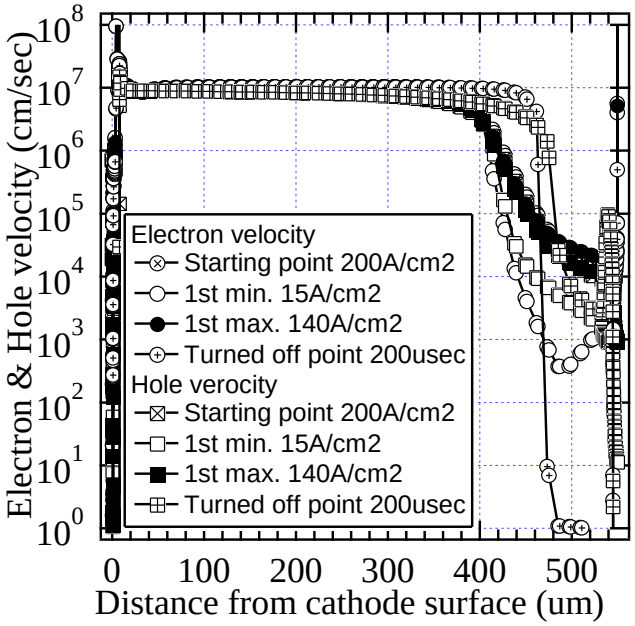
where τ_{sc} is the time required for the holes to traverse the space charge region (W_d) and τ_{Diff} is the time required for the hole to move through the undepleted N-type region (W_{ud}) by the diffusion process. As shown by the high electric field in the drift region (Fig. III-6 (a)), the hole velocities saturate in the drift region as shown in Fig. III-6 (c). In the remaining undepleted portion of the drift region (W_{ud}), the holes move via the slower diffusion process as inferred from the excess carrier profile shown in Fig. III-6 (b). Hence,

$$\tau_{sc} = W_d / V_{sat,p}\ ,\ \tau_{Diff} = W_{ud}^{\ 2} / 2 \cdot D_a \qquad \text{(III-2)}$$

For a 400μm (W_d) wide space charge region, τl = 4 ns using a saturate velocity of 1 X 10^7cm/s ($V_{sat,p}$). In our case, τ_{Diff} is calculated to be 4μs (for W_{ud} = 120μm and D_a = 18cm^2/s). The observed time lag between successive oscillatory humps (1.5μs) is lower than the calculated value of the time lag (τ_{Diff}) because of the electric field aiding the motion of holes in this region.



(a) Electric field distributions (b) Carrier distributions



(b) Carrier velocities in the drift mode

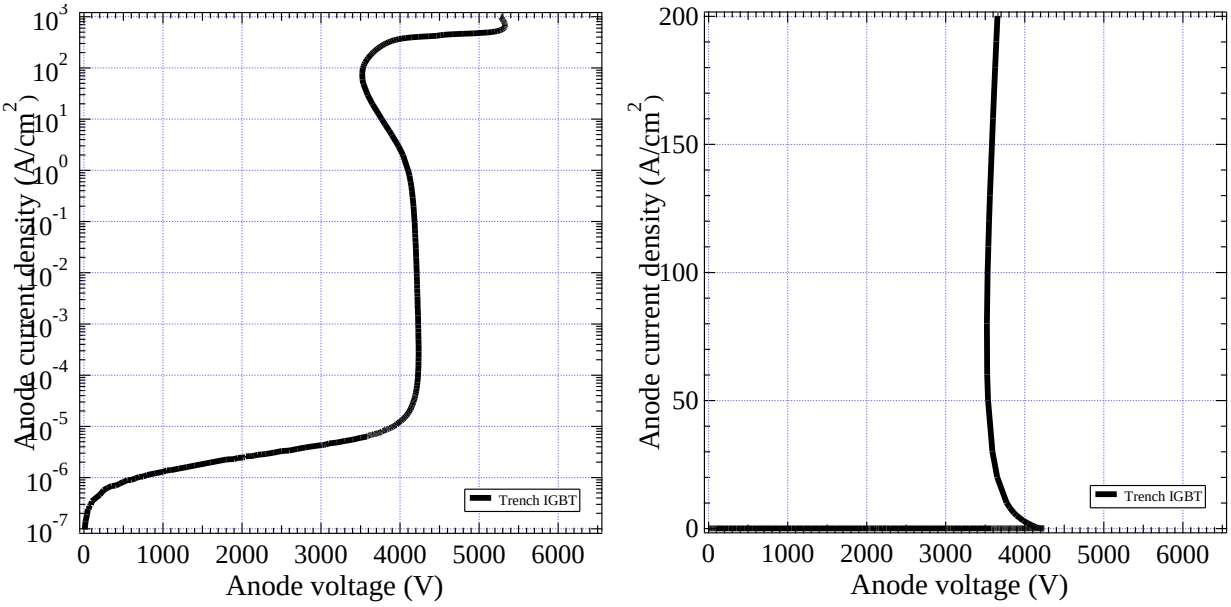
Fig. III-6. The electric field, carrier concentration and carrier velocities in the SAT-IGBT at various time instants of the turnoff waveform with a pronounced hump shown in Fig. III-5[31].

This observation of oscillation in the *Ic* waveform during an inductive load turn-off is reported for the first time. This oscillation is caused by impact ionization. The time lag between these oscillations is associated with the transit time for the injected holes through undepleted drift region near the collector.

III-3 Summary and discussion

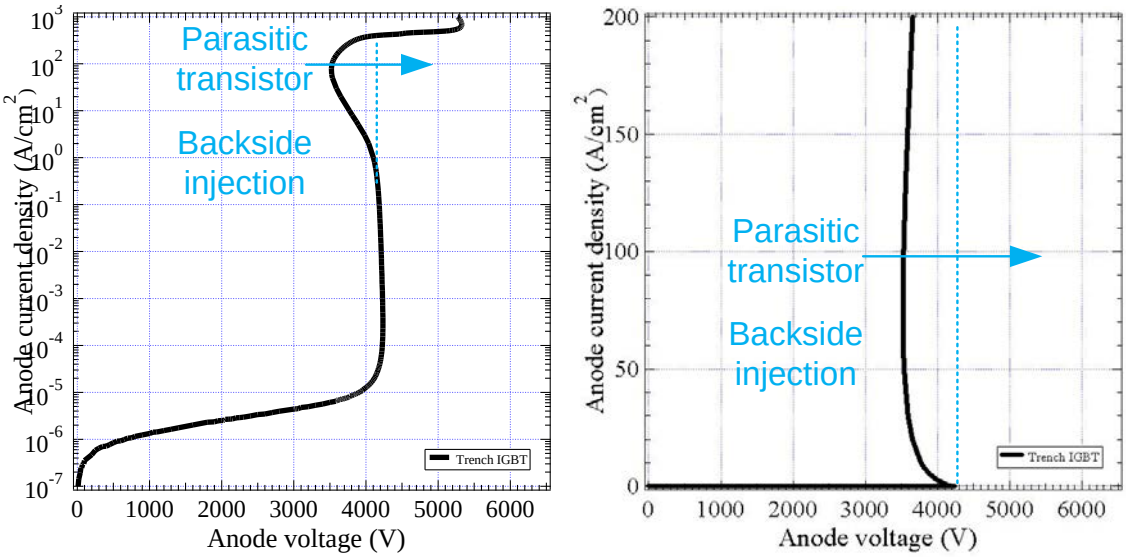
This observation allows determination of the RBSOA using a single simulation which saves computation time and effort. This is the first achievement[31] of simulation analysis for the RBSOA

characteristics of T-IGBT. And RBSOA of the most important dynamic characteristic can be tightly related to the *BV* curve of a static characteristic.



(a) Logarithmic scale same as III-2 (b) Linear scale around the negative resistance portion

Fig. III-7. BV characteristics until high current density of SAT-IGBT[31]



(a) Logarithmic scale (b) Linear scale

Fig. III-8. Direction of improvement for RBSOA by reducing the parasitic PNP transistor action[31] using the same BV curve of Fig. III-7

The RBSOA boundary for the IGBT is the first minimum V_c of the negative resistance portion observed in static BV characteristics in the high current density, as shown in Fig. III-7 (a) (b). The backside structure used in this simulation is the enhanced model of the parasitic PNP transistor action, so the static *BV* value is just same as 4500V and has no margin in higher current density region. But, those results are enough to

discuss the model of the high current density operation.

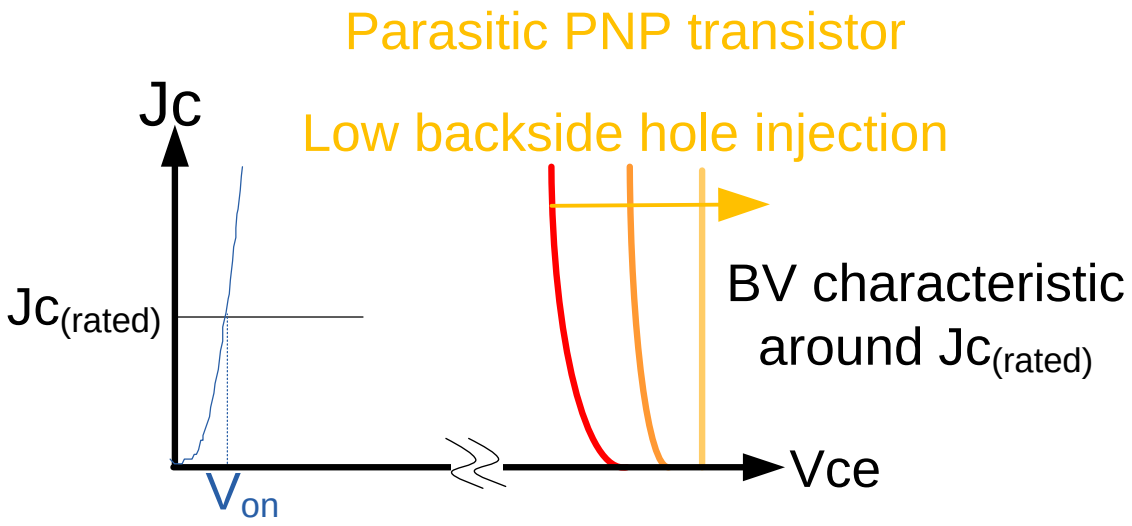


Fig. III-9. Schematic illustration of BV characteristics' improvements for a negative resistance region around the rated current density

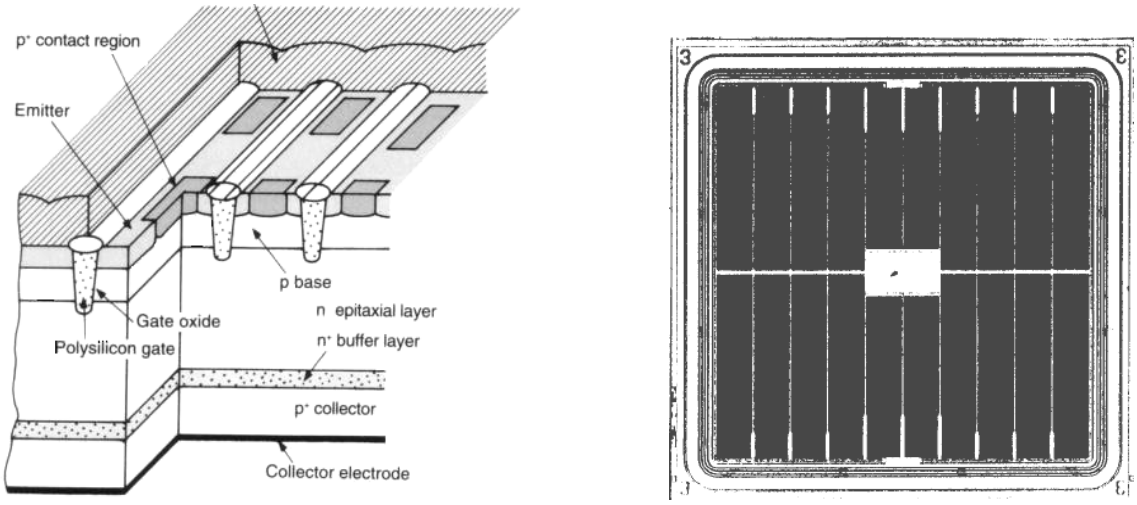
(1) The maximum voltage of the RBSOA boundary is nearly the same as the minimum voltage in the first negative resistance portion of the forward blocking characteristics extended to high current densities. Visualization is succeeded for the RBSOA boundary as the extended *BV* curve. The FBSOA boundary would be obtained in the same manner. The shape of SOA (= RBSOA + FBSOA) would be the real area consist of the *BV* curve and the *Von* curve, respectively as shown in Fig. III-9.

(2) The static *BV* characteristic of SAT-IGBT is similar to the PNP transistor and is marginally affected by the presence of the trench gate. That is the secondary breakdown of *BV* curve is caused by the PNP transistor action, and not caused by the Impact Ionization effect near around the trench bottom. The shape of RBSOA would be easily improved not to have a large negative resistance portion at around the rated current density region by the P-collector doping concentration to be low as to reduce the hole injection efficiency as shown in Fig. III-8. And the improved example of a negative resistance region around 100A/cm^2 is also shown in Fig. III-9, which will be explained at the later chapter.

In high voltage region, where the backside P-collector and N-buffer profile are easily optimized independently, there are several successful approach to reduce the hole injection, such as the alternative P^+/P^--collector structure[37] and the uniformly low P-collector[38]. One of the reason why this kind of approach has not been intensively carried out is that the IGBTs in the medium voltage class of 1200V and 600V had used Epitaxial wafers with an extremely thick and highly doped P^+ substrate of 400μm and more until year around 2000. There was no room to reduce the concentration of P^+ collector for the low hole injection. The "LPT" type backside structure has enabled to optimize the backside collector doping. So the current generation of the LPT type IGBT has been much improved on the RBSOA boundary of its shape. It will be discussed in chapter VII.

IV. Design of T-IGBT for improved V_{on}-E_{off} tradeoff

The T-IGBT was predicted to improve V_{on}[34], and certified in the end of 80's[20]. And the effect to improve the fundamental tradeoff V_{on}-E_{off} was commercially confirmed as the T-IGBT [9] in 1994. T-IGBT was realized by using the VLSI wafer process technology of one micrometer design rule as shown in Fig. IV-1.



(a) The 3D schematic cross-sectional view of cell structure (b) The photo-image of 600V 50A chip

Fig. IV-1. Trench gated IGBT (T-IGBT)[8]

Since the T-IGBT is free from the JFET effect and owing to the higher channel density, the T-IGBT has nearly the same forward *Vc-Ic* output characteristic as a PIN diode shown in Fig. IV-2. Unlike the planar gate IGBT, the T-IGBT does not show saturation in current.

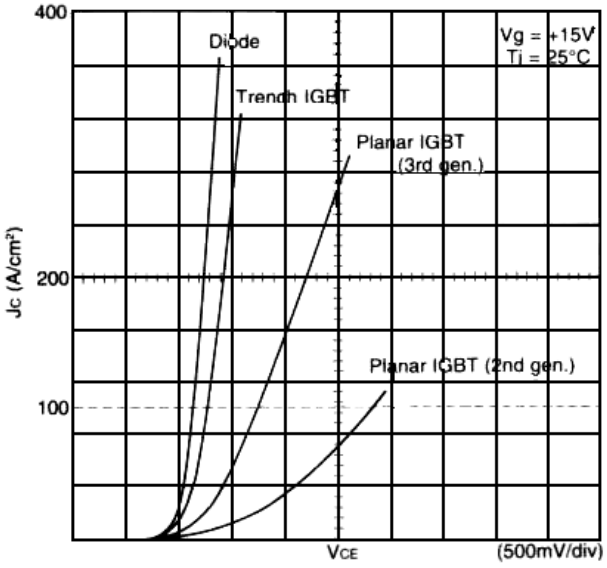


Fig. IV-2. The forward output Vc-Ic characteristics of T-IGBT, Planar gate IGBTs and PIN diode[8]

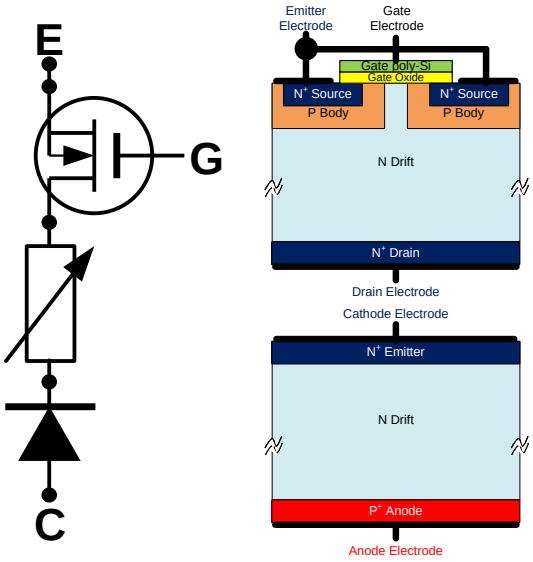


Fig. IV-3. The ideal ON state model[34]
IGBT = MOSFET + PIN diode

This is a good evidence of the ideal ON state model of the IGBT as the serial combination of MOSFET + Diode as shown in Fig. IV-3[35]. Prof. B. J. Baliga, who is one of the inventors of the IGBT concept as the MOS controlled Thyristor structure[34], suggested that the fundamental elements of constructing IGBT are those two parts. In the electrical circuit model, the current flows along only one direction from collector to emitter or form the higher potential electrode to the lower potential electrode. But, inside of the semiconductor material silicon, there are two type of current, that is the electron current and the hole current when the conductivity modulation occurs as the bipolar action. As far as the numbers of the electrons and holes are equal, the charge neutrality is maintained. At that time, the electrical resistivity goes down very closely to zero, and both the electron current and the hole current flow as the diffusion current, not a drift current. So this phenomenon is called the conductivity modulation. To maintain this conductivity modulation condition, the carrier lifetimes of both the electron and hole are long enough, and the numbers of both electrons and holes are also large enough to fulfill the entire drift region which is sometime very thick to support the high breakdown voltage. Here, MOSFET part is the electron provider and the PN junction in the backside collector is the hole provider, respectively. If the ability of both the electron injection of MOSFET and the hole injection of pn diode would be high enough, the total Von of IGBT would reach a simple summation of the N-channel resistance of MOSFET and the built-in potential of PN junction of the backside PIN diode. As shown in Fig. IV-2, the T-IGBT's forward output Vc-Ic curve is very close to the diode one. Form the Von point of view, the T-IGBT could closely reach the ideal characteristic of the IGBT concept.

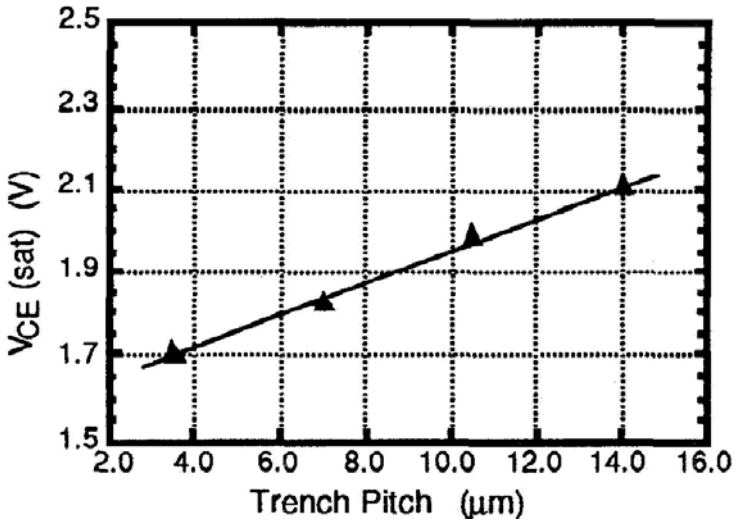


Fig. IV-4. The trench pitch dependence of Von of T-IGBT[8]

T-IGBT's V_{on} linearly depends on a trench pitch as shown in Fig. IV-4, and it does not saturate to be shrunk in its cell size. This is because absence of the JFET effect, which strongly affects the planar gate IGBT. But, this cell shrink concept should be carefully discussed in the later chapter as the wide cell pitch effect with the multiple dummy trenches.

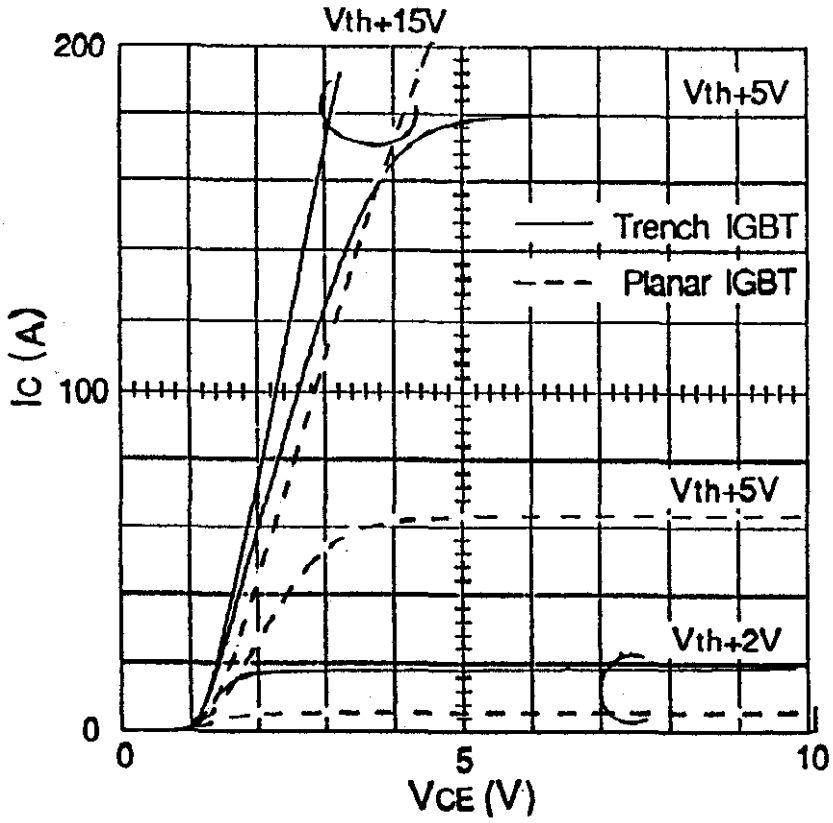
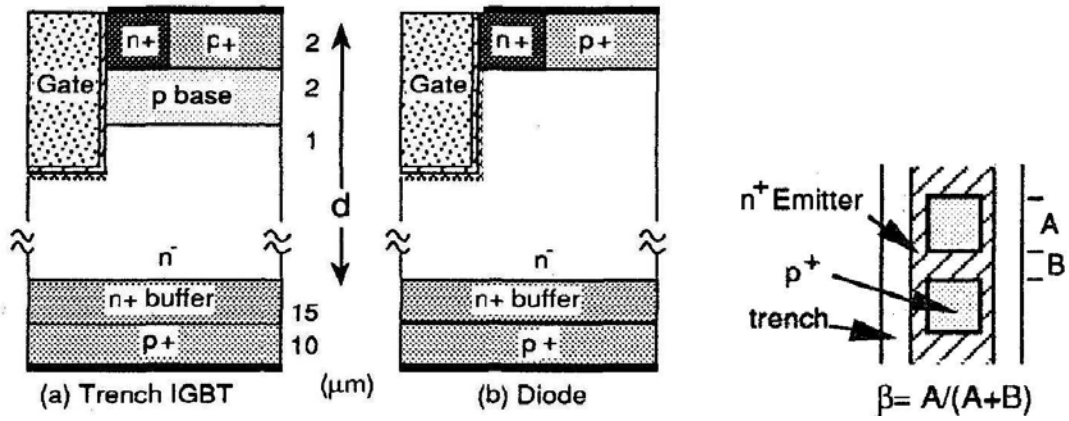


Fig. IV-5. The V_g dependence of the forward output V_c-I_c characteristics of T-IGBT and Planar IGBT[8]



(a) Schematic cross-sectional views (b) a definition of the pn ratio at the top surface

Fig. IV-6. T-IGBT and trench gated diode (T-Diode)[8]

In comparison with trench IGBT and PIN diode, there is the subsidiary but important idea which testifies n / (n + p) ratio plays an important role for the electron injection efficiency in the cathode side. Although this reference diode structure is not a simple PIN diode but a cathode shorted diode (Fig. IV-6), which has a common metal contact for both N^+ cathode and P^+ contact located next to the N^+ cathode. The higher the n/(n+p) ratio is, the higher the electron injection efficiency which characterizes V_{on} or R_{on} of device in the ON state.

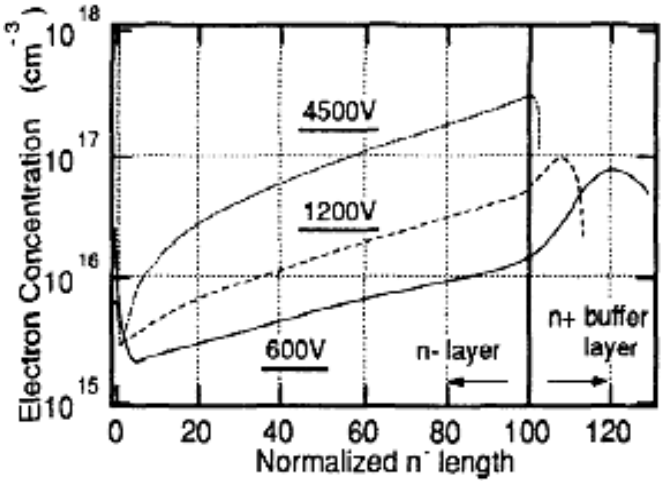


Fig. IV-7. Electron distribution as the excess carrier at the ON state of T-IGBT[8]
N-drift thicknesses are 50, 100, 570μm for 600, 1200, 4500V, respectively.

This simple T-IGBT is just an entrance of the fashion of a pushing up the cathode side electron injection efficiency. Even in the T-IGBT structure, the carrier distribution at the ON state, as shown in Fig. IV-7, is not same as the ideal PIN diode, which has the catenary carrier distribution as the previous chapter I. The T-IGBT's carrier density near the cathode is one order lower than its collector side one. Being discussed in the carrier distribution analysis in the chapter V, this low carrier injection efficiency can be improved by deepening the trench or widening the trench. But, either a deep or a wide trench has a larger gate capacitance than the standard one, and its large gate capacitance causes worse for both turn-on and turn-off characteristics and SOAs.

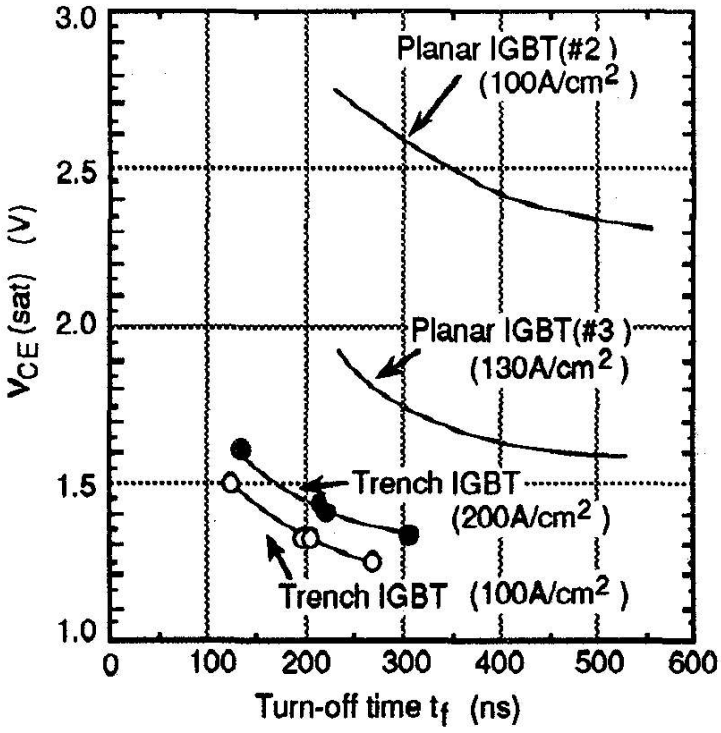


Fig. IV-8. The fundamental tradeoff characteristics of T-IGBT and the previous generation IGBTs[8]

As shown in Fig. IV-8, it is remarkable for the improvement of the fundamental tradeoff relationship V_{on} - t_f (turn-off fall time), which is usually used as the index of turn-off characteristics instead of E_{off}, in case of PT type IGBT's characteristic adapting the carrier lifetime control method and stands for a "fall time" defined as the time distance from 90% of Ic to 10% of I_c. And a $V_{CE(sat)}$ is an industrial naming of V_{on}. So, the trench gate is the solution to improve the baseline of the triangular tradeoff relationship.

The n/(n+p) ratio still has a little difficulty to be clear by the self-consistent explanation. The n/(n+p) ratio includes the accumulated n-channel region for n ratio. For example, the deeper or wider trench device has much larger N-type accumulated channel region than the standard one, or, the smaller cell pitch causes higher channel density to enlarge N-type accumulated channel area along the trench sidewall even in the standard trench IGBT structure, which has not so deep trench or wide trench, than the standard planar gate type IGBT structure. One more important idea is to maintain the less P region in the total area in the cathode side region. The second idea as the multiple trench gate type devices will be discussed in chapter V.

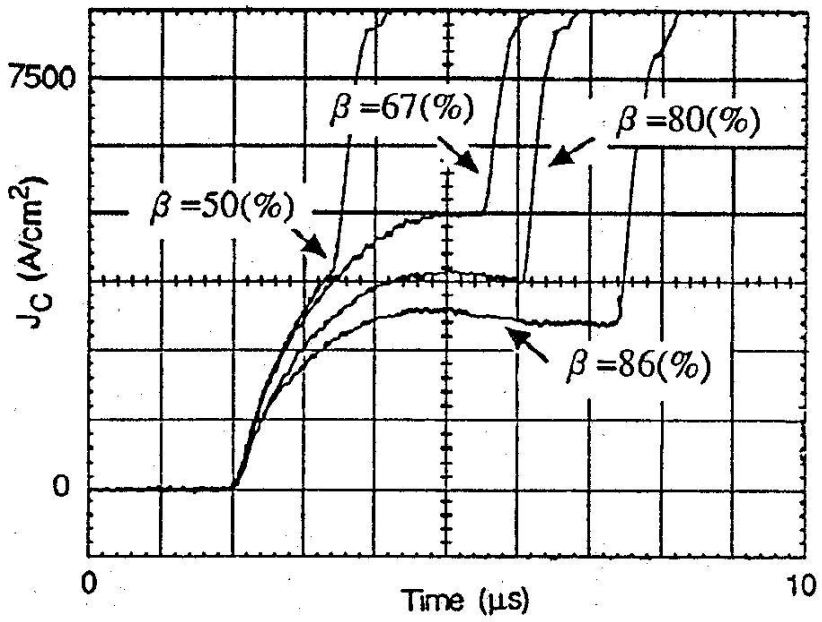


Fig. IV-9. Jc waveforms as SCSOA characteristics[8]

Here arises another frustration to be solved as the intersectional line tradeoff in the triangular tradeoff (Fig. I-8, II-12), that is SCSOA versus "V_{on}-E_{off}".

SCSOA capabilities as Jc waveforms were shown in Fig. IV-9, n/(n+p) ratio β dependence of time endurance width t_w. "t_w" is clearly improved by increasing p portion to reduce the I_{sc} (J_{sc}), but t_w could not reach 10μs in this case. Unfortunately, it was not acceptable for stand-alone type IGBT power module, in Mitsubishi Electric's product code-name of CM (Conductivity Modulation type) module. So, this low V_{on} but short characterized T-IGBT was used in the IPM (Intelligent Power Module), in which an SC (load-Shorted Circuit) mode protection circuit is installed together with for a rapid shut-down in case of SC-mode. In spite of an enormous I_{sc} (J_{sc}), T-IGBT's E_{sc} is much higher than the conventional P-IGBT (Planar gated IGBT). For example, P-IGBT's Jc is around 400A/cm^2 and tw is more than 20μs, it makes E_{sc} more than 8J/cm^2. In contrast, roughly estimated value of Esc for the above T-IGBT's case of β 67% is a half of 5000A/cm^2 3μs, 7.5J/cm^2,

this is almost same as P-IGBT's. But the case of β 86% is 3000A/cm^2 over and 5μs over, 15J/cm^2, and this is more than twice time larger than P-IGBT case. So, T-IGBT's E_{sc} is potentially close to the thermodynamics limit to be maintained by the effective N-drift thickness in an adiabatic condition.

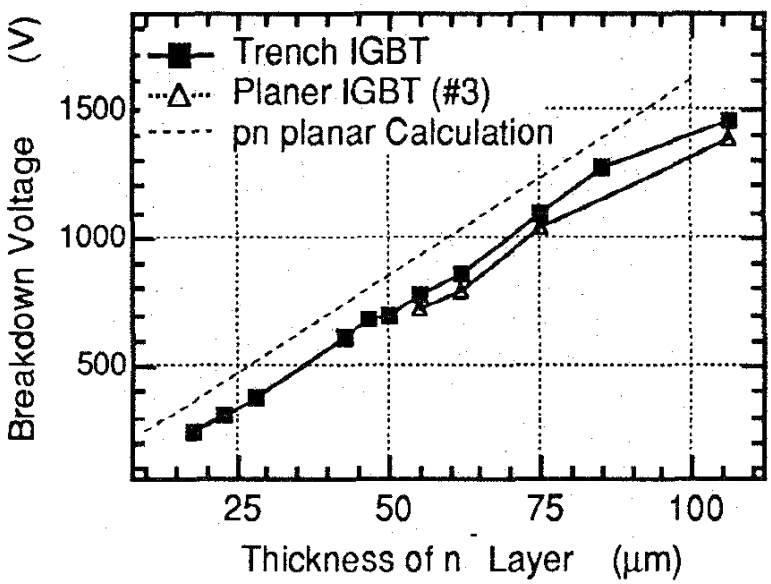


Fig. IV-10. N-drift thickness dependence of the BV characteristics[8]

And the *BV* characteristic is almost same as or little higher than the conventional P-IGBT as shown in Fig. IV-10. This is because P-IGBT's P-body region is not plane sheet in the MOS channel region. Although T-IGBT has a trench whose bottom electric field is concentrated, the degradation of *BV* is not so large as far as both the trench repetition pitch and jet depth is small.

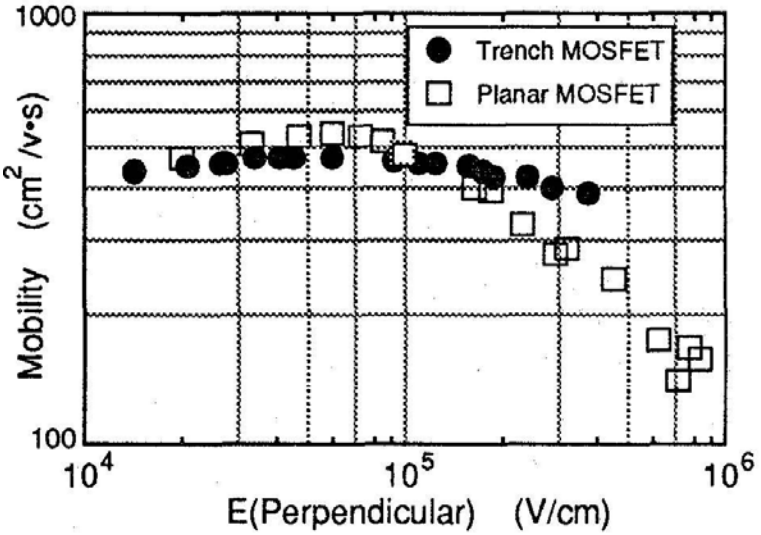


Fig. IV-11. Electron motilities for both trench and planar gate[8]

A sacrificial oxidation process for the post trench etch step is very effective to recover the electron mobility along the trench sidewall for the n-channel of MOS gate structure in T-IGBT[15][36], as shown in Fig.

IV-11. Generally speaking, it is not easy to discuss the absolute value of channel mobility. In the comparison of the relative value, the mobility of trench gate seems to be very close to the planar's one in the relatively low electric field region as the standard operation of the gate applied bias.

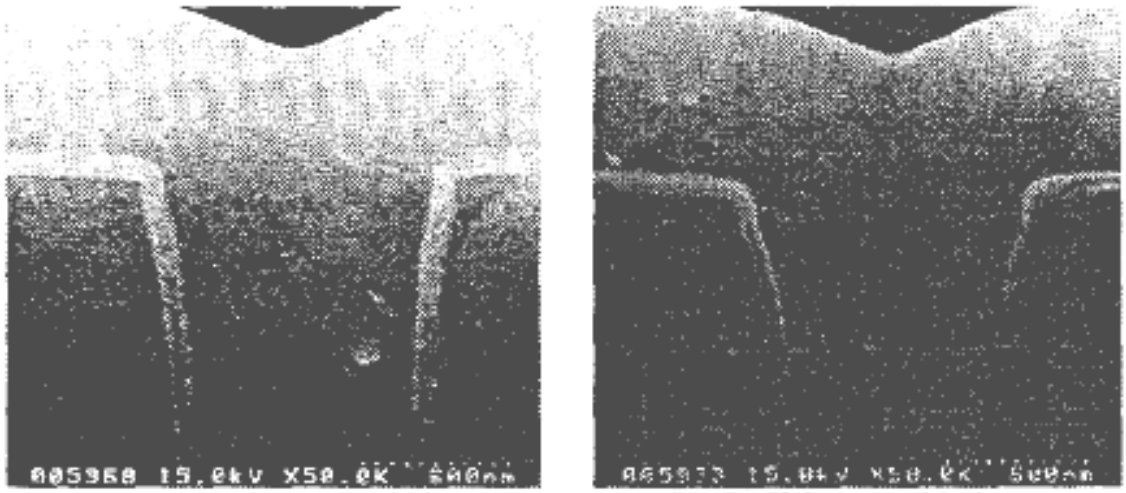
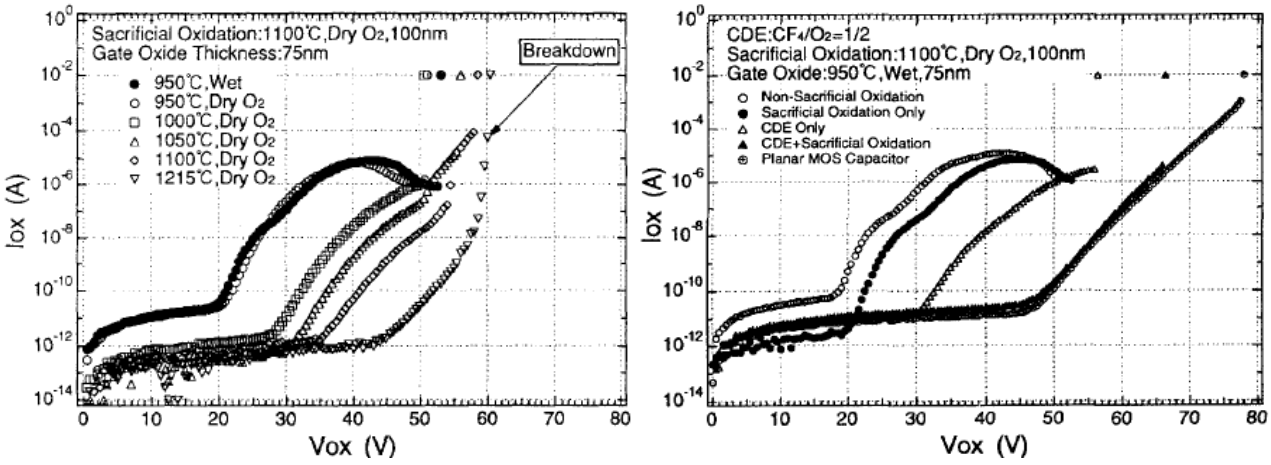


Fig. IV-12. SEM images of trench opening portion (Si mesa region)[36]
Both are improved examples



(a) Temperature and atmosphere conditions for sacrificial oxidation (b) combination with CDE

Fig. IV-13. Optimization for the post-trench treatment from TZDB (Time Zero Dielectric Breakdown) V_g-I_g characteristics[36]

There three large issues to be overcome form the first idea[20] to the mass-production phase. Trench gate process is originally developed as the isolation technology of LSI, so the depth are limited around 3μm and an aspect ratio is limited around 2 or 3. As the trench gate for power MOSFET or T-IGBT, 5μm or more depth with an aspect ratio of around 5 is needed. This heavier wafer process requirement needed an additional effort to establish the special treatment as the post-trench etching process. This is because the trench gate oxide yield and reliability are strongly affected by shapes of trench opening corner and bottom corner, and a channel mobility is

also affected by a micro-roughness of a trench sidewall.

A thermal oxidation process, either a sacrificial oxidation or a gate oxidation itself, produces an acute angle from even a right angle of Si mesa edge, and this sharp edge is harmful for both gate yield and reliability. To avoid Si mesa edge going to be acute angle and to make an obtuse angle, three extra process steps are needed[15][36] such as the CDE (Chemical Dry Etch) for an etch-back a shoulder portion of Si mesa, the high temperature (equal or more than 1100 cent-degree) and dry atmosphere sacrificial oxidation (Fig. IV-12 (a)(b)) to be removed before the gate oxidation and the independent wet atmosphere gate oxidation around 950degC or so. According to the wafer process cleanness (class), an LPCVD (Low Pressure Chemical Vapour Deposition) oxide layer[15] is also effective instead of the gate thermal oxidation.

Trench gate approach was the first step and the good evidence to improve the electron injection efficiency, and there still has been a more room to improve this efficiency by using the special trench gate structures discussed in Chapter VI.

V. Carrier distribution analysis to improve V_{on}-E_{off}

Mentioned above the chapter IV, high injection efficiency for the cathode side with the control gate is one of the very effective approach to get lower V_{on},, and low hole injection is one of the most effective way to get lower E_{off}. It is not easy but necessary to define the universal description about carrier distribution design for bipolar type devices corresponding to the widely spread device usage and application circuits, from the electron injection efficiency point of view in the cathode side structure including the control gate.

Except rectifier (diode) structures, for every forced turn-off (gate-control) type device, the control gate structure defines its electron injection efficiency of a cathode side for the N-channel device. Here are two examples of the control gate structure to vary the electron injection efficiency in the ON state. The first one is the MOS gated device[42], IGBTs and MCTs (MOS Controlled Thyristor), and the second one is the junction gated type devices, SIThy (Static Induction Thyristor or FCD : Filed Controlled Diode) and GTO (Gate Turn-Off Thyristor)[43]. Several similar kind of analysis were reported about IGBT including both the trench gate[44][45] and planar gate[45], but those did not widely discuss expanding to the PIN diodes and MCT or thyristor related structures.

V-1. Trench MOS gated devices (IGBT, MCT) and diode

V-1-1. Simulated device structures

The trench gated MCT (T-MCT) was selected as the representative of the MOS-bipolar power devices whose ON state performance is governed by thyristor-based operational physics while the trench gated IGBT (T-IGBT) was chosen as the representative of MOS-bipolar power devices whose ON state performance is governed by transistor-based operational physics. The ON state characteristics of these devices were analyzed by performing the two-dimensional numerical simulations using MEDICI, which is numerical device simulator software. The ON state characteristics of the T-IGBT and the T-MCT were compared to that of PIN diodes, which are with and without a trench region, because it is considered as the ideal device from the ON state point of view[21].

In the unit cell designs of the T-MCT, the T-IGBT and the PIN diode, a 550μm thick N^- drift region with a uniform doping level of $2 \times 10^{13} cm^{-3}$ was chosen to obtain a cell voltage blocking capability of over 4500 V. In order to obtain an acceptable ON state voltage drop for these high voltage device structures, a large high injection level lifetime τ_{HL} of 60μs ($\tau_{n0} = \tau_{p0} = 30\mu s$) is used in the N^- drift region. A 15μm deep N-type diffusion having a Gaussian profile was formed on the backside to realize the N^+ buffer region required to obtain the 4500V PT (Punch Through) type devices. The peak donor concentration in the 10μm thick buffer region was $5.9 \times 10^{16} cm^{-3}$. The P^+ collector/anode diffusion also had a Gaussian profile with a surface concentration of $1 \times 10^{18} cm^{-3}$ and a junction depth of 5μm. A shallow anode junction with low surface concentration and an N^+ buffer region were chosen as this combination has resulted in improved trade-off relationship between ON state forward voltage drop V_{on} and t_f (turn-off fall time) characteristics. The half cell and a half mesa width of the trench gate MOS-Bipolar power devices were 3μm and 1.5μm, respectively. The

half-width of the trench gate region was 1.5μm with a MOS-gate oxide thickness of 75nm along the trench sidewalls and bottom. To study the effects of cathode injection efficiency alone, the anode structure was kept identical in all the devices to ensure equal anode injection efficiency.

V-1-2. PIN diodes

The effect of cathode injection efficiency on the ON state voltage drop of a conventional PIN and trench PIN diode was studied by independently varying the surface concentration and the junction depth of the N^+ (cathode) diffusion. Cross-sections of the unit cells for diodes are illustrated in Fig. V-1-1.

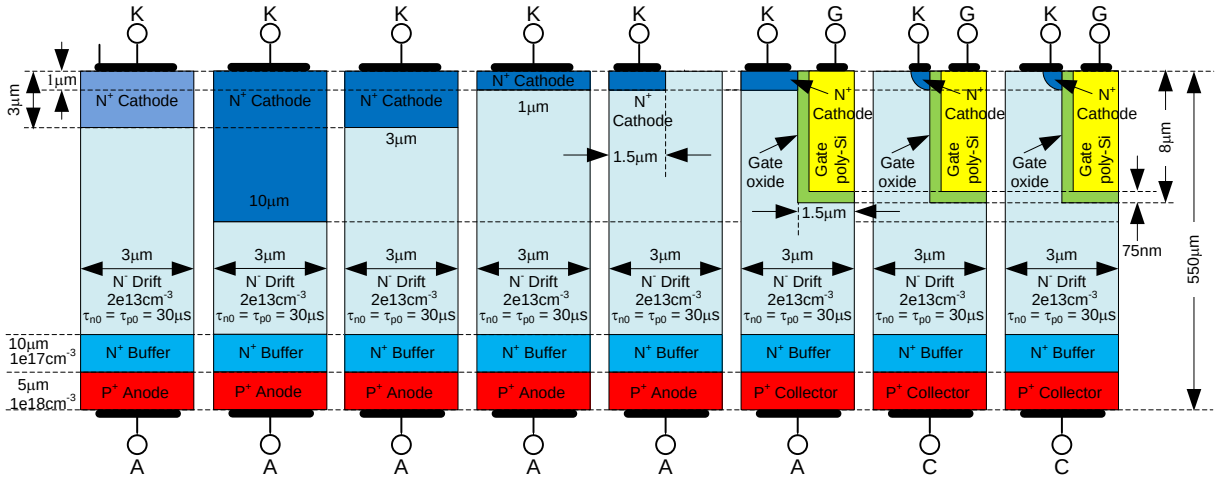


Fig. V-1-1. Schematic cross-sectional views of a half unit cell the PIN diodes and the TGDs (Trench-Gated Diodes) used in numerical simulations[42]

Table V-1-1. A summary of design parameters and numerical simulation results for all the diode structures[42]

Device Name	PIN-A	PIN-B	PIN-C	PIN-D	PIN-E	PIN-F	PIN-G	PIN-H	PIN-I	PIN-J	TGD-A	TGD-B	TGD-C
Cathode Area (%)	100						100			50	50	37.5	37.5
Cathode Depth (um)	1						10	3	1	1	1		
Cathode Conc.(cm-3)	1.0E+19	5.0E+18	1.0E+18	1.0E+17	1.0E+16	1.0E+15	1.8E+19			1.8E+19	2E+19		
ON-state voltage (V)	1.88	1.93	2.06	2.40	3.14	3.98	1.56	1.70	1.84	1.85	1.74	1.74	2.28
Iek ratio (%)	72.04	71.76	71.21	70.50	69.84	69.48	80.78	74.19	72.31	72.28	73.20	73.14	70.43
Iek ($X10^{-6}$) (A/um)	2.161	2.153	2.136	2.115	2.095	2.084	2.423	2.226	2.169	2.168	2.196	2.194	2.113
Ihk ($X10^{-6}$) (A/um)	0.839	0.847	0.864	0.885	0.905	0.916	0.577	0.774	0.831	0.832	0.804	0.806	0.057

For the conventional diode structures (PIN-A through PIN-F) of Fig. V-1-1 (a), the surface concentration of the N^+ cathode diffusion was decreased logarithmically from 1 x $10^{19}cm^{-3}$ to 1 x $10^{15}cm^{-3}$ in steps of one decade keeping the junction depth fixed at 1μm as described in more detail in Table V-1-1. On decreasing the cathode surface concentration, the cathode injection efficiency (defined as the ratio of the electron current to the total current at the cathode metal) was found to reduce from 72.04% to 69.48% with a corresponding increase in the ON state voltage drop (at an anode current density of $100A/cm^2$ from 1.88V to 3.98V. Similarly, on increasing the N^+ cathode junction depth from 1μm to 10μm with the surface concentration fixed at 1.8 x $10^{19}cm^{-3}$ (PIN-G through PIN-I), the cathode injection efficiency increased from 72.31% (for PIN-I) to 80.78% (for PIN-G) with a corresponding reduction in the ON state voltage drop from

1.84V to 1.56V as described in more detail in Table V-1-1. These results are consistent with the fact that with higher cathode injection efficiency, larger concentration of electrons is injected from the N^+ cathode into the N^- drift region in the ON state of the diode. Therefore, to maintain charge neutrality, the N^- drift region is simultaneously flooded with a higher concentration of holes.

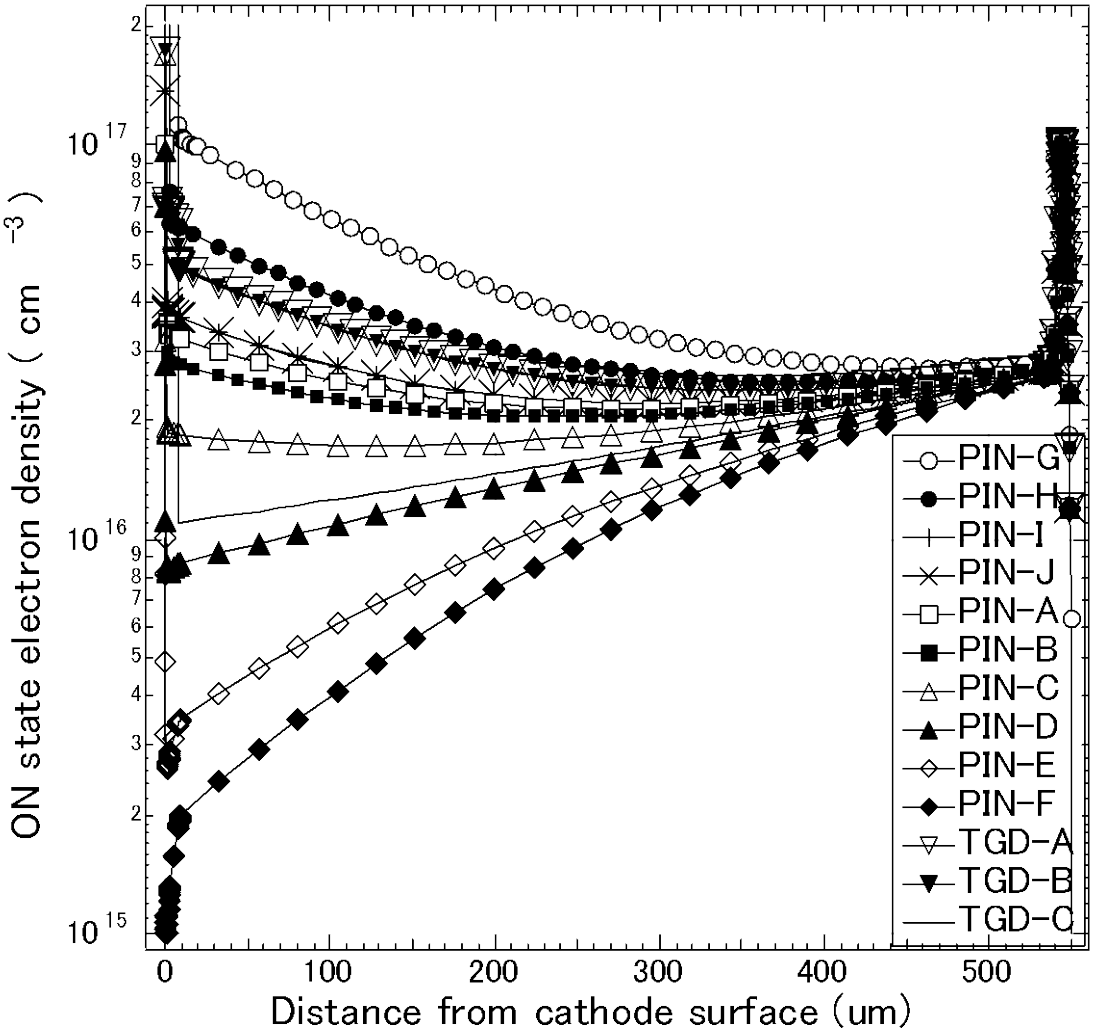


Fig. V-1-2. Variation of the ON state electron density in the N^- drift region of all the diode structures As far as the conductivity modulation being occurred, the amount of electrons and holes are identical[42].

This results in an increase in the conductivity modulation in the N^- drift region as shown by the electron distribution in Fig. V-1-2. Hence, the component of the mid region (N^- drift region) voltage drop associated with the transport of the injected holes is reduced resulting in a decrease in the ON state voltage drop. However, the mid-region drop becomes small at very high excess carrier concentration in the N^- drift region and the diode voltage drop is then dominated by the drop across the N^+/N^- drift junction and the N^+ buffer/P^+ junctions.

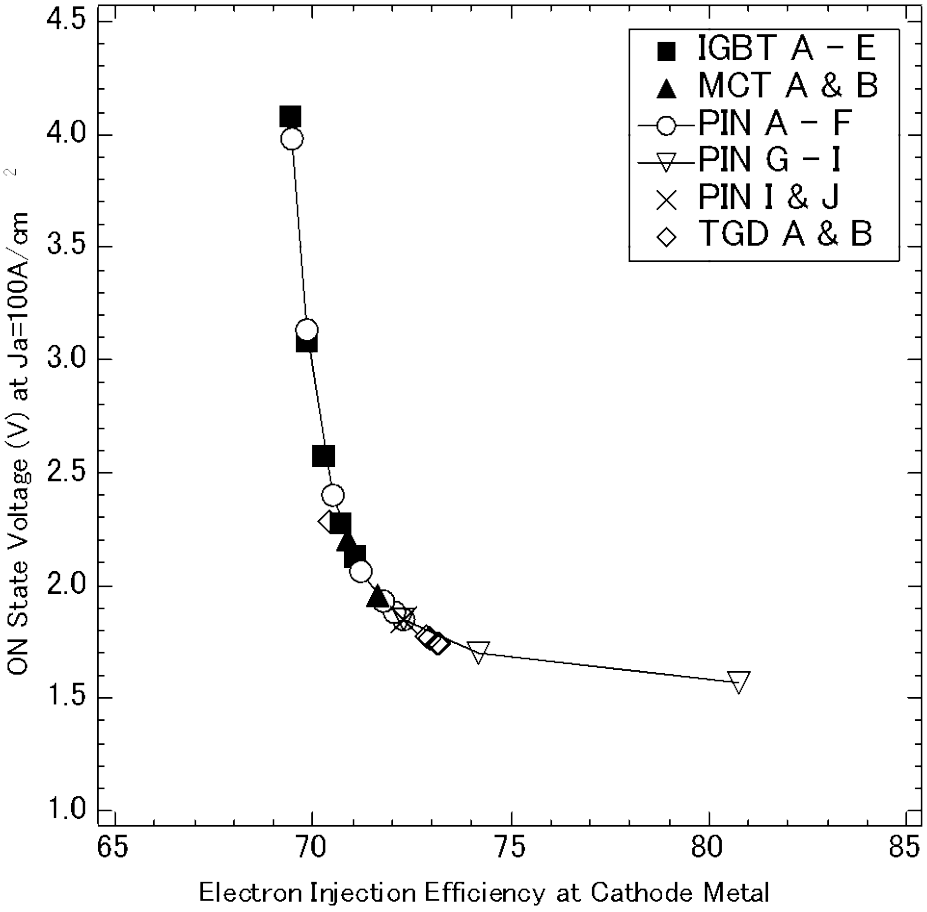


Fig. V-1-3. A unified curve representing the variation of the ON state forward voltage drop with the injection efficiency on the cathode-side applicable to all the bipolar power devices[42]

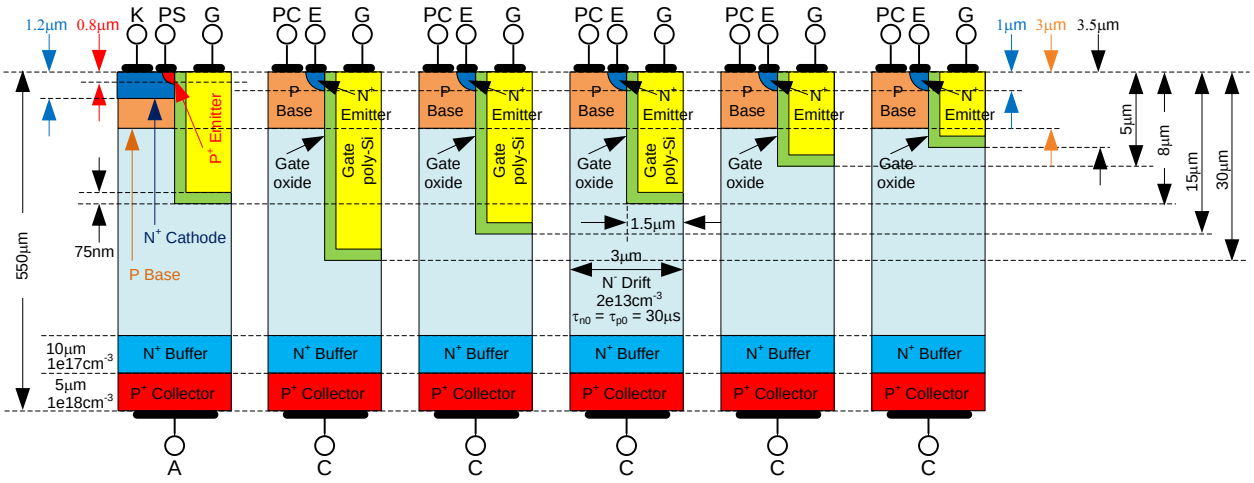
Therefore, there is no appreciable decrease in the ON state voltage drop for cathode injection efficiencies greater than 75% as shown in Fig. V-1-3.

Simulations were also performed to analyze the effect of changes in the cathode area of the PIN diode (PIN-J) by altering the length (L_{N+}) in the cell structure shown in Fig. V-1-1 (b). For the same N^+ cathode junction depth and surface concentration, it was found that the ON state voltage drop of the PIN diode is unaffected by the changes in the cathode area. The values of the cathode injection efficiency, forward voltage drop, the electron and the hole current density at the cathode terminal for a PIN diode obtained by varying the N^+ (cathode) parameters are provided in Table V-1-1.

The trench PIN diode unit cell cross-sections (TGD-A and TGD-B) shown in Fig. V-1-1 (c) and Fig. V-1-1 (d) were used to emulate the N^+ cathode in the T-MCT and the N^+ emitter in the self-aligned T-IGBT designs. These two diodes will be referred to as the trench gated diode (TGD-A) and self-aligned trench gated diode (TGD-B), respectively. With the gates bias at 15 V, the trench gated diodes with a 1μm deep N^+ cathode and a surface concentration of $1.8 \times 10^{19} cm^{-3}$ had an ON state voltage drop of 1.74V with a corresponding cathode injection efficiency of 73.2%. For the same cathode parameters, the injection efficiency on the cathode-side was observed to be higher than for the conventional PIN diode (PIN-I). This results in an increased conductivity of the N^- drift region as seen in Fig. 2 and consequently a lower forward voltage drop. In addition,

the ON state performance of another variant of the self-aligned trench diode structure (TGD-C), shown in Fig. V-1-1 (e) was numerically analyzed. In this structure, the cathode metal contacts both the N-drift region and the N^+ cathode region. This diode (TGD-C) had an ON state voltage drop of 2.28V and a cathode injection efficiency of 70.43 % with a gate bias of 15V. The diode TGD-C has a higher ON state voltage drop as compared to other diodes with the same cathode parameters because of poor conductivity modulation of the N^- drift region as seen in Fig. V-1-2. This occurs due to the excess carrier concentration being forced to zero at the metal contact in the N-drift region by the ohmic boundary conditions applied at the contact.

V-1-3. Trench MOS-controlled thyristor (T-MCT)



T-MCT-A, B T-IGBT-A T-IGBT-B T-IGBT-C T-IGBT-D T-IGBT-E

Fig. V-1-4. Unit Cell cross-sections of 4500V class T-MCT and the T-IGBT used in simulation[42]

The ON state performance of a trench MOS-Controlled Thyristor (T-MCT) was obtained through a numerical analysis of the unit half-cell shown in Fig. V-1-4 (a). The triple diffusions in the MCT were obtained by using a 3µm deep P-base region having a surface concentration of $2.2 \times 10^{17} cm^{-3}$, a 1.2µm deep N-base with a surface concentration of $8.8 \times 10^{18} cm^{-3}$ and a 0.8µm deep self-aligned P^+ region with a surface concentration of $6.5 \times 10^{19} cm^{-3}$. These parameters were chosen to produce a maximum acceptor concentration of $2 \times 10^{16} cm^{-3}$ below the N-base region along the trench sidewall and a maximum donor concentration of $1.5 \times 10^{17} cm^{-3}$ below the P^+ region along the trench sidewall. Thus, for a gate oxide thickness of 75nm, both the threshold voltages of a 1.8µm long, N-channel MOSFET (formed in the ON state of the MCT) and a 0.4µm long, P-channel MOSFET (formed during turn-off of the MCT) were approximately 3V.

Table V-1-2. A summary of the design parameters and simulation results for all the T-MCTs and T-IGBTs[42]

Device Name		MCT-A	MCT-B	IGBT-A	IGBT-B	IGBT-C	IGBT-D	IGBT-E
Cathode Conc.	(cm-3)	8.8E+18	8.7E+16	1E+19				
Trench Depth	(um)	8		30	15	8	5	3.5
ON-state voltage	(V)	1.99	2.21	2.13	2.28	2.57	3.08	4.08
Iek ratio	(%)	71.80	70.87	71.09	70.70	70.27	69.85	69.40
Iek (X10^{-6})	(A/um)	2.154	2.126	2.133	2.121	2.108	2.096	2.082
Ihk (X10^{-6})	(A/um)	0.065	0.074	0.000	0.000	0.000	0.000	0.000
Ihp+cont (X10^{-6})	(A/um)	0.781	0.800	0.867	0.879	0.892	0.905	0.918

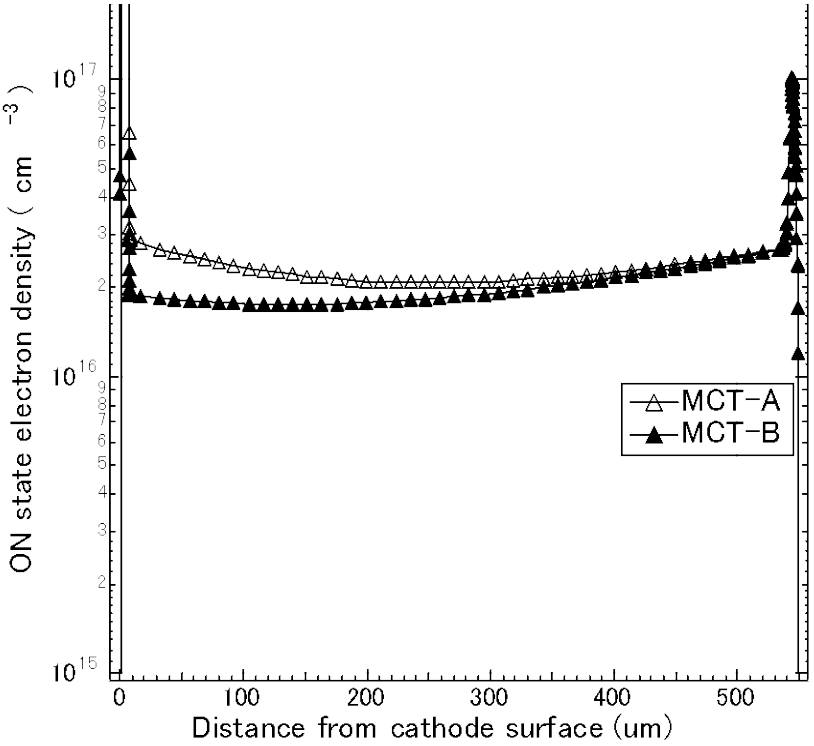


Fig. V-1-5. Variation of the ON state electron density in the N-drift region for the Trench MOS-Controlled Thyristor designs MCT-A and MCT-B[42].

The ON state voltage drop of the T-MCT (design MCT-A) was observed to be about 1.99V with a corresponding cathode injection efficiency of about 71.8%. The forward voltage drop for the MCT is low and comparable to a PIN diode because, in the ON state, the PNP transistor is operating in saturation mode with the collector-base junction (P-base/N-drift junction) forward biased. This results in a PIN diode-like excess carrier distribution in the N-drift region as shown in Fig. V-1-5. However, on reducing the cathode surface concentration to 8.7 x 10^{16}cm^{-3} (in design MCT-B), the cathode injection efficiency reduced to 70.87% with a corresponding increase in the forward voltage drop to 2.21V. Lower cathode injection efficiency causes a reduction in the conductivity modulation of the N-drift region (as shown in Fig. V-1-5) which results in an increase in the ON state voltage drop. The forward voltage drop of a T-MCT (1.99V for design MCT-A) can be made comparable to that of a PIN diode (1.56V for design PIN-G) by increasing the cathode injection efficiency. However, altering the N-base parameters to realize higher cathode injection efficiencies makes the task of realizing the triple diffused T-MCT structure exceedingly difficult. Further, the cathode-side injection

efficiency in the MCT is reduced by the presence of a parasitic PNP transistor. Therefore, due to practical considerations, the performance of the T-MCT cannot be made on par with a PIN diode. These results are summarized in Table V-1- 2 for ease of comparison.

V-1-4. T-IGBT

The unit half-cell of a T-IGBT used in numerical simulations is shown in Fig. V-1-4 (b). The double diffusion junctions in the T-IGBT were obtained using a 3 um deep P-base region with a surface concentration of 2.2 x $10^{17}cm^{-3}$ and a 1μm deep, N^+ emitter region with a surface concentration of 1 x $10^{19}cm^{-3}$. These parameters were chosen so that the threshold voltage of the T-IGBT is around 3V for a gate oxide thickness of 75nm. For a 5μm deep trench IGBT (IGBT-D), the ON state voltage drop was observed to be 3.08V with a corresponding cathode injection efficiency of 69.85%. Furthermore, the cathode injection efficiency increased from 69.4% to 70.7% with an increase in the trench depth from 3.5μm (IGBT-E) to 15μm (IGBT-B) accompanied by a decrease in the forward voltage drop from 4.08V to 2.28V as indicated in Table IV-1-2. The observed increase in the cathode injection efficiency and a reduction in ON state voltage drop with trench depth are consistent with the data reported in the literature[46].

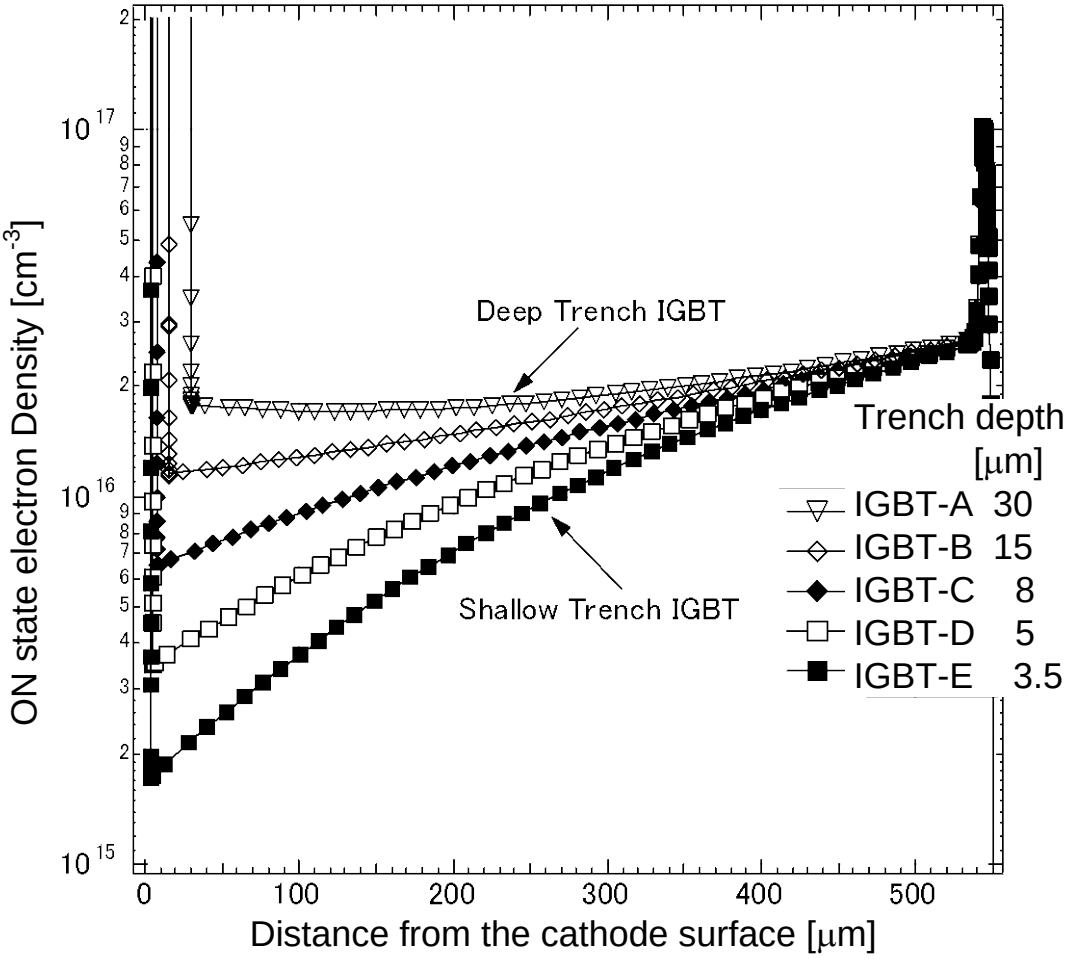


Fig. V-1-6. Variation of the ON state electron density in the N-drift region for the Trench Insulated Gate Bipolar Transistor (T-IGBT) designs IGBT-A, IGBT-B, IGBT-C, IGBT-D and IGBT-E[42]

With increasing cathode injection efficiency, a higher concentration of electrons is injected into the N-drift region resulting in an increase in the conductivity modulation of the N-drift region for deeper trench design as shown in Fig. V-1-6. However, in contrast to the T-MCT, the PNP transistor of the T-IGBT operates in the forward active mode and the reverse biased collector base junction (P-base/N-drift) junction forces the excess carrier concentration at the P-base/N-drift region to zero. Hence, due to a poor conductivity modulation of the N-drift region near the cathode as shown in Fig. V-1-6, the T-IGBT has a higher ON state voltage drop than the T-MCT. A summary of these results is provided in Table V-1-2 for ease of comparison.

V-1-5. Summary of V_{on}

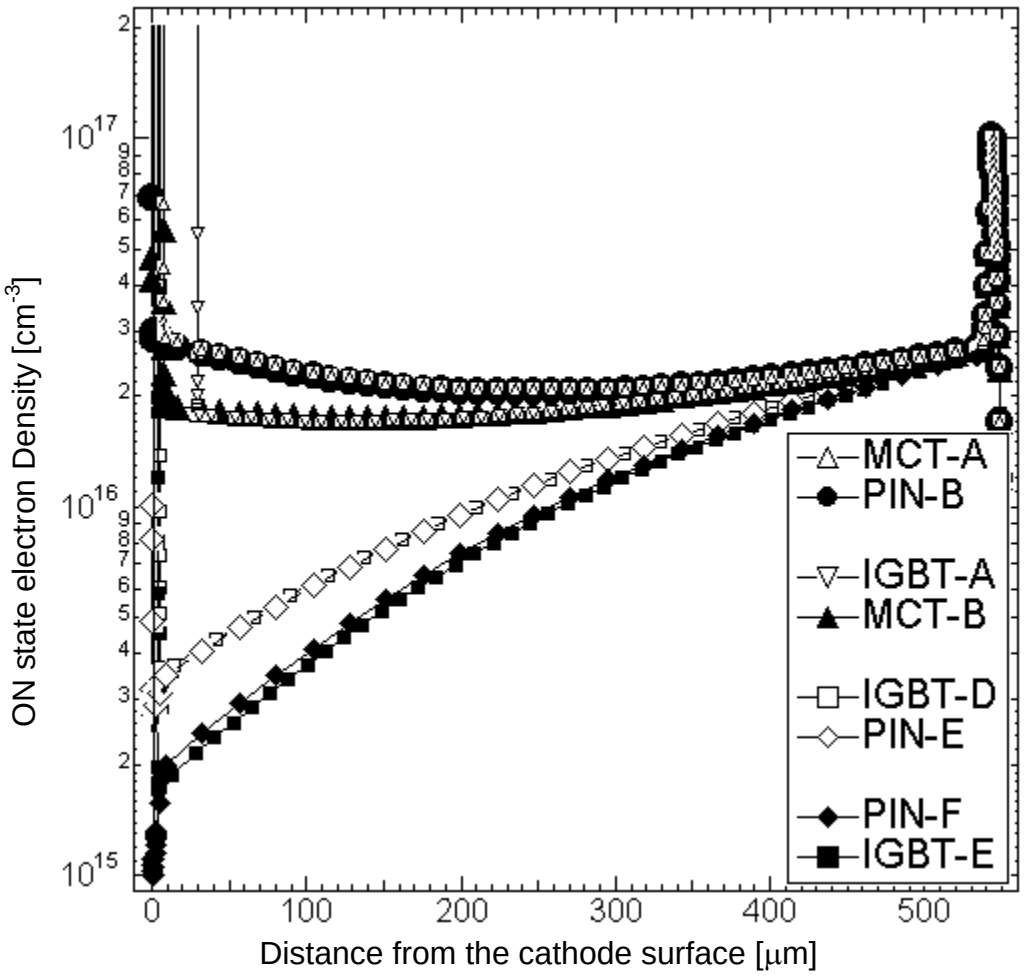


Fig. V-1-7. Comparison of ON state electron distribution in the N-drift region for the T-IGBT and T-MCT designs with PIN diodes that have equal cathode-side injection efficiency[42].

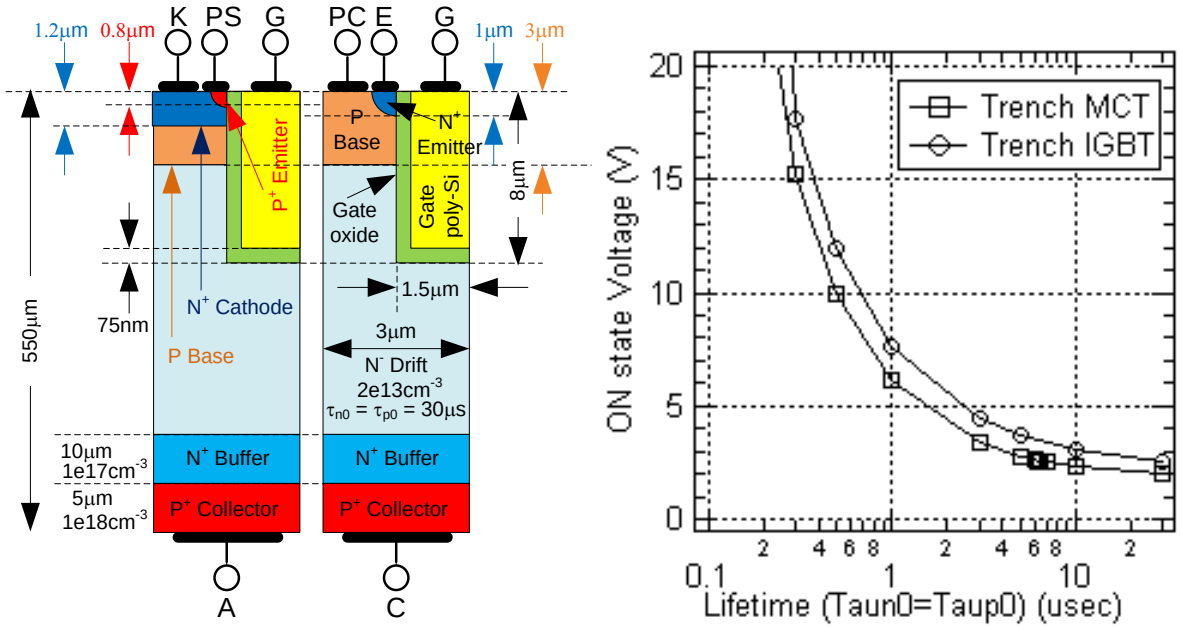
Within the family of MOS-gated bipolar devices, the IGBT and the MCT have been regarded as fundamentally different structures because the PNP transistor in the IGBT operates in the forward active mode with the collector-base (P-base/N-drift junction) reverse biased while that in the MCT operates in saturation with the collector-base junction forward biased. This produces the differences in the performance of the MCT and the IGBT. However, when the cathode injection efficiency was chosen to be as a parameter, it was

discovered that both the IGBT and the MCT, including their design variations, could all be mapped on a single curve shown in Fig. V-1-3, which represents the behavior, obtained for a PIN diode. Thus, a single universal curve can be used to determine the ON state voltage drop for all these devices when the cathode injection efficiency is used as a parameter. Furthermore, it was found that the excess carrier distribution within all these devices becomes identical in the case of equal cathode injection efficiency. Examples illustrating this behavior are shown in Fig. V-1-7. It can be seen that a 3.5μm-deep T-IGBT design (IGBT-E) is equivalent to a conventional PIN diode (PIN-F) with a 1 um-deep cathode having a surface concentration of $1 \times 10^{15} cm^{-3}$ (with a junction depth of 1μm) because they have an identical cathode injection efficiency of 69.4%. Similarly, a 5μm-deep T-IGBT design (IGBT-D) is equivalent to a conventional PIN diode (PIN-E) with a 1μm-deep cathode with a surface concentration of $1 \times 10^{16} cm^{-3}$ because they have an identical cathode injection efficiency of 69.8%. Thus, in the on state, each of the T-IGBT designs can be considered to perform as an equivalent conventional PIN diode having cathode injection efficiency identical to the T-IGBT design. Further, the T-MCT (MCT-A) is equivalent to a conventional PIN diode (PIN-B) with a 1μm-deep cathode with a surface concentration of $5 \times 10^{18} cm^{-3}$ because they have an identical cathode injection efficiency of 71.8%. In addition, the T-IGBT with a trench depth of 30μm (IGBT-A) is equivalent to the design MCT-B because they have an identical cathode injection efficiency of 71%. Although, the above T-IGBT design cannot support 4500V in the off-state, it is presented here for illustrating that if the cathode injection efficiencies of the transistor based device (T-IGBT) is equal to a thyristor based device (T-MCT), then their ON state performance and the excess carrier distribution in the N-drift region are identical.

In conclusion, a unified treatment of the IGBT and the MOS-gated thyristor is possible when the cathode injection efficiency is used as the parameter. It has been found that a single universal curve can be used to determine the ON state voltage drop of all the devices, irrespective of the differences in the operational physics that exist between the fundamentally different structures of an IGBT and MOS-Gated Thyristors. Furthermore, for the same cathode injection efficiency, the ON state voltage drop and the excess carrier distribution for all the devices are shown to be identical. Due to practical constraints associated with deep trench designs (greater than 15 um), the cathode-side injection efficiency of the T-IGBT will lie in the range of 69.4% to 70.7%. Consequently, the ON state performance of the T-IGBT cannot be made on par with the T-MCT having a cathode-side injection efficiency of 71.8% (MCT-A). Similarly, the performance of the T-MCT cannot be made on par with the conventional PIN diode due to the presence of the parasitic PNP transistor which limits the cathode-side injection efficiency of the T-MCT in the range of 70.87% to 71.8%. Thus, improvements in the ON state performance of the T-IGBT will be restricted to the upper part of the universal curve corresponding to lower cathode injection efficiencies while the ON state performance of the T-MCT cannot be pushed to the lower part of the universal curve corresponding to higher cathode injection efficiencies.

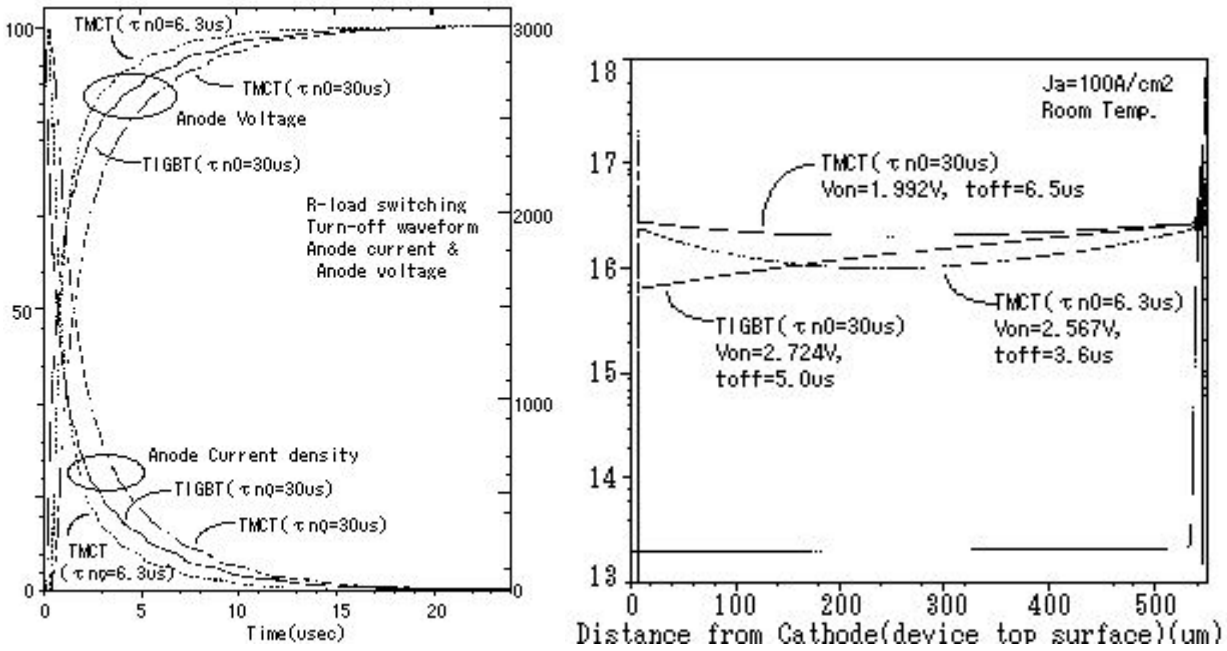
V-1-6. V_{on}-E_{off} trade-off

Direct comparison between T-IGBT and T-MCT is useful to confirm that the device with higher cathode side electron injection efficiency shows the better V_{on}-E_{off} tradeoff.



(a) Structures (b) carrier lifetime dependence of V_{on}

Fig. V-1-8. Carrier lifetime dependence of V_{on} for both T-IGBT & T-MCT[42]



(a) R-load turn-off waveforms (b) carrier profiles

Fig. V-1-9. Carrier profile and turn-off waveforms for both T-IGBT & T-MCT[42]

All the structural parameters are same for both T-IGBT and T-MCT except the transistor and thyristor action parts, as shown in Fig. V-1-8 (a). T-MCT's Von is lower than T-IGBT's in the entire lifetime region, as shown in Fig. V-1-8 (b), without any cross-point. From this Fig. V-1-8 (b), it is carefully chosen for the T-MCT's lifetime parameter of 6.3μs to have an almost same V_{on} of 2.567V as T-IGBT's V_{on} of 2.724V whose lifetime is 30μs long enough. T-MCT with shorter lifetime of 6.3μs has the smallest tail current as shown in Fig. V-1-9 (a) in spite of a little lower V_{on} of 2.567V than T-IGBT's V_{on} of 2.724V. As shown in Fig. V-1-9 (b),

T-MCT with shorter lifetime of 6.3 μs has a better symmetrical carrier profile than T-IGBT with longer lifetime of 30μs. Because of T-MCT's lifetime being shorter, T-MCT's carrier density around the anode side is lower than T-IGBT's one. But T-MCT's carrier density around the cathode side is higher than T-IGBT's, because T-MCT structure has originally higher electron injection efficiency discussed above. So, it is clearly shown that the higher electron injection efficiency device has the better Von-Eoff tradeoff, as far as the anode side structure is fixed.

As described in the previous chapter, both the middle voltage class of 1200V and the low voltage class of 600V devices had been using Epitaxial wafer as the starting material, there were no room to optimize the collector backside structure. In conclusion, as far as the V_{on}-E_{off} trade-off relationship is concerned, "the electron injection efficiency" in the control gate side is the good "design index".

V-2. Junction gate devices : SIThy and GTO

V-2-1. Background

Using numerical device simulation, the SIThy[47][48][49][50], which is a kind of SI (Static Induction) device[51][52] and is also called Field Controlled Diode (FCD), has the same low forward voltage drop V_{TM} (V_{TM} is local naming of V_{on} in Thyristor field) as a PIN diode by setting its doping concentration of a junction gate high enough and a channel region low. As the result, SIThy's carrier distribution is almost same as PIN diodes. On the other hand, GTO is also the forced turn-off type device, and its doping concentration of its gate is lower than SIThy's and uniformly distributed in the lateral direction, but it is a little higher than the conventional thyristor, with a small sacrifice of rising the ON state forward voltage drop. Those gate structural differences may change both GTO's carrier distribution of the ON state and the forward Vc-Ic characteristic from SIThy's. The trade-off between V_{TM}-E_{off} was improved by making higher doping concentration of SIThy's gate structure[53][54], because SIThy has a large electron injection from the cathode. To confirm the reason why SIThy's electron injection is greater than GTO's, it was analyzed that the relationship between gate structures and device characteristics of various types of SIThys and GTOs by using numerical device simulation.

V-2-2. Simulation condition and device structures

All the static and dynamic characteristics were numerically simulated by MEDICI, numerical device simulator. The device structures for both SIThy and GTO are adjusted for high voltage of 4500 V, and each current density is defined by anode size same manner as the mass production devices. The anode structure is carefully chosen as the anode-shorted structure that improves the trade-off between V_{TM}-t_f[43]. From the gate structure point of view, all the variation of SIThy's and GTO's structures are shown in Fig. V-2-1.

The carrier distribution profiles are represented by the electrons, not by the holes, because the amount of both electrons and holes are same as long as conductivity modulation is occurred. And it is easy to describe how large electrons are injected from cathode. If holes are used, its concentration is dropping down abruptly around the channel region surrounded by P-type gate region, since it not easy to understand the electron injection efficiency of the cathode. A peak doping concentration and a depth of P-type gate are represented by C_p and X_j respectively, and all the gate diffusion profiles are defined by Gaussian distribution.

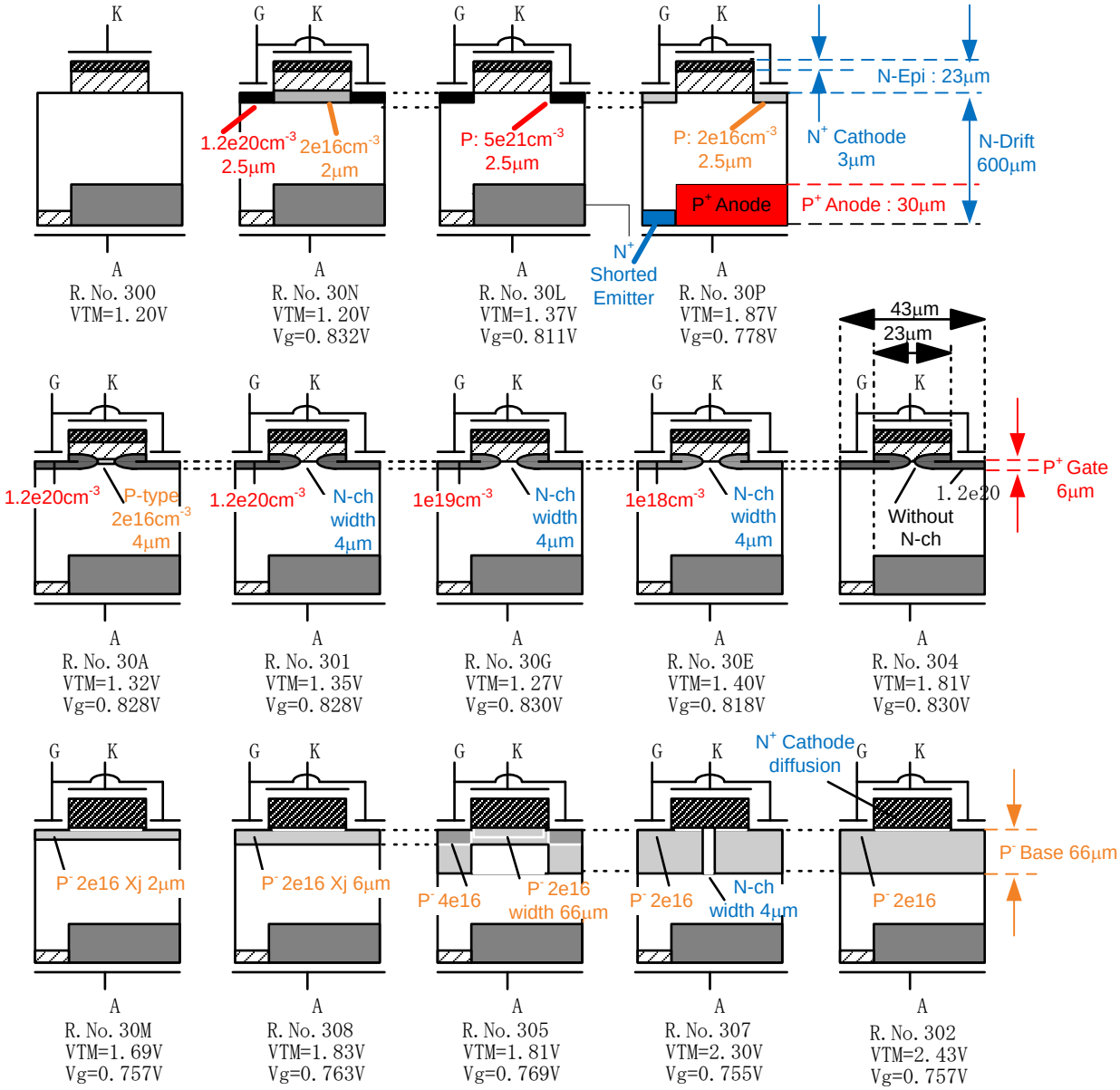


Fig. V-2-1. Schematic cross-section of unit cell structures used in the simulation of SIThys and GTOs[43]

V-2-3. Forward output Vc-Ic characteristics and carrier distributions

All the forward output V_c-I_c (V_a-I_a) characteristics and carrier distributions corresponding to various gate structures of both SIThys and GTOs at the ON state (Anode current density J_a is fixed at rated current density of 100 A/cm^2) are shown in Fig. V-2-1. From V_{TM} point of view, those are clearly divided into two groups, that is, Group 1 having very high C_p and Group 2 having relatively low C_p.

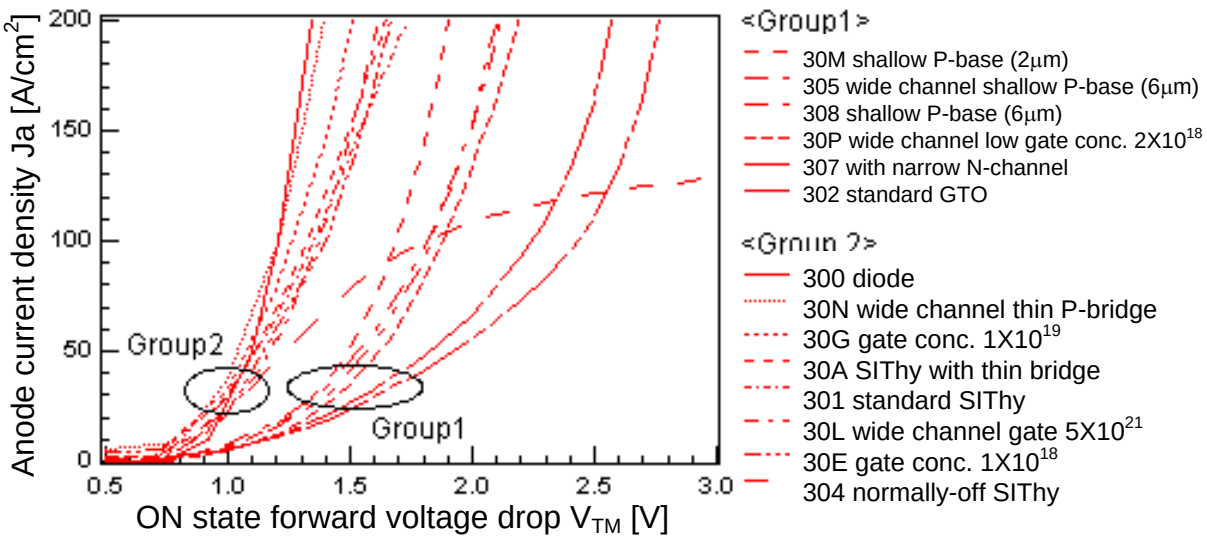
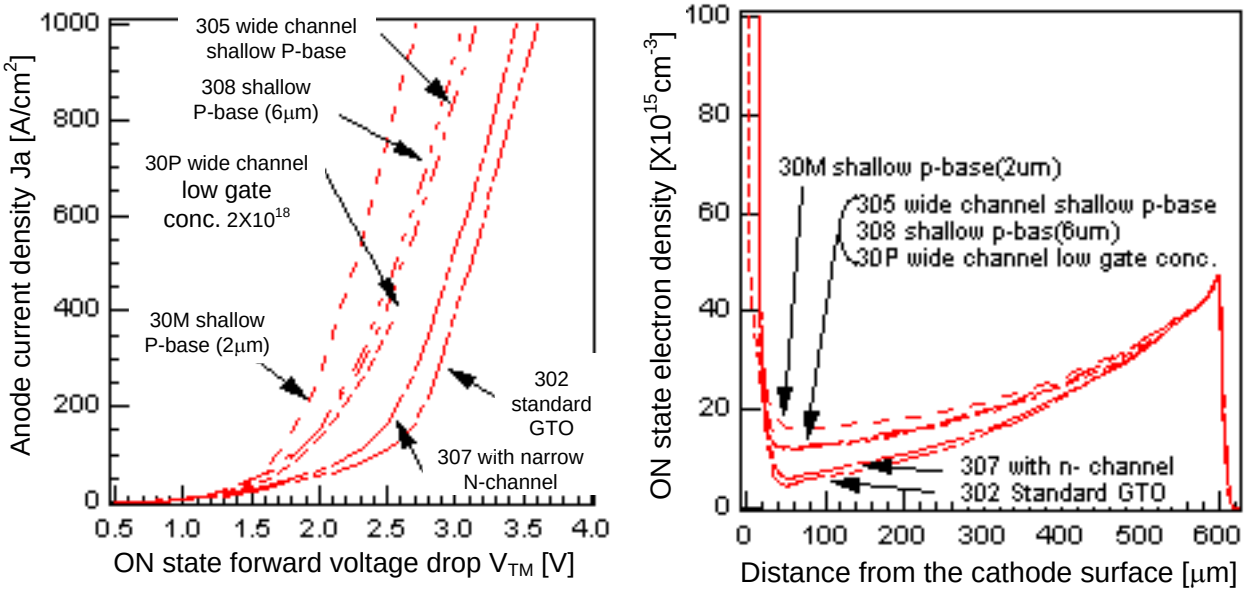


Fig. V-2-2. All the forward output Vc-Ic characteristics of SIThys and GTOs[43]

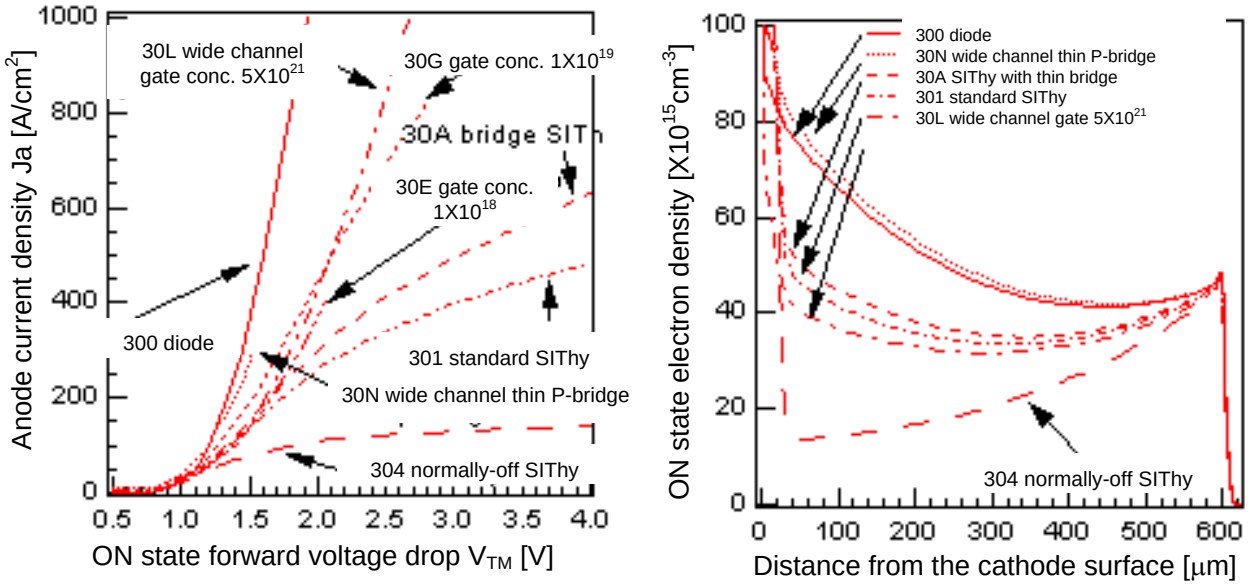
The C_p of Group 1 is in the range of 2 - 4 X $10^{16}cm^{-3}$. In the device structures whose X_j is shallow partially (structure No. 305: $X_{j(under\ cathode)}$ = 6μm, $X_{j(side\ gate)}$ = 66μm) or uniformly (structure No. 308: X_j = 6μm, 30M: X_j = 2μm), each V_{TM} is lower than V_{TM} of deep Xj devices like a typical GTO structure No. 302 whose X_j is uniformly deep as 66μm, but carrier concentration near the cathode is low as a typical GTO structure No. 302, shown in Fig. V-2-3 (b). Even in the device types having n^- channel surrounding by p^- gate region (structure No. 307: X_j = 66μm, and 30P: X_j = 2μm), it is kept this tendency that carrier concentration near the cathode is still low like a standard GTO and not improved in ON stated forward voltage drop so much.



(a) Output Vc-Ic characteristics (b) Carrier distributions at 100A/cm^2

Fig. V-2-3. The characteristics of SIThys and GTOs in group 1[43]

The C_p of low V_{TM} Group 2, shown in Fig. V-2-4, is more than 1 X 10^{18}cm^{-3} and the X_j is shallow around/or less than 6μm. As shown in Fig. V-2-4 (b), each carrier density of group 2 near the cathode is higher than anyone of group 1 except a normally-off type SITh structure No. 304, and is almost same as the simple diode structure No. 300. As long as the doping concentration of channel region is low and the main anode current density J_a is kept under the rated current density 100 A/cm^2, the forward output V_c-I_c characteristics are not affected by the doping type of a channel region, whether N$^-$ or P$^-$. The first example is comparing the typical SIThy structure No. 301 (C_p = 1.2 X 10^{20}cm^{-3}, X_j = 6μm) to the p$^-$ type lightly doped bridged structure No. 30A ($C_{p(bridge)}$ = 2 X 10^{16}cm^{-3}, $X_{j(bridge)}$ = 4μm), and the second one is also comparing the structure having relatively wide channel without rounded jet region but very shallow gate depth structure No. 30L (X_j = 2.5μm, $W_{channel}$ = 23μm; this too wide channel structure cannot support high voltage, so just for V_{TM} reference.) to p$^-$ bridged type for this structure No. 30N ($C_{p(bridge)}$ = 2 X 10^{16}cm^{-3}, $X_{j(bridge)}$ = 2.5μm: same depth as main gate portion).



(a) Output Vc-Ic characteristics (b) Carrier distributions at 100A/cm^2

Fig. V-2-4. The characteristics of SIThys and GTOs in group 2[43]

Though forward output V_c-I_c characteristics of typical wide channel ($W_{channel}$ = 4μm) structures No. 301 with typical P^{++} gate concentration ($C_{p(main\ gate)}$ = 1.2 X 10^{20}cm^{-3}), No. 30A with P$^-$ bridge ($C_{p(main\ gate)}$ = 1.2 X 10^{20}cm^{-3}, $X_{j(bridge)}$ = 2.5μm, $C_{p(main\ gate)}$ = 1.2 X 10^{20}cm^{-3}) in the channel region, and No. 30G with P$^-$ bridge in the channel region but relatively low C_p ($C_{p(main\ gate)}$ = 1 X 10^{19}cm^{-3}, $C_{p(bridge)}$ = 2 X 10^{16}cm^{-3}, $X_{j(bridge)}$ = 2.5μm) do not saturate up to the rated current density 100A/cm^2, those forward output V_c–I_c characteristics start to saturate over 200A/cm^2. And, the normally-off type structure No. 304, which is shorter gate interval than No. 301 and has only the p$^-$ channel constructed by only the diffusion area from the typical SIThy's gate structure, shows a current saturation tendency in the forward output V_c- I_c characteristic over 50A/cm^2, and very similar ON state carrier density profile as group 1.

V-2-4. V_{on}-E_{off} tradeoff

As V_{TM} -E_{off} tradeoff is shown in Fig.V-2-5, the typical SIThy structure No. 301 in group 2 has better trade-off relationship than the typical GTO's one in group 1. These trade-off curves are obtained by changing an ambipolar carrier lifetime τ_{HL} in high level injection.

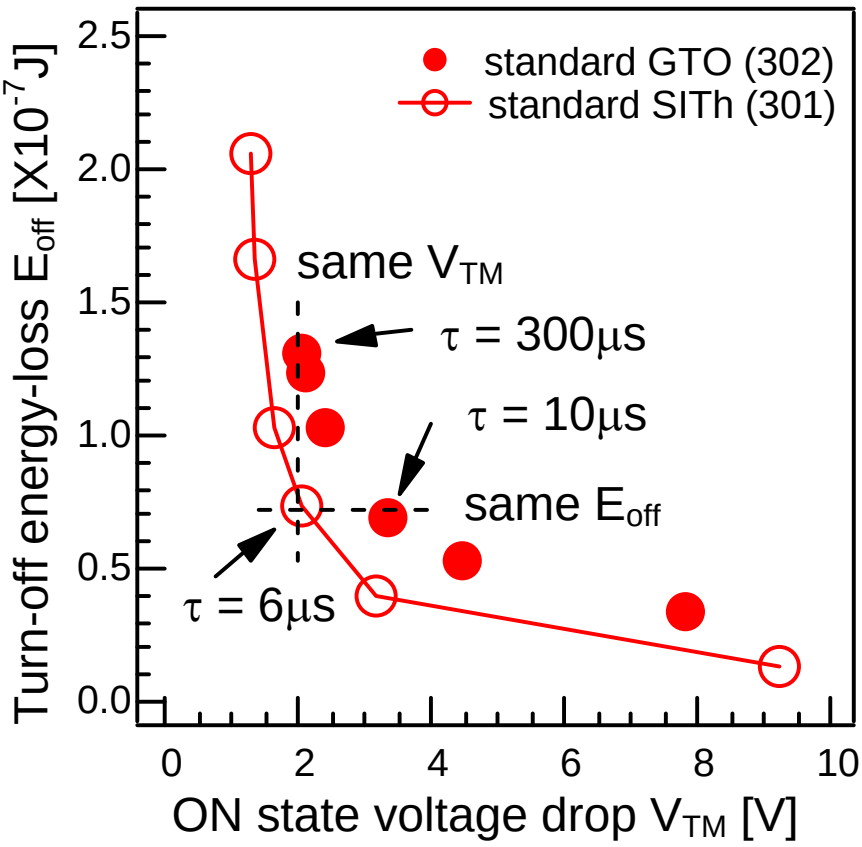
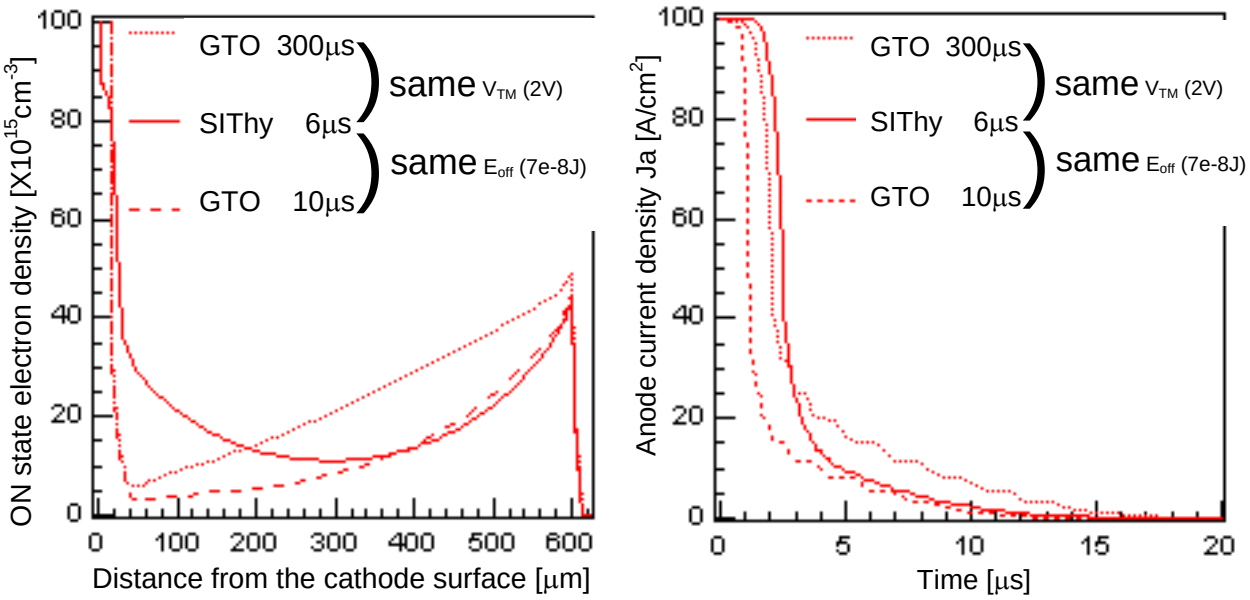


Fig. V-2-5. V_{TM} -E_{off} tradeoff curves of the typical SIThy No. 301 in group 2 and the typical GTO[43]

In comparison with the typical SIThy's and the typical GTO's carrier distribution having same V_{TM} (τ_{HL} is different) in the trade-off curves of V_{TM}-E_{off} shown in Fig. V-2-5, it is clear that this SIThy's stored charge near its cathode is higher than this GTO's one shown in Fig. V-2-6 (a). The carrier distribution profile of this SIThy is balanced shape, in which the carrier density height of both cathode and anode end is almost same like a hanging bridge and both electrons and holes flow smoothly by drift and diffusion. On the other hands, near the anode region, this GTO has large excess carrier to sweep out in its final step of the turn off time period, i.e. this GTO has larger E_{off} than SIThy does. In the same manner, comparing the SIThy and GTO having the same E_{off} value in the trade-off curve in Fig. V-2-5, it is also clear that SIThy's stored charge near its anode is almost same as that GTO's but only that SIThy's stored charge near its cathode is higher than that of GTO's.



(a) Carrier distributions at 100A/cm^2 (b) turn-off J_a waveforms

Fig. V-2-6. Carrier distribution having same V_{TM} in the trade-off curves of V_{TM} -E_{off} shown in Fig. V-2-5[43]

The E_{off} which is only the anode current energy loss in the resistive loaded main circuit is divided into three timing parts, that is, (1) storage time period, (2) anode current falling period, and (3) tail current period, in the anode current waveform. In the first time period, (1) storage time period, the anode current loss is negligible. But, in the real circuit including gate driver circuit, a reverse biased Gate-Cathode driving current is needed to sweep out the stored charge around gate structure to build space charge region up. According to the storage time length, this gate driving current increases total electric energy loss in a system. In the second time period, (2) anode current falling period, the anode current-voltage power reaches the peak value. The anode current energy loss is as large as the following tail time period value. This energy loss is independent from various device structures described in Fig. V-2-6 (b). In the third time period, (3) tail current period, the anode voltage and the anode tail current, which corresponds the several percentage of the rated anode current, produces relatively large energy loss. And this tail current energy loss strongly depends on both the device structure and the ambipolar carrier lifetime representing the residual stored charge distribution in the neutral region near the anode electrode.

Comparing typical SIThy's and typical GTO's carrier distribution profile in the ON state at the same V_{TM} value, typical GTO has much larger stored charge near anode region in the n- base body. This excess carrier around anode region increases the tail current energy loss and causes the total energy loss larger than SIThy's one. On the other hand, at the same E_{off} condition, both SIThy and typical GTO have almost same amount of the excess carrier near the anode regions. But the typical SIThy with the larger stored charge near the cathode region has the lower V_{TM} value. Those are clear to compare three turn-off waveforms shown in Fig. V-2-6 (b).

V-2-5. Gate potential effect on V_{on}

Carrier density of typical SIThy No.301 near the cathode is higher than that of typical GTO No. 302, and V_{TM} -E_{off} of typical SIThy is better than that of typical GTO. It is originated in the gate potential V_g effect for the carrier distribution profile.

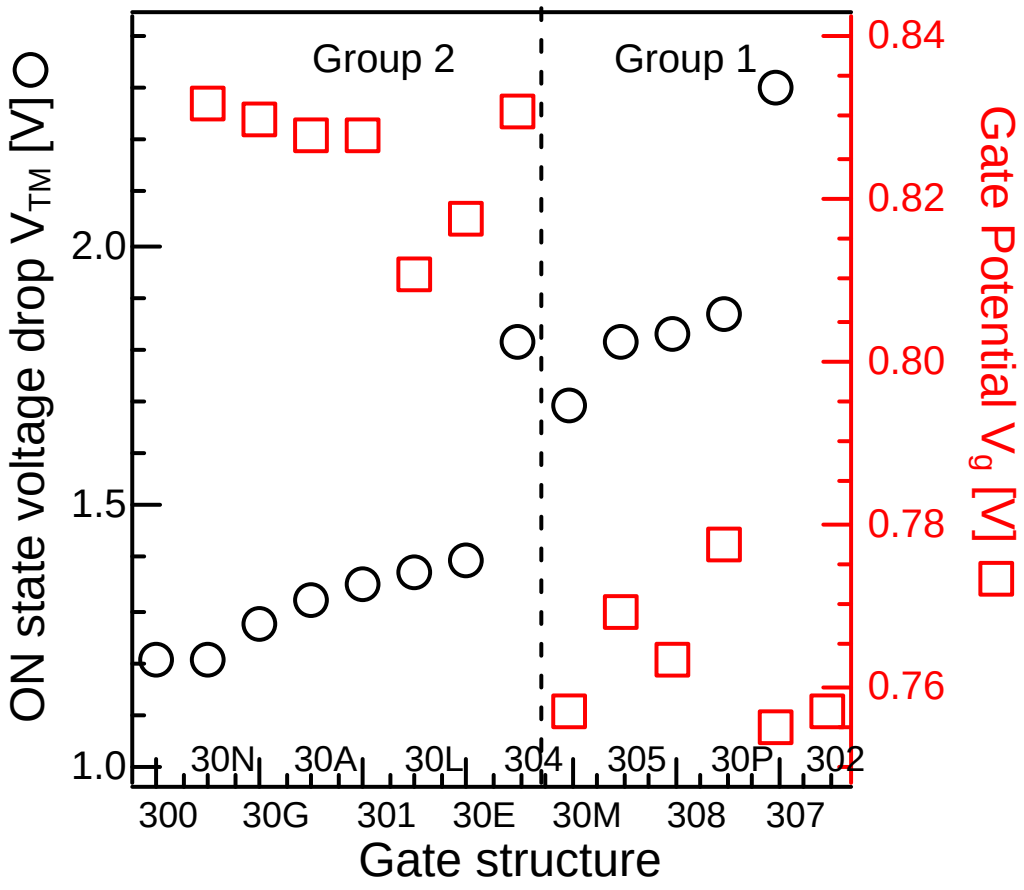


Fig. V-2-7. V_{TM} and V_g classification for all the SIThys and GTOs[43]

The same classification shown in Fig. V-2-7 can be done for both V_g and V_{TM} as the grouping of the forward V_c-I_c characteristics in Fig. V-2-2. It is obvious that, if the *Vg* value of SIT of SIThy or P-base of NPN transistor in GTO is pushed up at 0.1V for any structure of SIThy or GTO like ones, the amount of the electron injection from the cathode is drastically improved.

The next consideration is V_{TM} differences inside of the group 2 having high V_g value. As shown in Fig. V-2-7, each No. 30P, 30L, and 30N structure is standing on the V_g ascending line, and on a V_{TM} descending line respectively. Here, No. 30N structure has p gate jet portion under the cathode but 30L does not, and 30P structure has very low C_p concentration in four orders. Moreover, the structure No. 30N with p-bridge, which does not interfere the current flow through the channel region, has lower V_{TM} than 30L and almost same ON state characteristics of simple diode, because of relatively high V_g potential realized by high doping concentration of C_p drawing down the potential barrier for the electron even in the p-bridge region in contrast with uniformly low C_p concentration gate structure of No. 30L.

On the other hands, comparing typical SIThy structure No. 301, normally off type SIThy structure No. 304, and low and uniform doping concentration structure No. 308, V_g potential of No. 304 is as high as one of No. 301, but V_{TM} of No. 304 is worse than No. 301 and almost same as No. 308. That is because structure No. 304 does not have so widely spread low-doping concentration region, where the doping concentration is low under 2 X 10^{16}cm^{-3}, unlike No. 301, and all the main current flows through relatively high doping concentration

region, where the doping concentration is around 1 X $10^{17}cm^{-3}$ and higher than the injected electron density from the cathode. This is the evidence that both the channel width of the main current flow and the doping concentration at the channel region should be taken account for the factor to define the V_{TM} value. However, V_g potential is still dominant to compare the shallow and uniform doping concentration structure No. 308 and the normally of type SIThy No. 304, that is, No. 304 gets high V_g potential value from high doping concentration potion and low doping concentration in the normally off channel region.

V-2-6. Summary of simulation result

It is certified that SIThy's high carrier density near the cathode is realized by high gate potential coming from high doping concentration of gate region. So, SIThys have suitable carrier profile that is high near the cathode and low near the anode, in the ON state and better trade-off relationship than GTOs do. SIThy can realize a PIN diode like carrier distribution profile in the ON state because of its high gate potential. Moreover, it is one of the most important ideas that SIThy is characterized by its high electron injection efficiency, which is shown as high carrier density near the cathode, but its efficiency is continuously changed from high value as the SIThy to the low value as the GTO.

V-2-7. Experimental result

Although these experimental results were much earlier than the above simulation consideration, the idea of this simulation procedure from the higher V_g and doping concentration point of view is originated in that experimental result itself. So it is worth to review these result, here again.

Fig. V-2-8. Top view of SIThy[53]

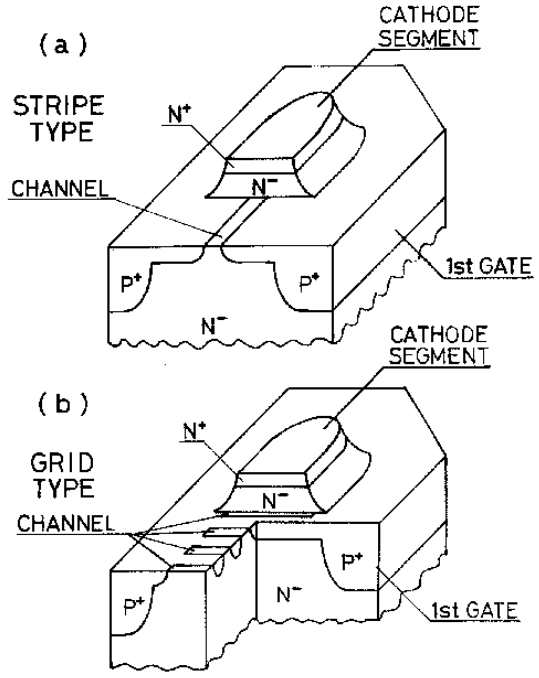
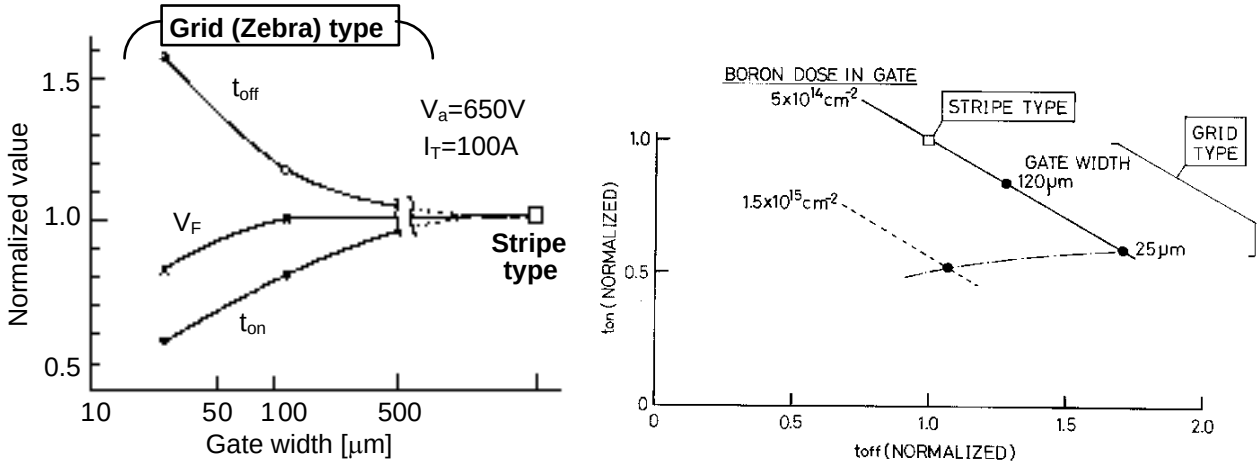


Fig. V-2-9. Schematic 3D gate structure of SIThy[53][54]

There are same tendency as the simulation result for the gate structures of 4500V class both single

gate and double gate SIThy, as shown in Fig. V-2-8, 9. The higher the gate concentration is, the better the V_F-t_f tradeoff is, as shown in Fig. V-2-10.

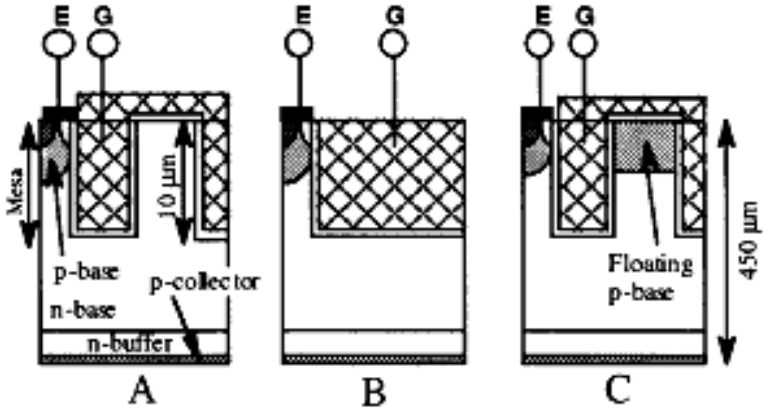


(a) gate structure dependence of V_F, t_{on} and t_{off} **(b)** t_{on} and t_{off}

Fig. V-2-10. SIThy gate structure and doping concentration dependence of t_{on} and t_{off}[53][54]

VI. Multiple trench gate approach to improve V_{on}-E_{off} of IGBT

Before the multiple trench structure, as the IEGT[55][56], is found out as the one of the best solution for the V_{on}-E_{off} characteristics, the deeper or wider the trench IGBT is better device than the standard trench IGBT, as shown in Fig. VI-1-4. As discuss in the above section, the deep or wider trench IGBT structure has the lower V_{on} than shallower or narrower trench ones, but both type have the gate capacitance-increasing problem. Moreover, in the device fabrication process, the deeper trench is difficult to make and the wider trench is difficult to refill.



(A) Multiple trench gate without P (B) Wide trench gate (C) Multiple trench gate with floating P

Fig. VI-1. Variation of the trench gate to improve V_{on}-E_{off} characteristics for 4500V class IGBT[57]

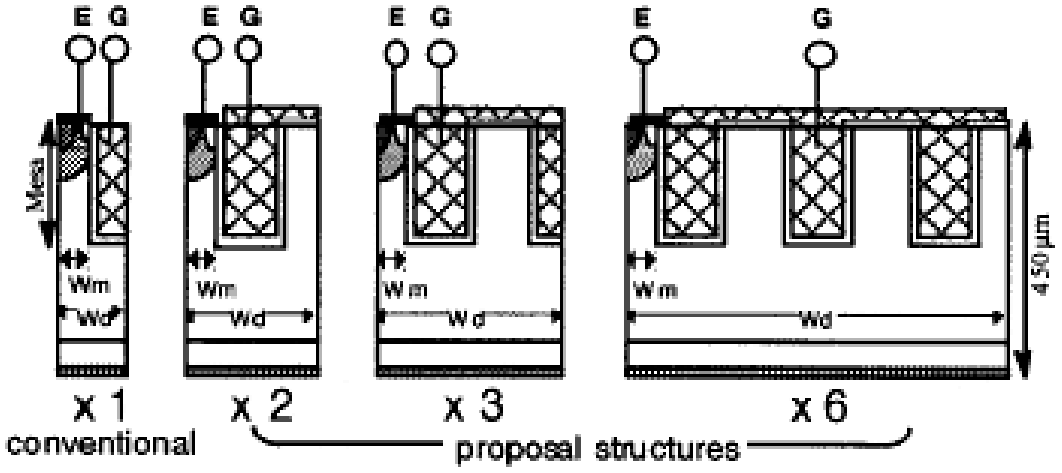
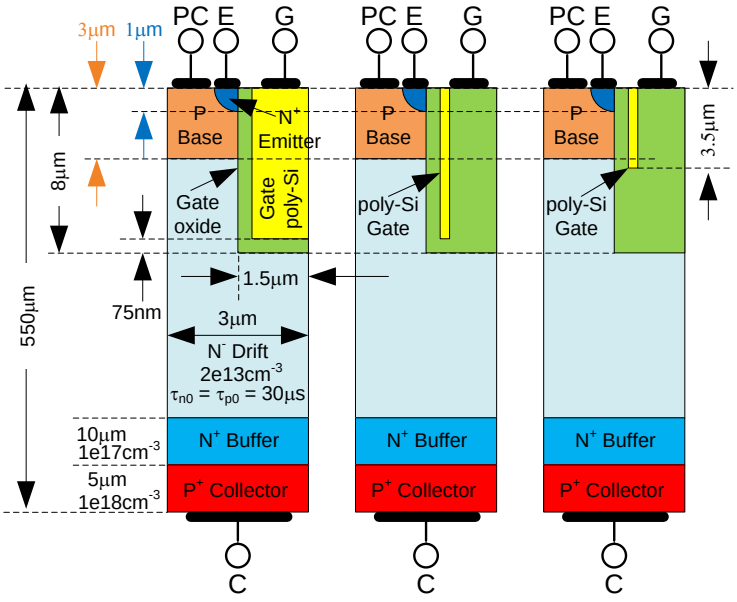


Fig. VI-2. Variation of the multiple trench gates for 4500V class IGBT[57]

Before discussing about "less p region" structure, partially formed trench gate structure, shown in Fig, VI-3, should be disclosed. It is not easy to realize this partially formed trench gate structure, but the simulation result certify there is no need to form gate electrode far beyond the inversion channel region to extend accumulation channel region below p base region to bottom of the trench, because V_{on} difference between standard trench gate which have the fully formed doped poly silicon films inside the trench and partially formed trench gate which has just short poly silicon gate films is very slight. So that, the extended accumulation channel area is not always necessary to push up the electron injection efficiency, and deep or wide trench without inside

poly silicon gate may predict another important possibility to understand how to increase the N-emitter injection efficiency, that is the geometrical cross-sectional structure around p-base and trench gate.



(a) conventional (b) partial gate (c) partial gate
along a trench sidewall only for N-channel region

Fig. VI-3. Partially formed trench gate structures for 4500V class IGBT[37]

The idea of the "less P region" isolated by trench near the cathode is the second hypothesis to increase the N-emitter injection efficiency. To enforce the conductivity modulation in N-base, it is necessary to increase the hole density in N-base, especially near the N-emitter. In the following parts of this section, to use the examples of high voltage trench IGBT and related structures, the second hypothesis would be confirmed by both experimental results and simulation results.

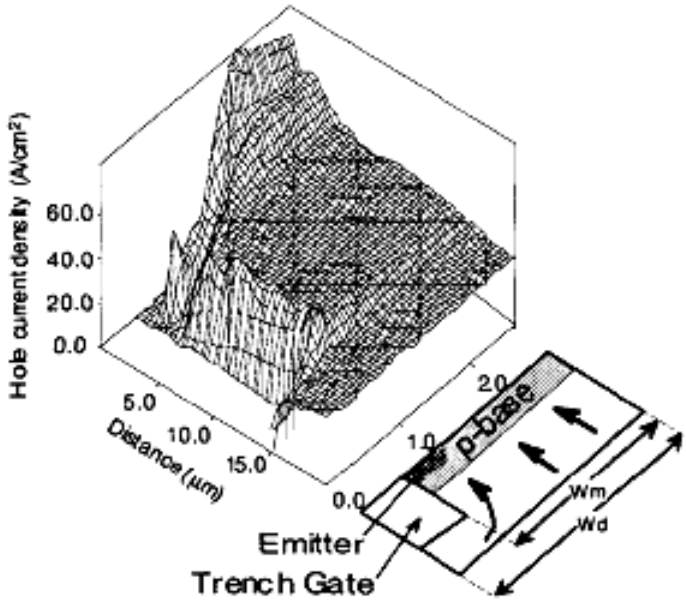


Fig. VI-4. The hole current density (J_h) near the mesa region in the conventional trench IGBT[57]

Fig. VI-4 shows the simulated distribution of hole current density (J_h) near the mesa region in the conventional trench IGBT. In the mesa region, J_h increases in inverse proportion (W_d/W_m) to narrowing of the N-base in the ration of W_m/W_d, where Wd is the half-cell width of IGBT and Wm is the half width of the active mesa region which has P-base. We also find that the hole diffusion current ratio to the hole current is almost constant and about 40%, not 100%; moreover the holes linearly pile up from p-base junction to the mesa edge. So the increase of J_h in the mesa region induces high hole density just below the mesa region. This high hole density underneath the mesa region pulls up the hole density in the entire n-base. Fig. VI-5 is the simulated hole density in the mesa region for the various W_d/W_m (1.2 – 4.0) ratio structures. The larger the W_d/W_m, the higher the hole density is at the mesa edge. It is also seen that this W_d/W_m effect of coarse pitch is smaller than that of fine pitch.

It is clear that narrowing the active mesa width makes the conductivity modulation more effective and lower the forward voltage drop in the N-base of IGBT.

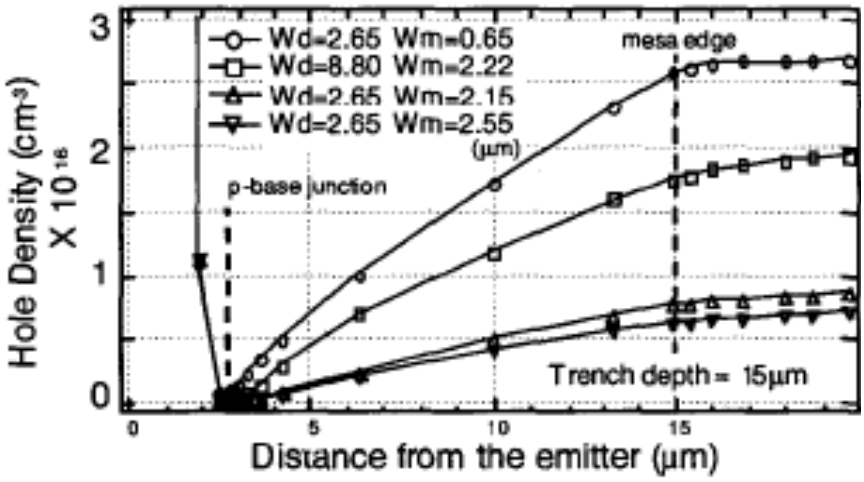


Fig. VI-5. The simulated hole density in the mesa region for the various W_d/W_m (1.2 – 4.0) ratio structures[57]

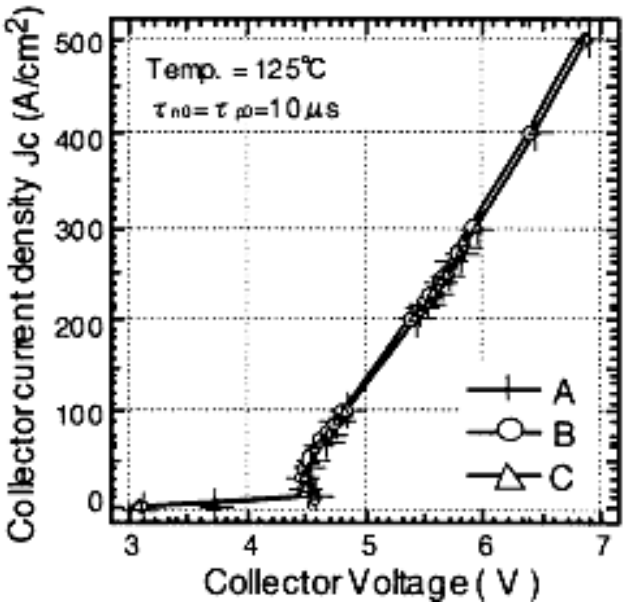


Fig. VI-6. The simulated V_c-I_c (J_c) characteristics for the structures A, B and C of Fig. VI-1[57]

To improve the forward voltage drop by using the above concepts, we proposed structure A (multiple trench structure) from candidate illustrated in Fig. VI-2. In structure A, the region of the emitter and the P-base are reduced by introducing N-type spacers between trenches to increase Wd/Wm without changing the trench shape. In structure B, the trench width is widened for the same purpose. Structure C is similar to A, but it has floating p-bases. By numerical simulation, these three structures have almost same *Vc-Ic* (*Jc*) characteristics (Fig. VI-6). But, described before, taking account the fabricating wafer process steps, the structure B has a large disadvantage of refilling the wide trench.

There are the variations of structure A shown in Fig. VI-2. The singlet (X 1) is the conventional structure for the reference. The doublet (X 2), the triplet (X 3) and the sextuplet (X 6) have one p-base every 2, 3 and 6 trenches, respectively.

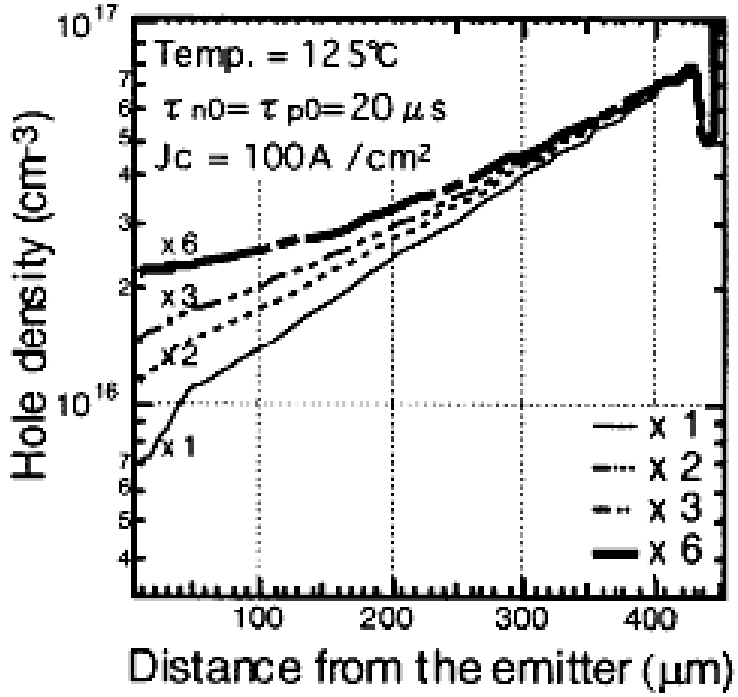


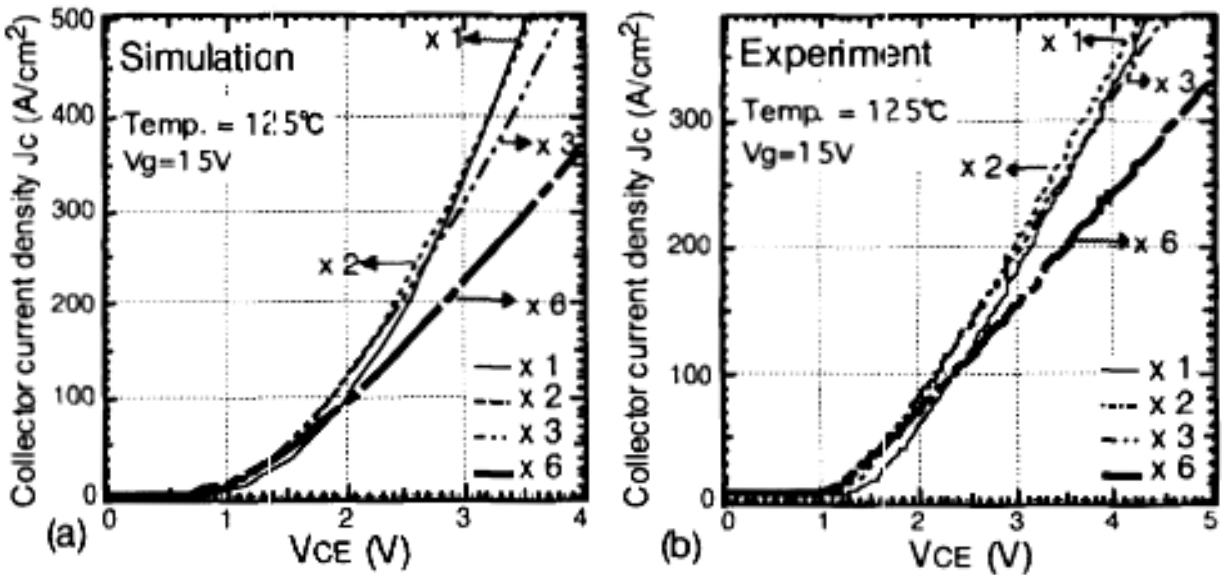
Fig. VI-7. The simulated hole densities of the multiple trench IGBTs in their ON state[57]

The characteristics of the multiple trench IGBTs were investigated by numerical simulation and experimentally confirmed. Here are the Conditions set forth on the simulations and the fabricated devices.

Two-dimensional simulations were done using MEDICI with analytical mobility model, band gap narrowing, Auger recombination, Fermi-Dirac statistics and Shockley Reed Hall (SRH) lifetime model. The trench depth, the trench pitch and the trench width were 10μm, 5.3μm and 1.0μm respectively, and the thickness of the N-base was 450μm (for 4500V forward blocking voltage), and the gate oxide thickness tox was varied from 50nm to 150nm. We used the carrier life time at high level injection τ_{HL} (= τ_{n0} + τ_{p0}) 40μs that was extracted by the TEG (Test Engineering Group) pattern[58], so the ambipolar diffusion length La was 235μm, which was much larger than the sextuplet cell pitch (31.8μm), the longest of all the designs.

Multiple trench IGBTs whose active area was 2.5mm^2 were fabricated. All the device parameters were the same as the ones in the simulation.

The forward V_c-I_c characteristics are discussed in a detail in this part. The simulated hole densities of the multiple trench IGBTs in their ON state are shown in Fig. VI-7. As described in the concepts part of this section, the hole densities of the multiple trench IGBTs are higher than that of the conventional singlet one (X 1), especially near the N-emitter (cathode) side, and the sextuplet achieves the highest hole density of all the investigated device structures.



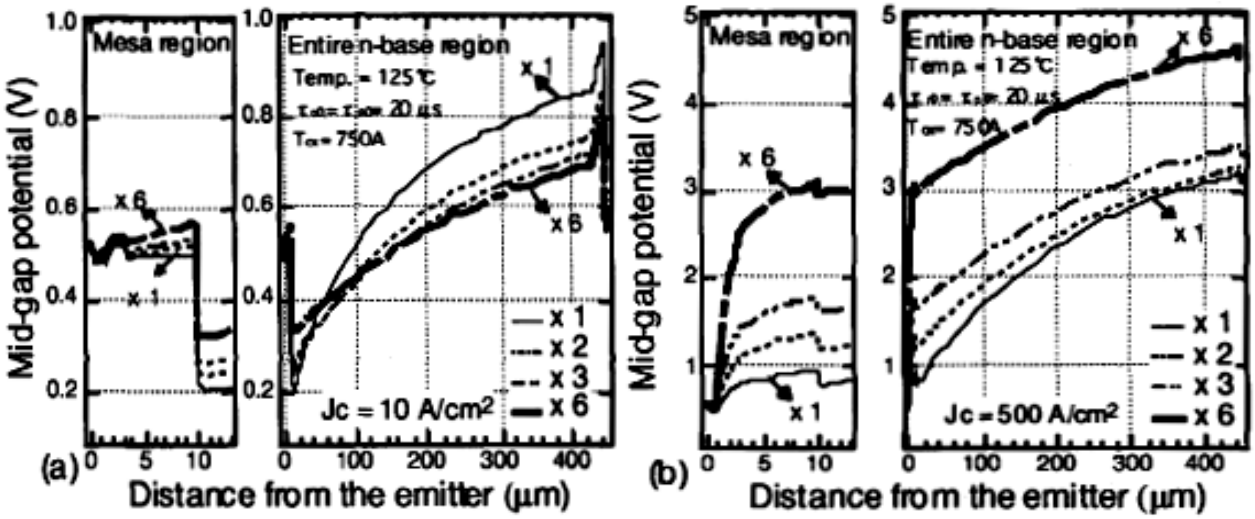
(a) Simulation **(b) Experiment**

Fig. VI-8. The simulated and measured V_c-I_c (J_c) characteristics[57]

Both simulated and measured V_c-I_c (J_c) characteristics of Fig. VI-8 (a) and (b) show that the structure achieved the highest hole density, the sextuplet, does not always exhibit the lowest forward voltage drop over the whole current density range. The sextuplet obtains the lowest forward voltage drop at low current density (<50A/cm^2). But, as the current density increases, structures which have fewer multiple trenches (X 2 or X 3) show the lowest forward voltage drop. Moreover, the conventional singlet structure (X 1) indicates the lowest forward voltage drop at more than 400A/cm^2.

The analysis would be done as following; The multiple trench IGBTs achieves a higher hole density in the n-base than the singlet does, but they have less MOS channel density because of reduction of the emitter. So the multiple trench IGBTs need better MOSFFET performance to improve the forward voltage drop at very high current density.

Fig. VI-9 shows the mid-gap potential along the trench sidewall (MOSFET region) and in the entire n-base. At the low current density of 10A/cm^2 in Fig. VI-9 (a), the potential drops in the MOSFET region for all structures are small, so that the total potential drop is dominated by the conductivity modulation in the N-base, and the sextuplet has the lowest forward voltage drop. However, at the high current density of 500A/cm^2 in Fig. VI-9 (b), because of less channel density, the sextuplet's potential drop in the MOSFET region becomes much higher than the other structures, even though the potential drop in the entire n-base keeps the minimum value.



(a) 10A/cm^2 **(b)** 500A/cm^2

Fig. VI-9. The mid-gap potential along the trench sidewall (MOSFET region) and in the entire N-base[57]

The multiple trench IGBTS improve the potential drop in the n-base, but have a large potential drop at MOSFET region. So, to improve an overall potential drop in the forward conduction state, it is necessary to consider the rating current density and various MOSFET parameters.

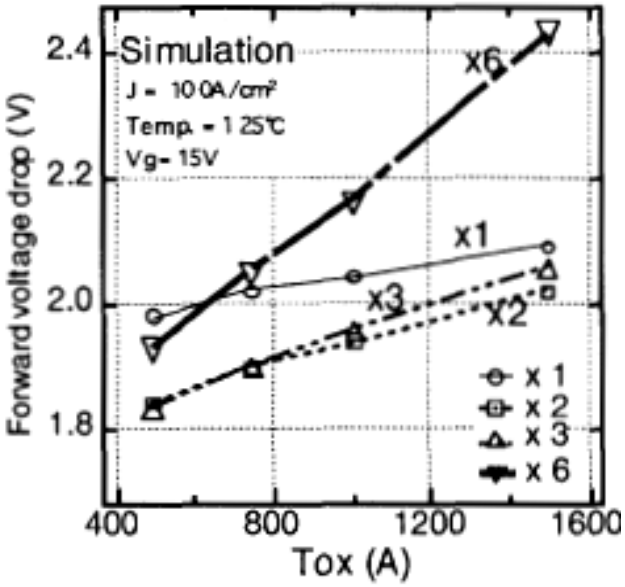
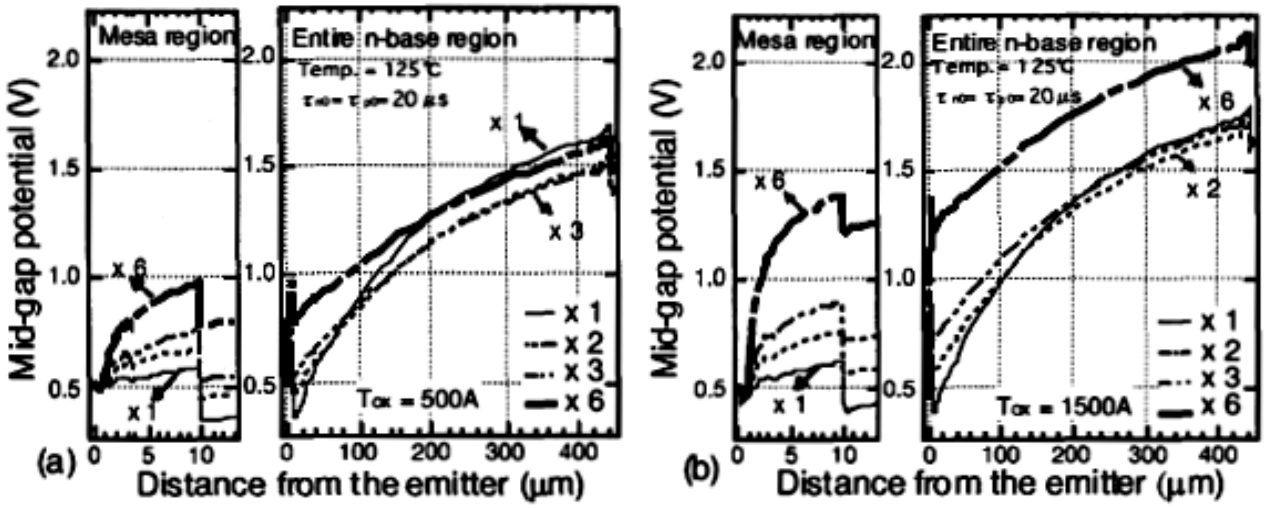


Fig. VI-10. The V_{on} at 100A/cm^2 of T-IGBTs with gate oxide thickness t_{ox} between 50nm and 150nm[57]

To analyze the effect of the MOSFET performance for the multiple trench structures, the gate-oxide thickness dependencies of the V_c-I_c characteristics are examined. Fig. VI-10 shows the forward voltage drops at 100 A/cm^2 of the multiple trench IGBTs with gate oxide thickness t_{ox} between 50nm and 150nm. Fig. VI-11 (a) and (b) show the mid-gap potential at J_c = 100A/cm^2 with t_{ox} = 50nm and 150nm. The multiple trench IGBTs of t_{ox} = 150nm, especially for the sextuplet, cannot keep low forward voltage drop because of the high potential drop in the MOSFET region. On the other hand, the multiple trench IGBTs of t_{ox} = 50nm effectively improved

the total voltage drop because they keep the potential drop low in the MOSFET region.



(a) tox = 50nm (b) tox = 150nm

Fig. VI-11. The mid-gap potential along the trench sidewall (MOSFET region) and in the entire N-base at 100A/cm^2 of the multiple trench IGBTs with gate oxide thickness t_{ox} between 50nm and 150nm[57]

Finally, Fig. VI-12 is an experimental "territorial-map" of the multiple trench structure which achieves the lowest forward voltage drop for a certain current density (y-axis) and a gate oxide thickness (x-axis). The multiple trench structure is more effective in the area of thin gate oxide thickness and low current density, because, in this area, the potential drop in the MOSFET region is so low that the total potential drop is dominated by the N-base. At a rating current density 100A/cm^2 and for a gate oxide thickness of 75nm, the triplet achieves the lowest forward voltage drop, and makes an improvement of about 10% over the conventional structure (X 1).

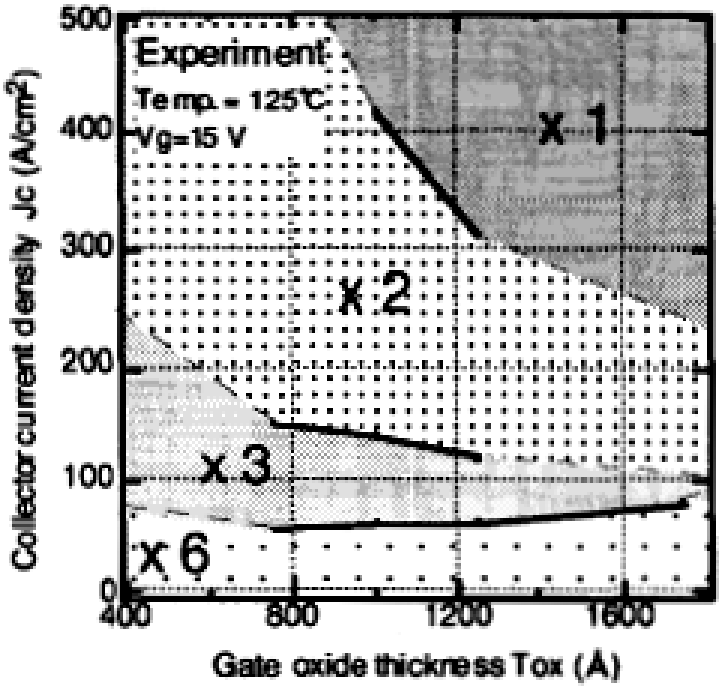


Fig. VI-12. The experimental "territorial-map" of the multiple trench structure[57]

In conclusion of this part, from both simulation and the experimental result of the multiple trench IGBTs, minimizing the p-base region, which corresponds to narrowing the active mesa width, led to lowering the V_{on} of T-IGBT. It was also clear that the V_{on} of T-IGBT was determined by the balance of the conductivity modulation in the N-base and the performance of MOSFETs, and by minimizing the P-base region the former had advantage while the latter fell off.

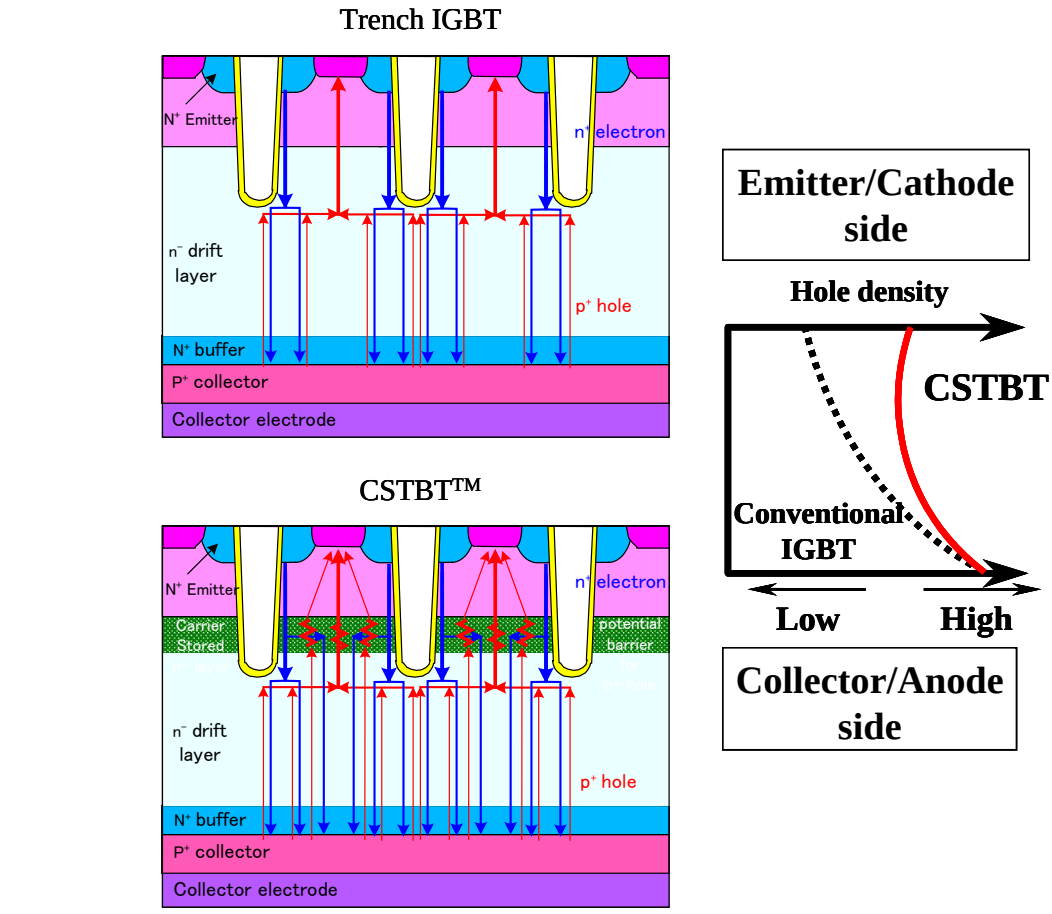
For the 4500 V trench IGBT, the triplet type is the balanced optimum structure at 100A/cm^2 of the rated current density in the realistic gate oxide range, and its forward voltage drop is improved by 10% over the conventional structure.

In other words, in the lower voltage class or in the higher J_c region, the conventional (X 1) T-IGBT structure is superior from the V_{on} point of view, in the higher voltage class or in the lower J_c region, the wide cell pitch (X N) structure is superior.

VII. Design of IGBT to improve SOA - V_{on} - E_{off} tradeoff

VII-1. Front side electron injection enhancement : CSTBT™

CSTBT[10][11] stands for "Carrier Stored Trench gated Bipolar Transistor" and is named as the advanced structure of T-IGBT. It has the relatively highly doped extra-N-type layer, which is so called CS (Carrier Stored) layer, laid underneath the P-body region of MOSFET part of T-IGBT, as illustrated in Fig. VII-1. CSTBT™ has three characteristics in its operation mechanisms in the ON state. Thanks to this CS-layer, CSTBT™ reduces the JFET effect, which exists on a PN junction between P-body and N-drift even in T-IGBT structure, and obtains the higher electron injection enhancement as illustrated in Fig. VII-1 (b). This higher electron carrier density also induces a highly stacked hole density at a position very close to the bottom end of the N-channel region. It seems as if the high density hole carriers are stored in the CS-layer. This is the origin of the name of CSTBT™. Fig. VII-1 (c) shows both CSTBT™'s and T-IGBT's carrier (hole) profiles, in which both electrons and holes are identical as far as the conductivity modulation occurring for maintaining the charge neutrality. CSTBT™ has the higher carrier density near the N-emitter, so CSTBT™ has the better V_{on}-E_{off} tradeoff than the conventional T-IGBT.



(a) top : Trench gated IGBT (T-IGBT)
(b) bottom : CSTBT™
(c) carrier density along the trench sidewall in the ON state for CSTBT and T-IGBT

Fig. VII-1. Structures, operational mechanisms and carrier densities of CSTBT™ and T-IGBT[6]

VII-2. To regulate electron injection : Wide cell pitch CSTBT™

Figure VII-2 shows the improvement process for IGBT characteristics among the triangular tradeoff relationship. In figure VII-2, the upper row shows the semi-equivalent circuit mode for the ON state only. Actually, those are not accurate from the circuit models, but it might be easy to grasp how to reduce V_{on} by changing the parts of device. The second upper row shows the forward output V_c-I_c characteristics. The third row shows triangular tradeoff where the thick arrow indicates parameter of major improvement. The lowest row shows the schematic cross-sectional view of the device cell structures, i.e. the planar gate IGBT, the trench gate IGBT, CSTBT™ and wide cell pitch type CSTBT™, respectively.

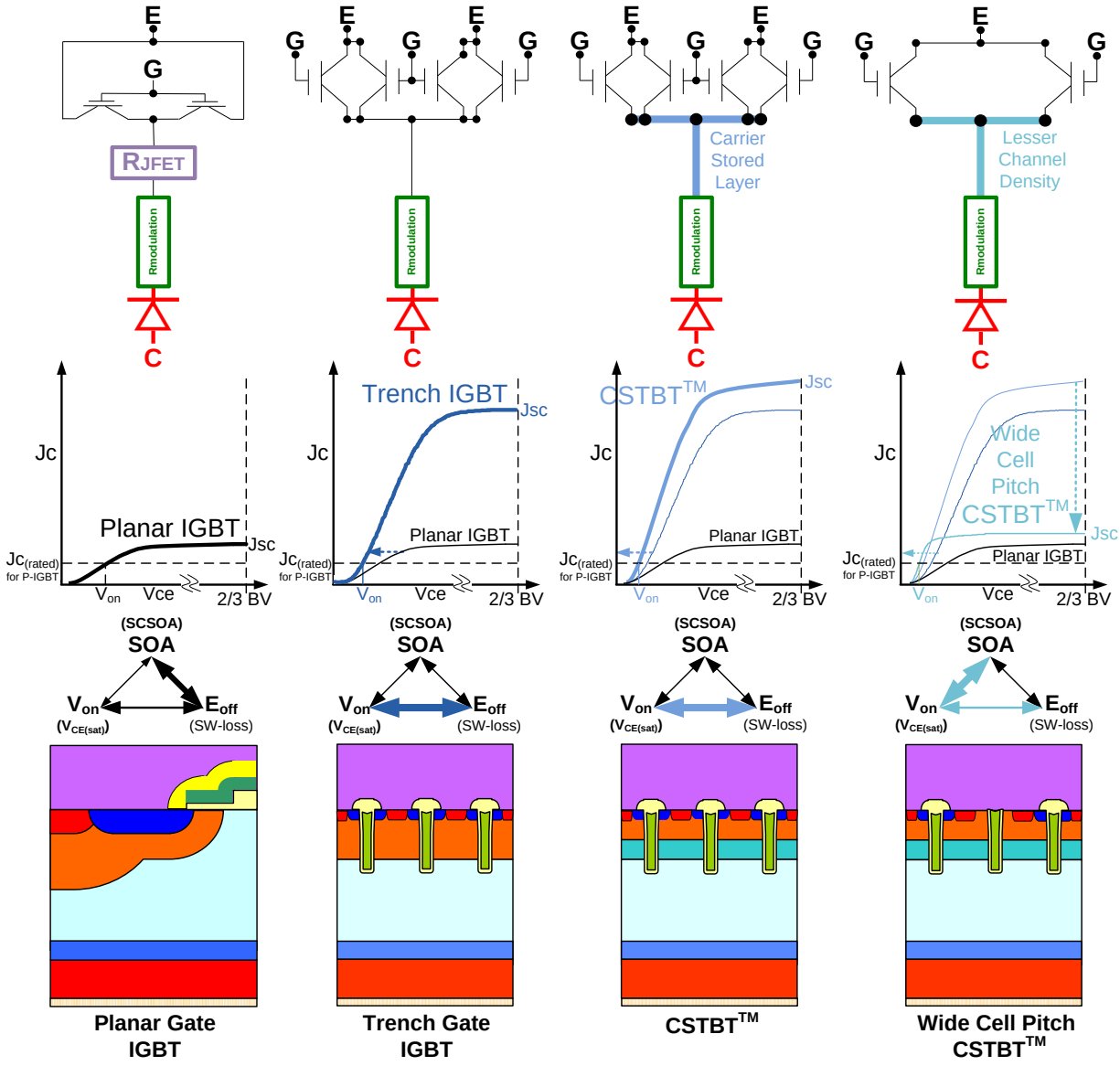


Fig. VII-2. The forward output V_c-J_c characteristics up to the highest current density J_{sc} corresponding to the short-circuit operation mode, the improved tradeoff relationship among the triangular tradeoff and their IGBT structures of the medium voltage class of 1200V is assumed[(1)(3)]

In the figures, $J_{c(rated)}$ is fixed at the Planar IGBT's value, but it has increased almost twice and more in the Trench IGBT and CSTBT™ from the total balance point of view.

Figure VII-2 presents one of the ways to improve the triangular tradeoff relationship. A planar gate type of the 3rd generation IGBT employed the well balanced characteristic whose saturation current (I_{sat}) was low as to maintain a sufficiently large SCSOA. But its V_{on} was not so low because of its widely arranged MOS gate cell structure. The next generation fine patterned "sub-micron" planar IGBT[7], shown in Fig. I-7 right bottom, remarkably improved its V_{on} by both increasing its cell density and reducing the JFET effect. The T-IGBT has the much lower V_{on} to improve the fundamental tradeoff between V_{on} and E_{off}, because of both its higher cell density and being free from JFET effect. But this historical T-IGBT's large I_{sat} (J_{sat}) (saturation current) in the ON state requires a protection circuit to compensate the small SCSOA. This J_{sc} is shown in Fig. VII-2 as the cross-point across the two thirds (2/3) of BV line, how large an I_{sat} (J_{sat}) corresponding the SCSOA is in FBSOA boundary.

To overcome the above dilemma of a low V_{on} characteristic maintaining a low I_{sat} characteristic consistently, the latter two structures of a standard CSTBT™ and a wide cell pitch type CSTBT™ were applied at almost the same time in case of 1200V[11][14]. Previously, the standard CSTBT™ structure of 600V class[10] achieves a lower V_{on} than the trench gate IGBT, as explain in the section VII-1, and the standard CSTBT™ is suitable for IPM application. Then the wide cell pitch CSTBT™ structure with dummy trench gates, which are inactive and directly connected to the emitter electrode, reduces the I_{sat} so low as to maintain its SCSOA wide enough[15]. This wide cell pitch CSTBT™ structure is applied to CM, a stand-alone IGBT module.

VII-3. To regulate backside hole injection : LPT

After the discussion about V_{on}-$I_{sat(SCSOA)}$, returning back to the RBSOA again in Fig. VII-3, which is merged figure of Fig VII-2's V_{on} part and Fig. III-9, the same kind of simulations was done for both FBSOA and RBSOA up to high current density simultaneously, as shown in Fig VII-4. There is no negative resistance region in the *BV* curve around $J_{c(rated)}$ of 100A/cm^2 for the 4500V T-IGBT with the optimized backside structure as shown in Fig. VII-4. Actually $J_{c(rated)}$ of this HV class is almost a half of 100A/cm^2, but, for the continence, $J_{c(rated)}$ is assumed to be still 100A/cm^2.

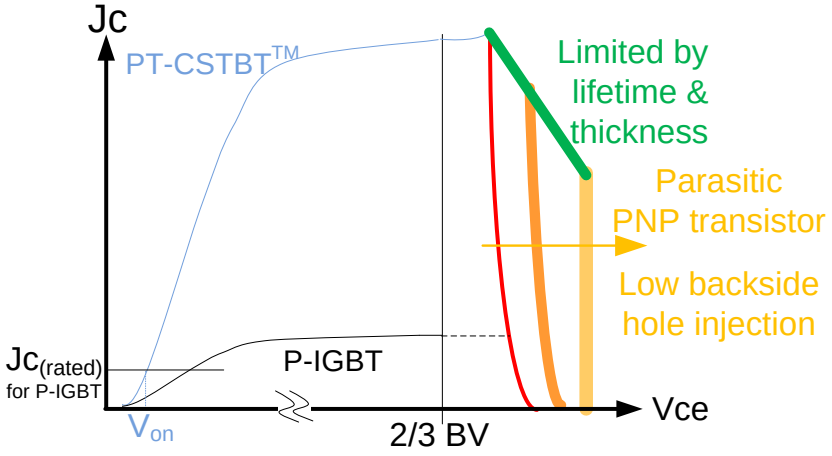


Fig. VII-3. The Schematic illustration for the improvement direction of RBSOA in the V_c-I_c (J_c) plane
The low to medium voltage classes of 600 to 1700V including 1200V are assumed.
The two thirds (2/3) of BV line indicates how large an I_{sat} (J_{sat}) corresponding the SCSOA is in FBSOA boundary as shown in the same manner of Fig. VII-2.

Another secondary breakdown region appears in the extremely high current density region of around 1000A/cm^2. But, it is quite natural to show the PNP transistor action for IGBT, this region is characterized by the N-drift thickness and carrier lifetimes. The most important point of Fig. VII-4 is that V_{on} curve of FBSOA limit and *BV* curve of RBSOA limit are jointed. So, SOA is literally closed as the area, which are figured by V_{on} curve and *BV* cure.

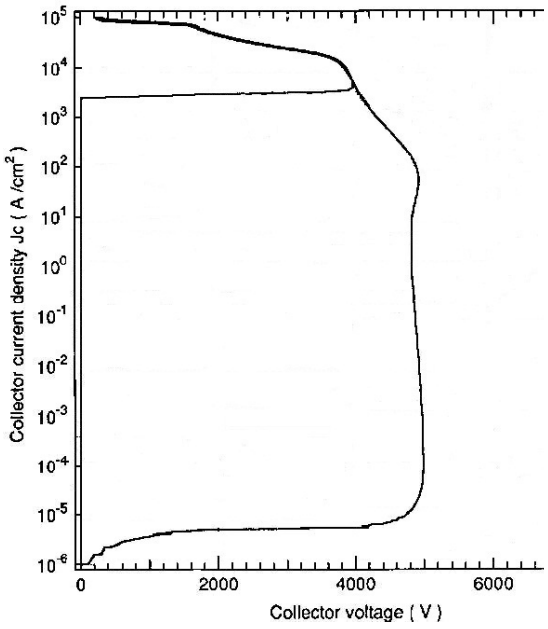


Fig. VII-4. Simulation result of 4500V T-IGBT with the optimized backside structure

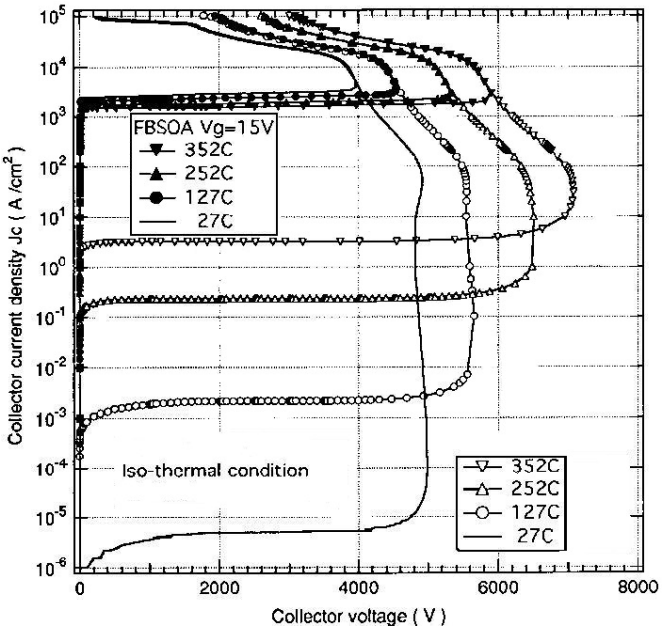


Fig. VII-5. Temperature dependence of Fig VII-4 FBSOA+RBSOA boundaries

As shown in Fig. VII-5, concept of "SOA = FBSOA + RBSOA" of Fig. VII-4 is expanded up to 352degC in the isothermal condition. It is clearly seen that all the couples of V_{on} curve and *BV* curve as the FBSOA and RBSOA met together to enclose a certain area. As th temperature increase, I_{sat} are slowly going down according to the channel mobility increase, and the diffusion current as the leakage current of *BV* curve rapidly increase, but *BV* value itself also increase as the reduction of the ratio of impact ionization. Of course, it would be impossible to maintain the leakage current level of A/cm^2 at 352degC in the real device cooling condition, but as the transient operational point of view, it is also quite natural that this hot condition could be simulated until the intrinsic carrier temperature, which is much higher than 352degC.

From this temperature dependence, it is clear that each temperature's SOA has a similar shape and does not have so special shape or drastic change at all until 352degC, maybe up to 650 or 800degC. This is very good sign to estimate SCSOA as the time integral of Isat in the very large V_{cc}. There is no necessity to take the degradation of FBSOA and RBSOA into account in case of SCSOA estimation, which is only defined as the thermo-dynamics problem as E_{sc}.

As the mentioned above, backside structures are strongly depending upon the device *BV* classes, and sometimes several improvements had been applied at the same time for the mass-production phase device. And, each device structure does not accurately correspond to the real mass-production devices.

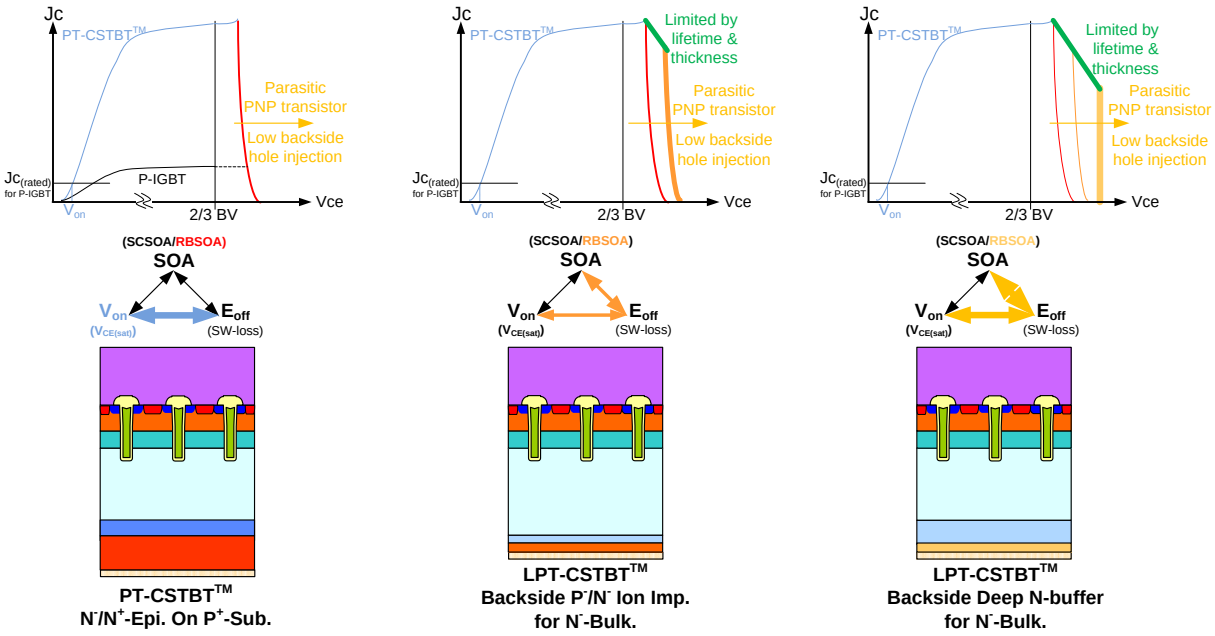


Fig. VII-6. IGBT's backside structure dependence of RBSOA's two dimensional shape in linear scale V_{on} curves as the FBSOA boundary, BV curves as the RBSOA boundary, the improved tradeoff relationship among the triangular tradeoff, and 1200V class IGBT is assumed(1)

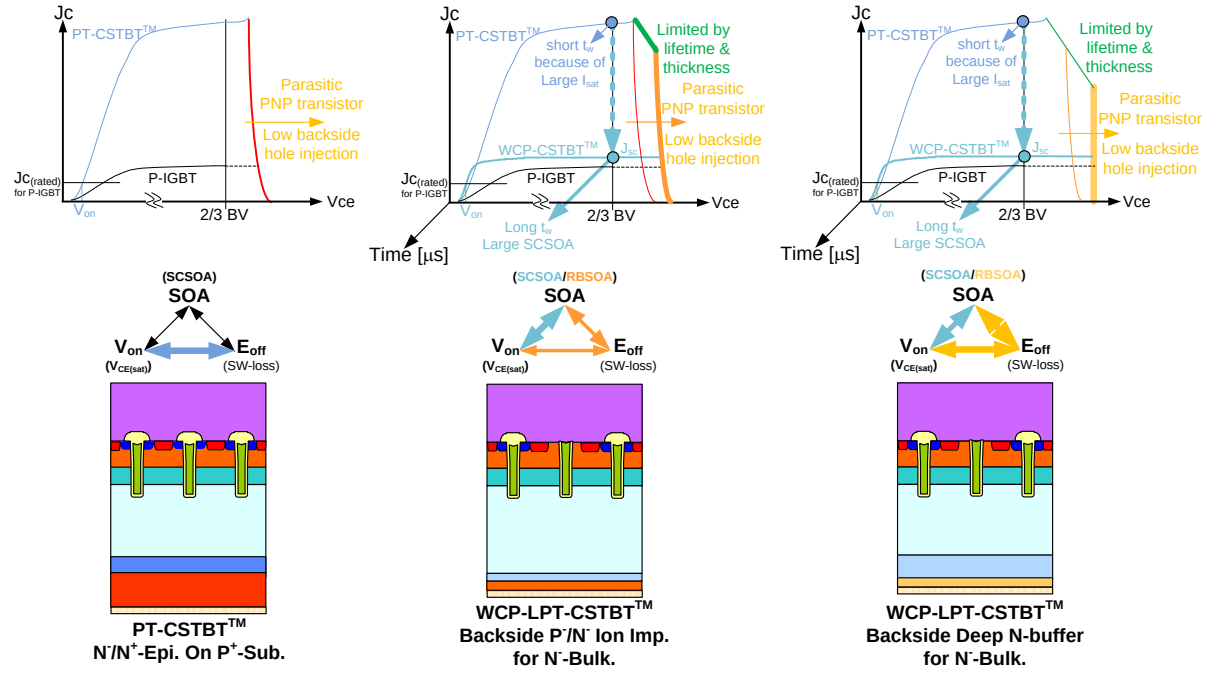


Fig. VII-7. IGBT's backside structure dependence of the schematic 3-dimensional illustration for SCSOA in linear scale

In addition to Fig. VII-6, t_w as the index of SCSOA is illustrated, and 1200V class IGBT is assumed(1)

In Fig. VII-6, MOS gate structure is fixed on the standard CSTBT™ , not the wide cell pitch one, to focus on the RBSOA shape, IGBT's P-collector side structure effects are described. PT-type has the highest hole injection efficiency. The LPT-type in the middle column has the relatively lower P-collector doping

concentration than the PT-type, but its N-buffer is shallower than the latest LPT type device. So the *BV* curves gradually shifted from the strong negative resistance one to the straight one without the negative resistance part.

In Fig. VII-7, combination effect between FBSOA and RBSOA for SCSOA are described. For the square shaped SOA point of view as described in chapter I, the Improvement of RBSOA indirectly affects to improve FBSOA even in the wide cell pitch case.

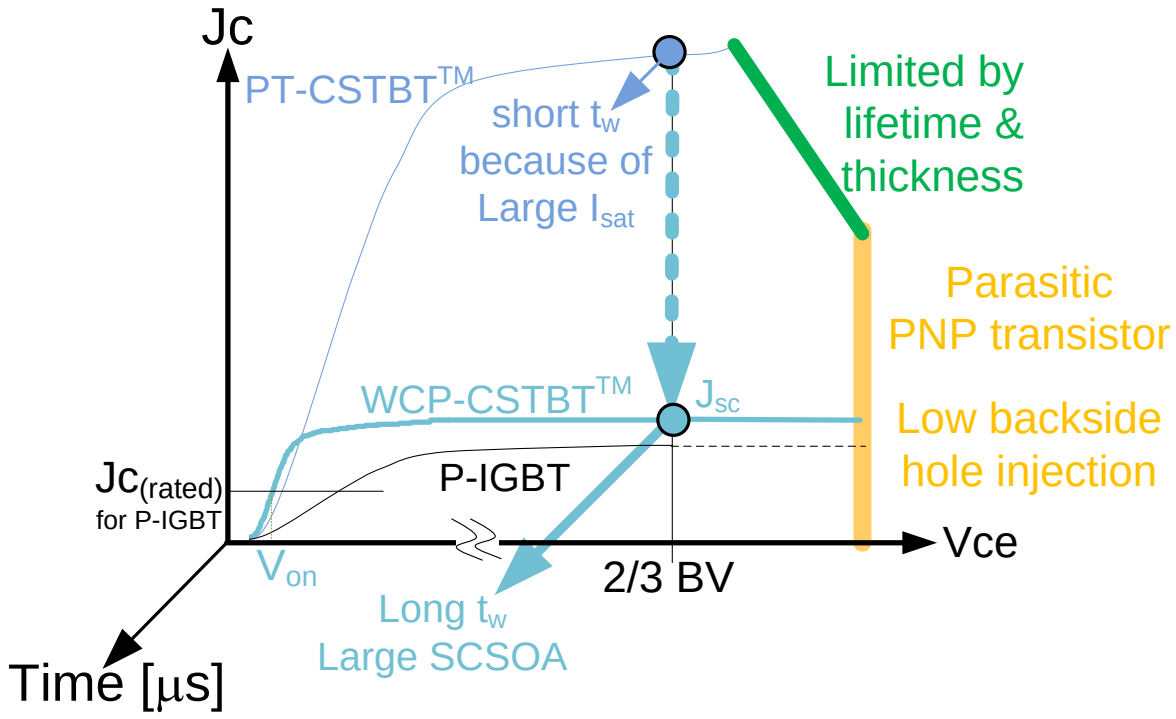


Fig. VII-8. Summary of the schematic 3-dimensional illustration for SCSOA in the 2-dimesional SOA=FBSOA+RBSOA plane

In conclusion, the design concept for the N-channel IGBT type device would be the followings.

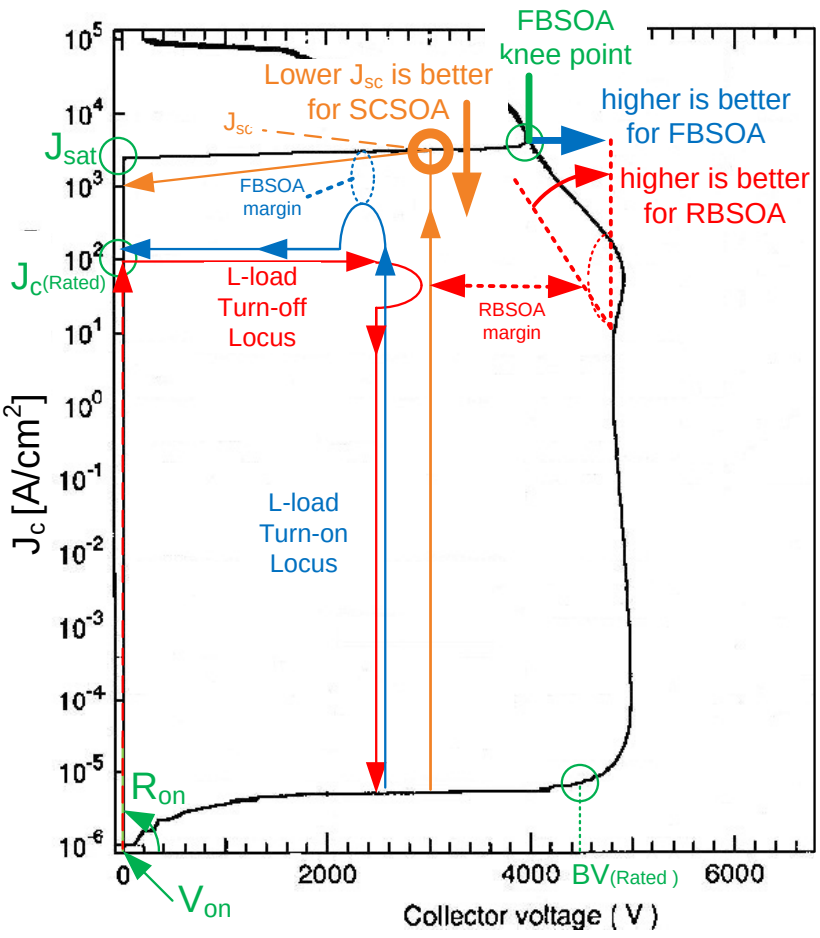
(1) To improve V_{on}-E_{off} : To increase the electron injection efficiency of the emitter (gate) side

(2) To improve RBSOA : To decrease the hole injection efficiency of the collector (without gate) side

(3) To improve FBSOA and SCSOA : To reduce and limit the saturation current

For example 1200V class device, the LPT type low hole injection structure is suitable for the RBSOA improvement, and the wide cell pitch CSTBT™ (T-IGBT) structure is one of the best solutions for the V_{on}-SCSOA tradeoff.

These concepts are schematically illustrated in the Fig. VII-9.



$E_{on} = \int V_{CE} \times I_c(rated)\, dt$
$E_{off} = \int V_{CE} \times I_c(rated)\, dt$
$E_{sc} = \int V_{CC} \times I_{sc}\, dt$

THe standard VCE of switching test is a 1/2 of the rated BV, and the Vcc of SC (Short Circuit) mode test is 2/3 of the rated BV, respectively.

RBSOA is limited by the secondary breakdown of the parasitic PNP-transistor in anti-parallel. The lower PNP gain of the parasitic transistor is favorable to enhance the RBSOA.

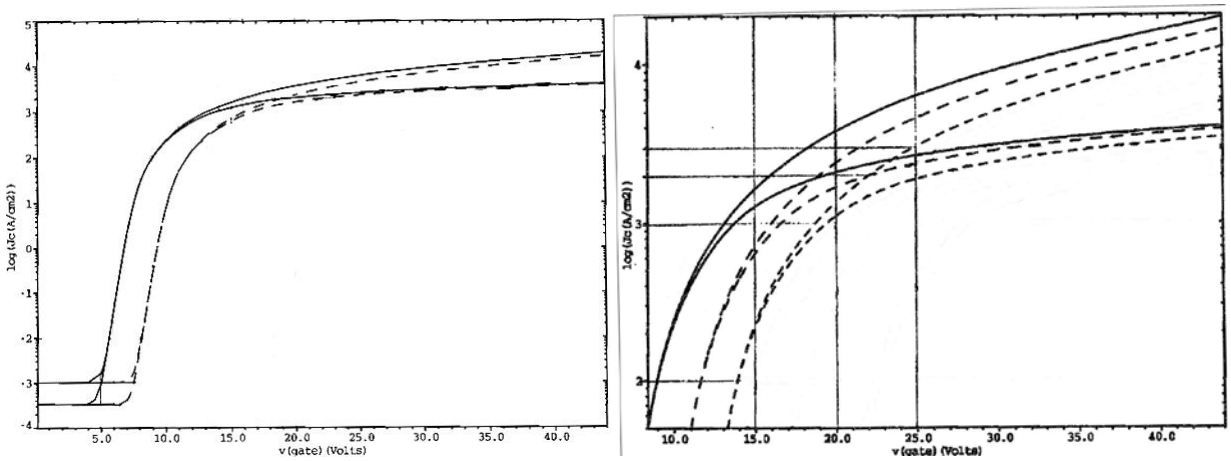
Although E_{sc} is limited by the device thickness from the thermodynamics, the SCSOA index t_w would be improved by lowering J_{sat}.

Fig. VII-9. Totally balanced solution of the operational area (SOA) as the FBSOA and RBSOA combination for the N-channel IGBT type device in V_c-I_c plane

VIII. Role of periphery on the device operation of SCSOA

Effects of stray (wire-bond) inductance Le and resistance Re for SCSOA

Sometimes, the experimental I_c (J_c) waveform during the SC mode switching seems to be quite different from the simulated waveform. Both large and smaller cases are observed comparing with the simulation result. There are two large reasons.



(a) full Ic range scale for std. and low V_{th} cases (b) high Ic range scale for low, std. and high V_{th} cases

Fig. VIII-1. V_g-I_c transconductance (static) characteristics for V_c=10V and 3000V

The first reason of that difference is IGBT's V_g-I_c transconductance characteristics. In case of MOSFET as the traditional unipolar device, Id (Ic) is easily saturated in the high V_g region. But IGBT's I_c is never saturated even in the high V_g region, as shown in Fig. VIII-1 (a) and (b). The lower 2 curves in (a) and lower 3 curves in (b) are the characteristics of V_c = 10V. Even in the condition of V_c = 10V, I_c is gradually increasing. They have a saturation tendency but does not completely saturated at all. And the higher 3 curves in (b) are V_c = 3000V case, which V_c is same as the SC mode V_{cc} corresponding to the 2/3 of rated *BV* of device.

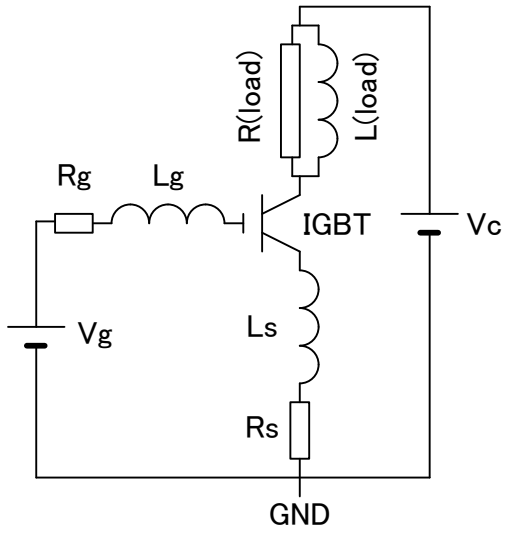


Fig. VIII-2. The equivalent circuit model

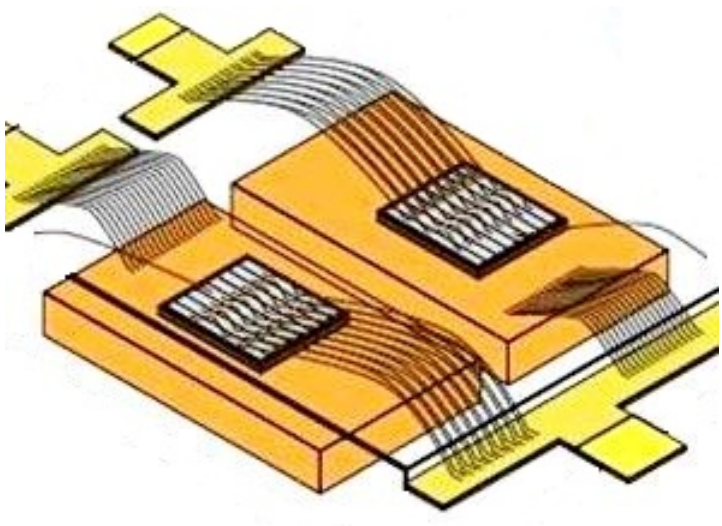
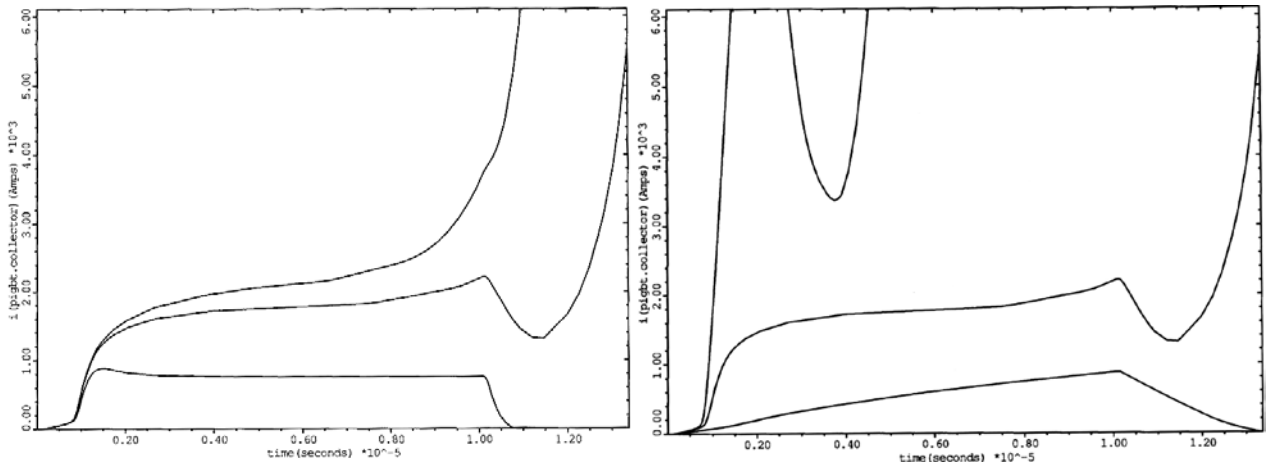


Fig. VIII-3. The schematic 3D view of wire bonding[59][60]



(a) Effects of the stray resistances (R_s) (b) Effects of the stray inductances (L_s)

Rs : 50nΩ (small), 500nΩ (standard), 5mΩ (large) Ls : 0.5nH (small), 6.25nH (standard), 50nH (large)

Fig. VIII-4. Effects of stray inductance and resistance for SC (load Shorted Circuit) mode switching

The second reason of that difference is coming from the stray inductance and resistance effect, which are mainly originated in a wire-bonding structure, as shown in Fig. VIII-3[59][60]. An equivalent circuit model for the stray resistances R_s and inductances L_s are described in Fig. VIII-2. On the every terminal of chip (E, C, G), R_s and L_s are supposed to be attached. The stray elements on the collector side might be negligible, because the electrical potential (V_c) is freely up and down. The stray inductance L_e and resistance R_e on the emitter side are carefully taken into account.

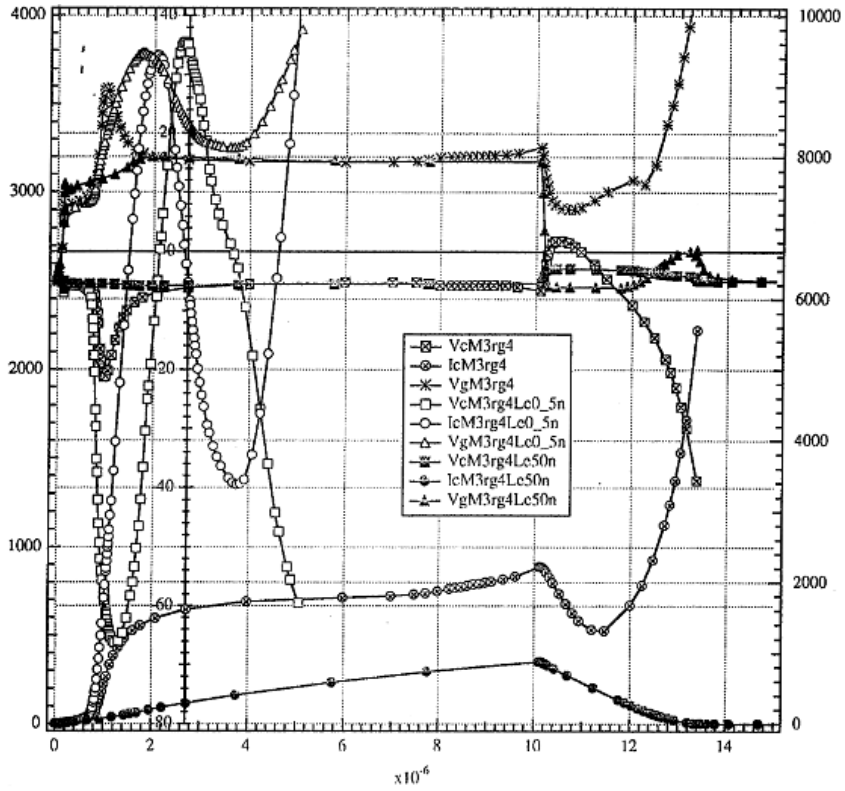


Fig. VIII-5. L_s effects on I_c for SC mode switching same as Fig. VIII-3 (b) with V_c & V_g as the vertical wire-bond inductances L_s : 0.5nH (small), 6.25nH (standard), 50nH (large)

The Re produces a large voltage drop between the IGBT chip's emitter and GND (Ground) to reduce the net V_g. The larger the R_e is, the lower the I_{sc} is, as shown in Fig. VIII-4 (a). The situation cause by L_e is more complex than Re case, as shown in Fig VIII-4 (b) and its detail of Fig. VIII-5.

As the same manner as the R_e case, the small L_e induces a negative emitter bias during the large dIc/dt time period in the initial stage of SC mode turn-on. This sequence correspond to the larger V_g drive for example V_g = 30V or more, as shown in Fig. VIII-5. Once V_g reaches the maximum value, it turns down to the ordinal V_g = 15V. But this V_g reduction also starts to regulate I_{sc}, and its sign of current flow is going to be negative. This negative differential value causes another change in V_g, and so on. In fact, too small L_e causes not only too large I_{sc} (I_{cp}) but also oscillation (ringing). On the other hands, the larger L_e directly reduces the collector current flow itself, as shown in Fig. VIII-4 (b) and VIII-5.

Only in the extremely large current case such as SC mode, these phenomena occur to be easily observed, and there are no critical situation can be observed in usual switching conditions.

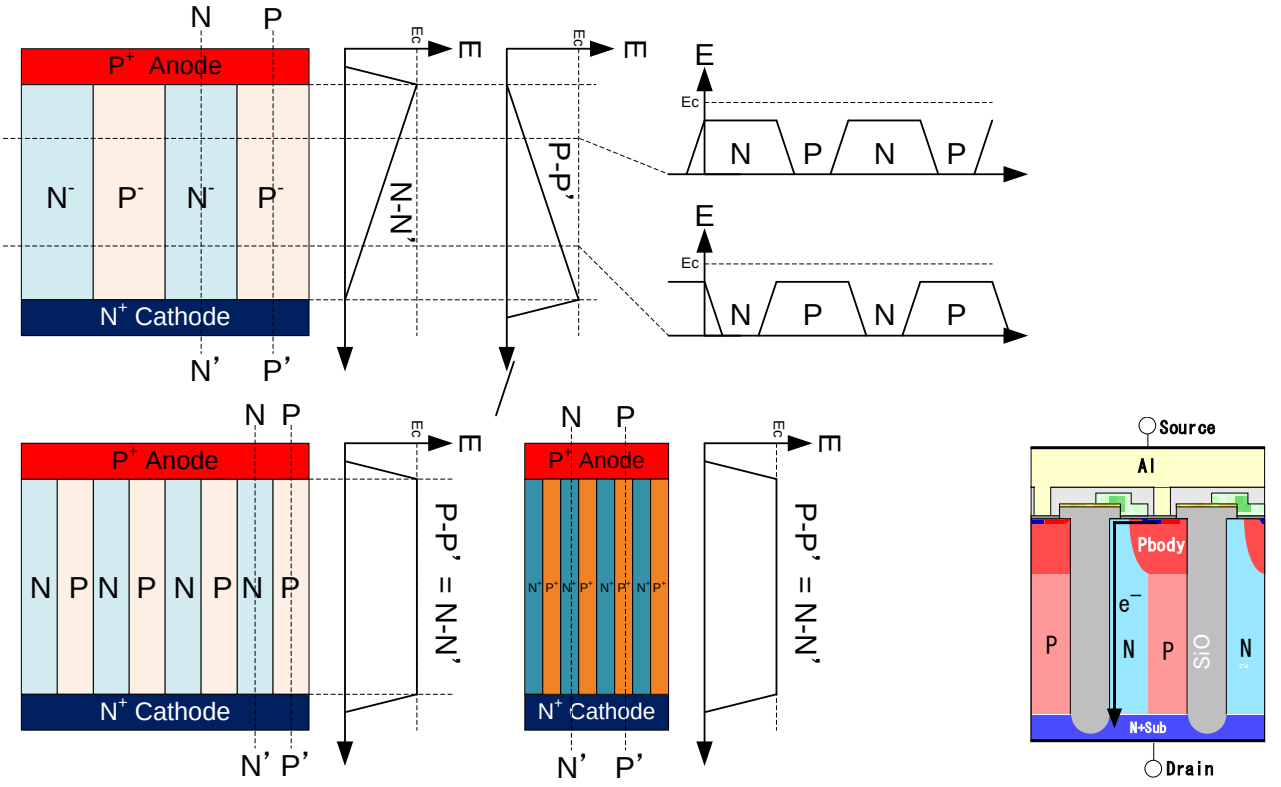
Not only from the above electrical characteristics point of view but also from the reliability point of view, the bonding between the chip surface and the electrode of the package should be tight and less electrically and thermally resistive. One of the effort to reduce those electrical R and L and thermal and mechanical resistance is improved by DLB (Direct Lead Bonding) method[59][60].

So, as the assembly structure and process, the bonding material and method between power semiconductor chip and package electrode are carefully chosen to be optimized the transient (dynamic) characteristics.

IX. To eliminate the built-in potential of a PN junction

IX-1. STM (Super Trench MOSFET) as the Super Junction (SJ) Device

SJ (Super Junction) device was originally invented as the charge compensation structure, in which N-drift region is partially replaced by P-drift region of equal charge as the summation, in the years of 1984[61], 1991[62], 1993[63], independently. All those ideas are only disclosed in the patents, and there is no technical paper in a publication.



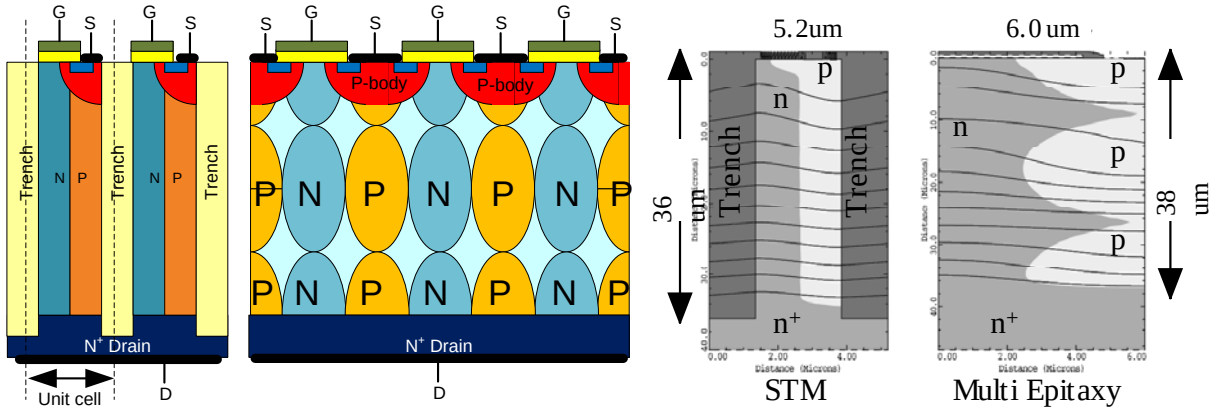
(a) Basic structure of SJ device (b) STM (Super Trench MOSFET)

Fig. IX-1-1. SJ device candidate[68][69]

Basically there is no regulation and limitation for 3-dimensional or 2-dimensional arrangement for the charge-compensating P-region in the N-drift region, so the simplification of the alternating "N & P columns" arrangement is allowed to explain its operation mechanism for the convenience, as shown in Fig. IX-1-1. Using the RESURF (REduced SURFace Field) effect in the multi-mode for all the interface not only between the vertical main PN junctions of P-body and N-drift near the top and of P-column and N^+-substrate near the bottom but also between N-column (N-drift) and P-column, both N-column and P-column are fully depleted when the applied voltage is low far from the *BV*. The electric field distribution of a triangular shape in the conventional PIN structure like a MOSFET or diode changes its shape to the rectangular shape in the N-drift region and the P-column region, as shown in Fig. IX-1-1 (a). Form this *BV* point of view, the factor of the first advantage is only twice. As the second advantage, the N-drift concentration would be increase until much higher than the conventional N-drift concentration explained in chapter II, as far as the horizontal thicknesses

and the repeating pitch are small enough to be fully depleted by the required *BV* value. So the doping concentration of N-drift region is going to be high theoretically up to the saturation concentration of the N-type dopant, i.e. practically up to the one or two order higher than the conventional concentration depending upon the *BV* class. So the $R_{on,sp}$ of SJ device is much lower than the Si limit value.

The practical effort based on the patent article[62] started in 1997[64] and intensely studied as the device simulation[64], and followed by the pilot product[66][67]. The name of SJ (Super Junction) is after the first technical paper[65] by the ISPSD (International Symposium on Power Semiconductor Devices and ICs) committee. The first attempt and most of the mass-production device on the year around 2000 are based upon the fabrication wafer process consist of the multi-epitaxial crystal growth. For the 600V class device, it takes about 7 layered epi-growth with additional twice times photo-lithography steps for each epi-layer, which means an extra 14 layers of photo-lithography in addition to the standard 7 or 8 mask step of the standard MOSFET fabrication process, that is, the total number of mask step is more than 21 layers.



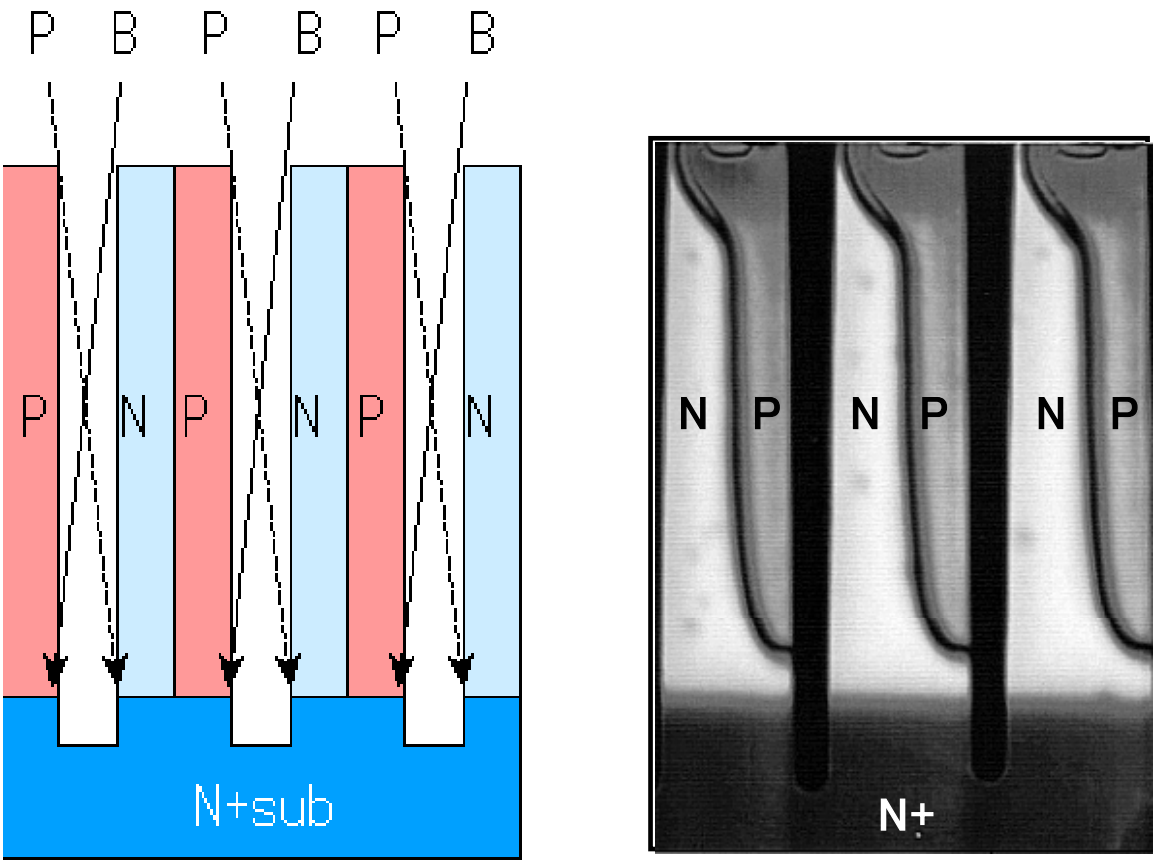
STM Multi Epitaxy

(a) Schematic cross-sectional view (b) Simulated potential distribution

Fig. IX-1-2. Advantages of 600V class STM comparing the multi-Epitaxial structure (conventional)[68]

Table. IX-1-1. Simulation parameters and results for STM and Multi-Epitaxial structure[68]

Device		STM		Multi-Epitaxy
BV [V]	250	600	1000	600
Cell pitch [μm]	5.2	5.2	7.2	12
Ron,sp [mΩcm^2] @100A/cm^2	4	13	36	32
Trench depth or Epitaxial thickness [μm]	17	36	64	47.5
	1			6 (x2 of Epi. Layer)
Wafer process	Easy for balanced doping Deep trench technology			Depending on epi. Technology
Cost estimation	Economical			Expensive



(a) Schematic view of ion implantation (b) SCM (Scanning Capacitance Microscope) image of doping

Fig. IX-1-3. Fabrication wafer process and results of 200V class STM structure[69]

To overcome this fabrication disadvantage, STM (Super Trench MOSFET) as the SJ device was suggested[68][69], as shown in Fig. IX-1-1 (b) and Fig. IX-1-2 (a). This device needs only one extra-mask step to make a trench and a trench sidewall ion implantation (Fig. IX-1-2). Although there is an extra oxide-filled trench column between N-drift and P-column, the pitch of N and P column is small enough by using highly tuned high aspect ratio trench. So the equi-potential contour distribution is more flat and uniform than the multi-epitaxy structure, which is modified for the small epi-step structure.

It was not in the mass-production phase, but its characteristics are evaluated much lower than the Si limit and about 30% of Si limit in 200V class device[6].

IX-2. To eliminate the built-in potential using SJ-RC-IGBT

Through the simulation, a concept for the next generation MOSFET or IGBT as a single chip solution by combining Super Junction MOSFET (SJ-MOSFET) with Reverse Conducting IGBT (RC-IGBT) is presented[70]. Since the MOSFET's fundamental trade-off relationship between $R_{on,sp}$ and turn-off loss E_{off} is much better than IGBT's, we focus how to push up a connection collector current density Jconnect where SJ MOSFET's forward output V_c-I_c curve touches the IGBT's one and found out the good combination for an N-drift and an N-buffer. This proposed device has an enough UIS (Unclamped Inductive Switching) capability as the SJ-MOSFET's SOA and acceptable dynamic characteristics as the IGBT or the FWD.

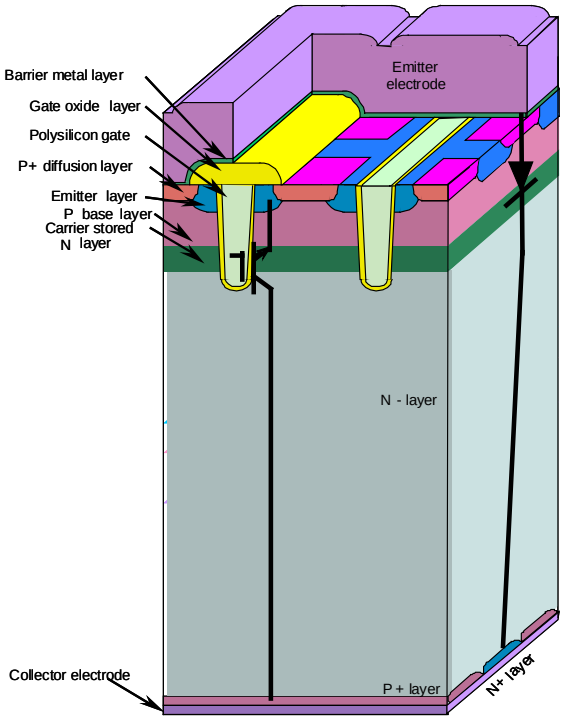


Fig. IX-2-1. RC-IGBT (Reverse Conducting IGBT)[71]

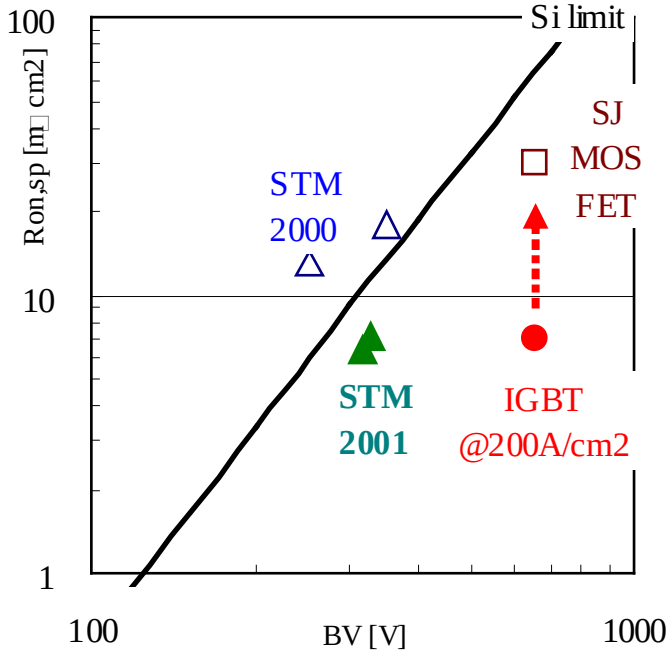


Fig. IX-2-2. Across the Si limit (BV-$R_{on,sp}$)[70] previous SJ device works[68][69][6] and IGBT

IX-2-1. Back ground

Both well known SJ-MOSFET[64][65][66][67] and our medium voltage class device named Super Trench MOSFET (STM)[69][70] with very tight cell pitch (Fig.IX-1-1 (b)) seems to be a little behind from IGBT in the high Jc region more than 200A/cm^2 (Fig. IX-2-2)[6], but IGBTs' $R_{on,sp}$ are worse in the low current density Jc region because of the built-in potential of a PN junction. Taking account UIS capability, SJ-MOSFET requires an N-buffer layer of the conventional low doping concentration under the N and P column structure above the high concentration N$^+$-drain region[72].

We found out how to establish the high current density point at which the SJ-MOSFET's forward output V_c-I_c curve could join the RC-IGBT's one while maintaining both a high saturation current characteristic as IGBT operation and a large SOA especially a UIS as MOSFET. And a body diode's recovery loss E_{rec} is also a large issue.

In the Fig. IX-2-2, $R_{on,sp}$ for both the well known SJ-MOSFET's and our STM2001[6], indicated as the square and triangle symbol respectively, are about 30% of the Si limit, but it is worse than IGBT's, as mentioned above in the high J_c. As long as simply operated as the bipolar device, the conventional RC-IGBT (Fig.IX-2-1)[71] should be carefully optimized in its backside structure to avoid a snap-back phenomenon in the forward output V_c-I_c characteristic. A $V_{CE(sat)}$–E_{off} tradeoff relationship of the recent SJ-RC-IGBT[73] is reported to be quite good.

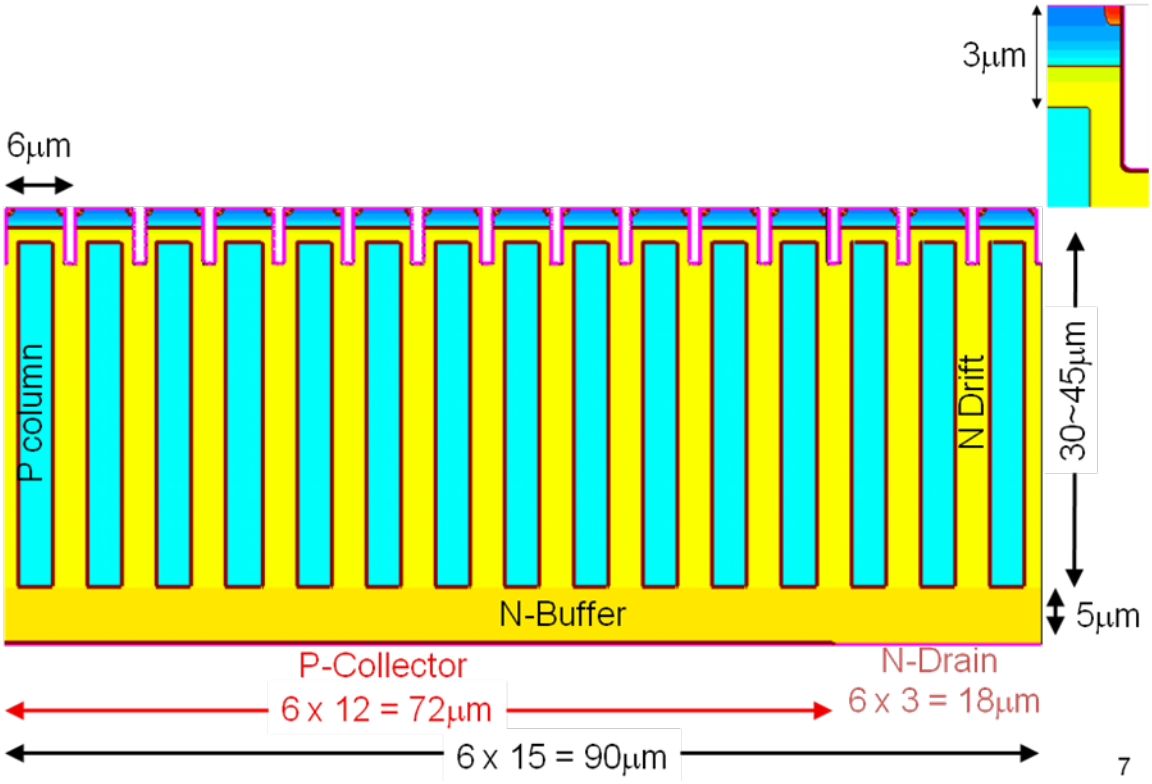


Fig. IX-2-3. SJ-RC-IGBT structure in this simulation[70]

Table IX-2-1. Summary of Structural Parameters[70]

	Cell Pitch Wcell [um]	N-Drift thickness tND [um]	N-Drift conc. cND [cm^{-3}]	N-Buffer thickness tNB [um]	N-Buffer conc. cNB [cm^{-3}]
Aa	6	30	1.4E+15	5	4.9E+15
Ab			4.2E+15		
Ac			8.3E+15		
Ad			1.0E+16		
Bc		35	8.3E+15		
Bd			1.0E+16		
Db		45	4.2E+15		
Bc2		35	8.3E+15		1.0E+16
Bd2			1.0E+16		

IX-2-2. Simulated device structure

The simulation device width is 90μm with 6μm cell pitch, and n or p column width is 3μm. The 12 of 15 columns are assigned to Light Punch Through (LPT) type IGBT with thin P-collector, and the others are to MOSFET with thin and low concentration drain region. The referred conventional IGBT and MOSFET are not shown, but simply without P-column. All the size parameters are described Fig. IX-2-3 and Table IX-2-1.

Based upon the SJ physics, the higher the N-column concentration is, the better $R_{on,sp}$ of MOSFET is. But the P/N columns should be very thin to maintain the fully depleted condition. We estimated 3μm width is realistic for the N-column as the N-drift width using our deep trench technology more than 90μm[74].

Table IX-2-2. Summary of Electrical Characteristics[70]

	BV [V]	Eave [V/μm]	Analytical BV [V] for cND	Ron,sp MOS region [m ohm cm2]	Von [V] 20A/cm^2	Von [V] 200A/cm^2	Isat [A/cm^2]	MOS-IGBT connection Jconnect [A/cm^2]	MOS-IGBT connection Vconnect [V]
Aa	616	19.0	235	45.3	0.78	1.07	4,850	15	0.77
Ab	616	19.0	103	24.3	0.49	1.04	3,650	40	0.76
Ac	580	17.8	61	16.4	0.33	1.01	3,200	53	0.71
Ad	552	17.0	53	14.4	0.29	1.00	3,004	60	0.71
Bc	661	17.6	61	17.6	0.35	1.06	3,149	49	0.74
Bd	648	17.3	53	15.9	0.32	1.04	3,039	58	0.77
Db	867	18.3	103	31.1	0.62	1.16	3,350	31	0.78
Bc2	659	17.6	61	14.1	0.28	1.06	3,125	61	0.82
Bd2	636	17.0	53	12.7	0.25	1.05	3,039	68	0.84

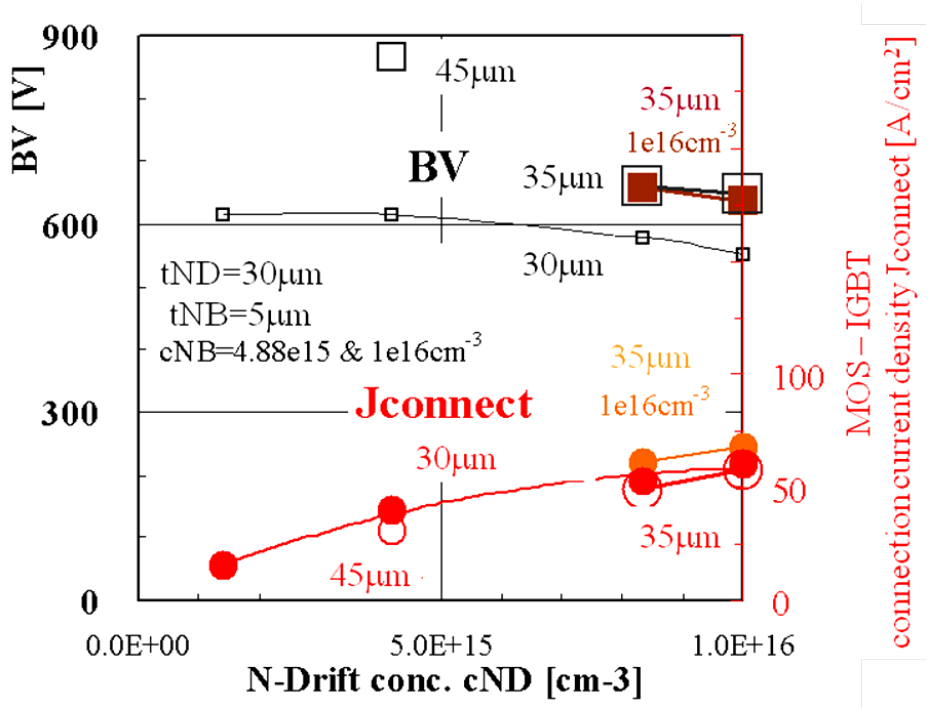


Fig. IX-2-4. N-drift conc. vs. BV & $J_{connect}$[70]

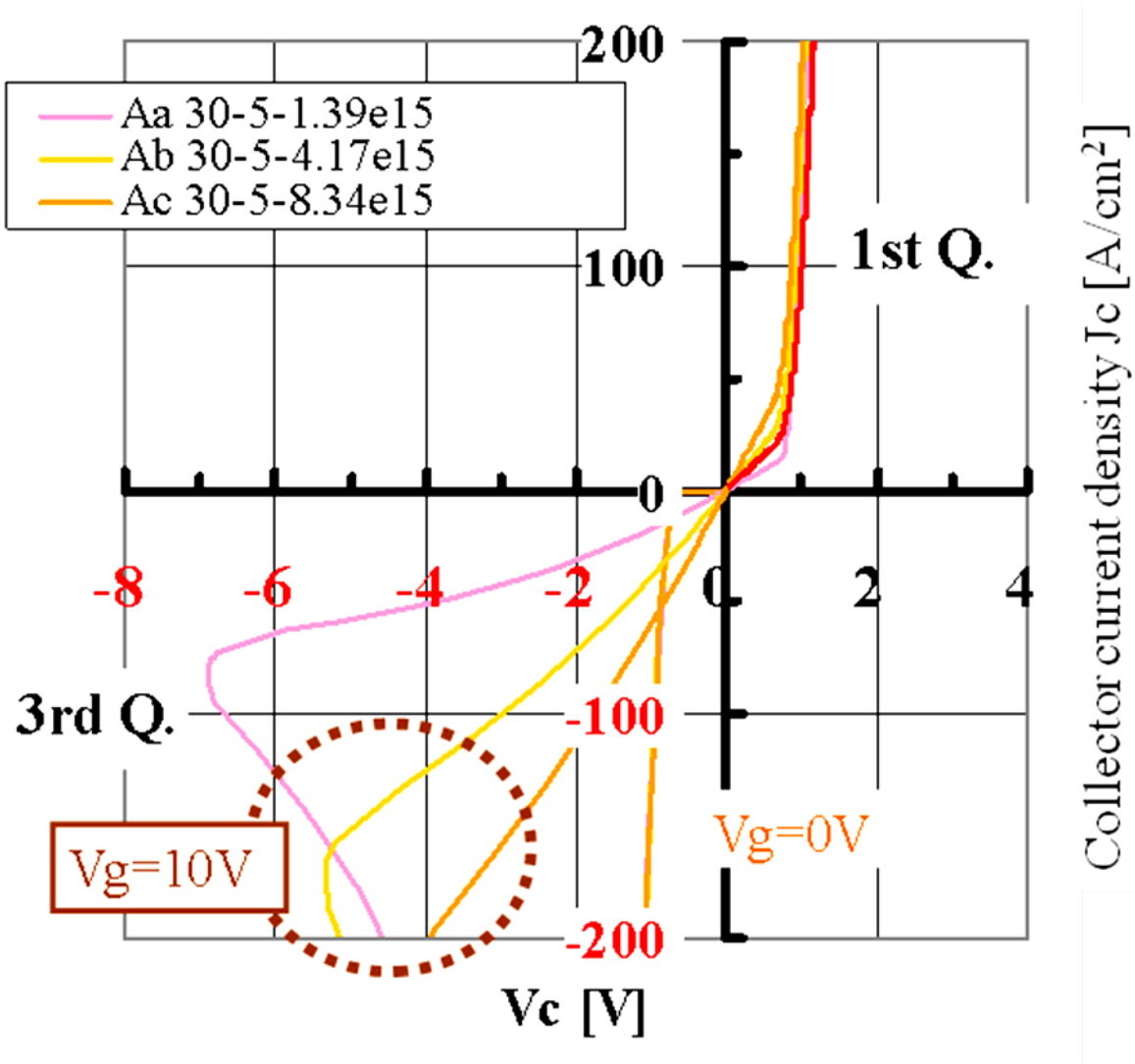


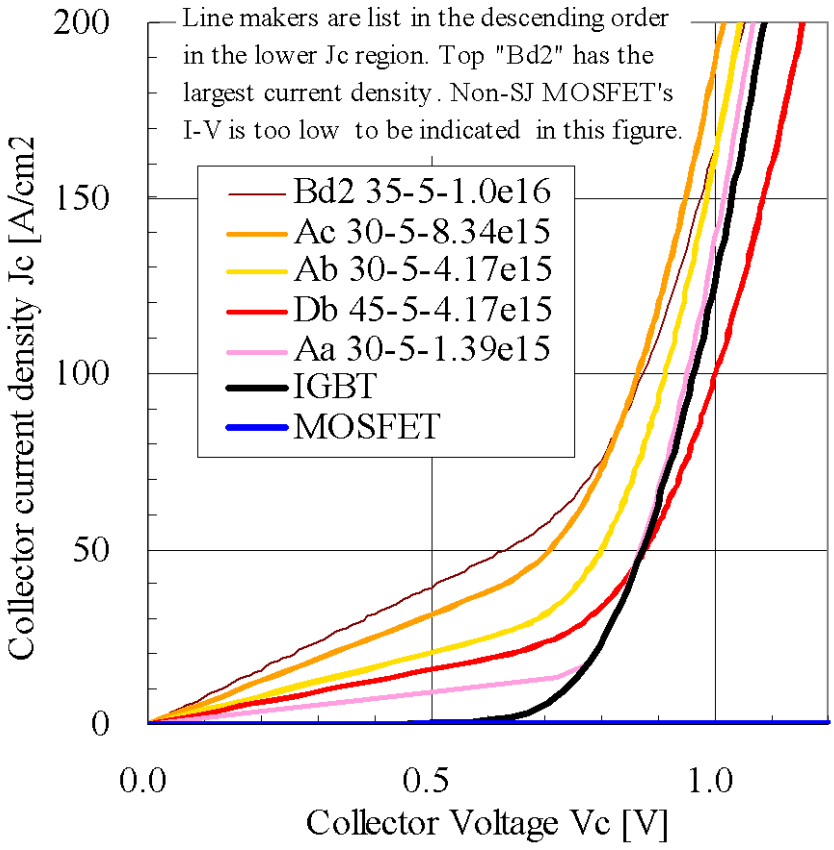
Fig. IX-2-5. Forward output V_c-I_c characteristics for both the 1st & 3rd Quadrant[70]

IX-2-3. Characteristics

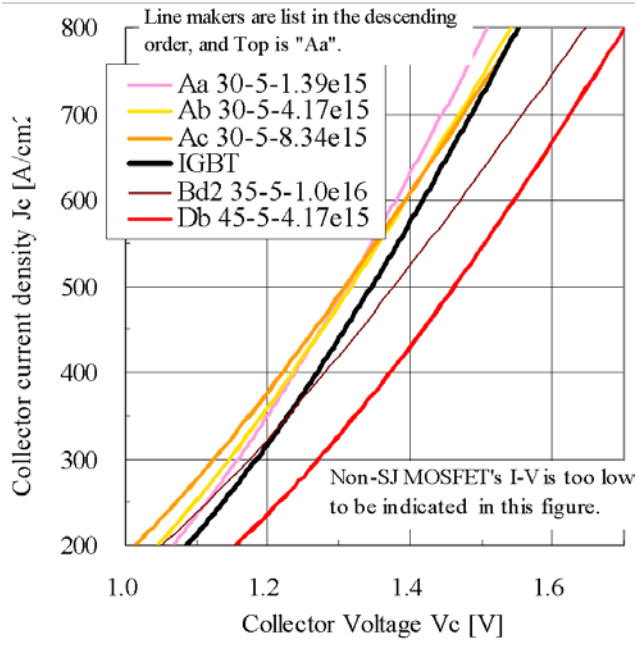
All the structural parameters are listed in Table. IX-2-1, and fundamental reference values for the concentration and thickness were estimated from the well-known analytical equations. We carefully choose this N-buffer concentration as 4.9e15 and 1e16cm^{-3} to be relatively high for the 600V class IGBT. This N-buffer could maintain only a 90V or 53V in the non-SJ operation, but enough value for UIS capability as the SJ-MOSFET operation. And these values never cause the snap-back phenomena in the first quadrant of the output V_c-I_c characteristic.

Fundamental electrical characteristics are listed in table IX-2-2. As the structural notation, capital A, B and D stand for n-column length t_{ND} 30, 35 and 45μm, small letters a, b, c and d stand for N-column concentration 1.4, 4.2, 8.3e15 and 1e16cm^{-3} and Arabian number 2 and 4 stand for N-buffer concentration 4.9e15 and 1.0e16cm^{-3}, respectively. For all the structures, the higher the N-column concentration is, the higher the Jconnect. On the other hands, decrease of Breakdown Voltage *BV* is moderate, and the longer the N-column is the slower the decreasing ratio of *BV*. Focusing on the $J_{connect}$ characteristics, effects of N-column length and

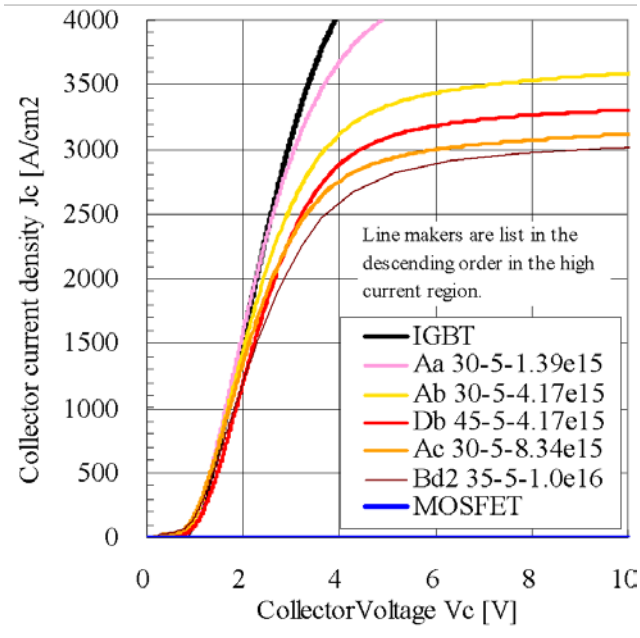
N-buffer concentration is large in the low N-column concentration region. The N-column concentration approaching 1e16cm^{-3}, the Jconnect reached almost 70A/cm^2. This $J_{connect}$ value might be the limit of this 600V class device. This is because N-column doping concentration 1e16cm^{-3} is very close to the excess carrier concentration in this current density operation.



(a) Low current density region



(b) Medium current density region



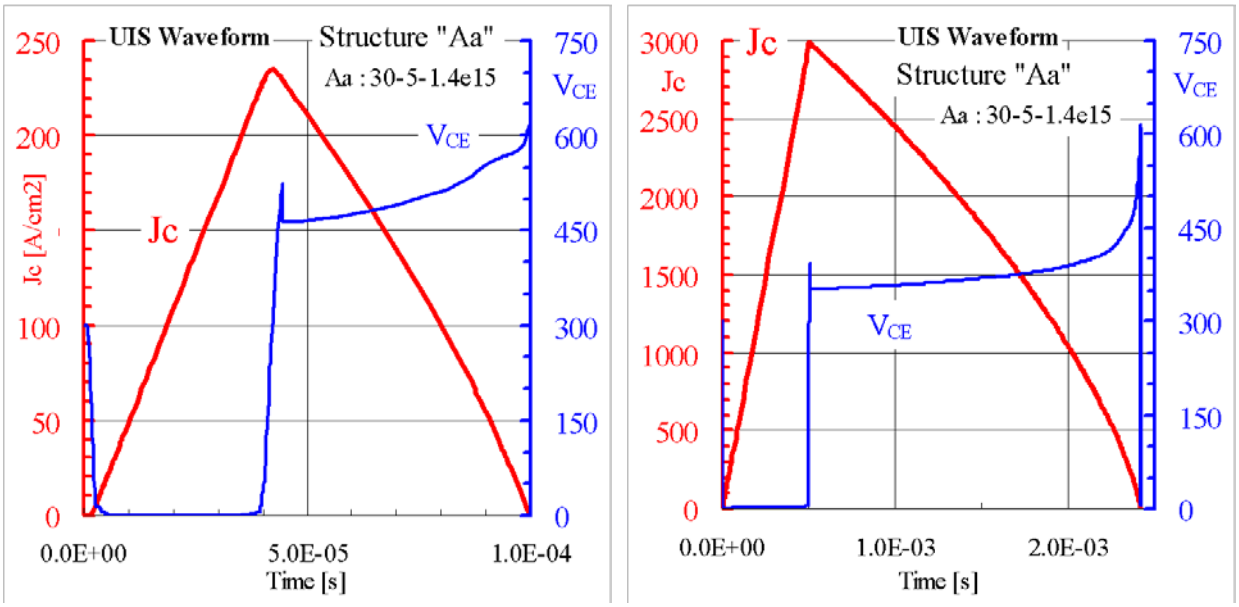
(c) High current density region

Fig. IX-2-6. the forward output V_c-I_c characteristics of SJ-RC-IGBT[70]

Both the forward and backward output V_c-I_c characteristics are shown in Fig. IX-2-5, parts of magnifications are listed in Fig. IX-2-6a, 7b and 7c. The backward output V_c-I_c characteristics as the diode in the third quadrant (Fig. IX-2-5) has a snap-back phenomenon in case of the gate positive bias to create n-channel, which makes an anode-shorted type diode. But the forward bias operation shows extremely good agreement for both MOSFET mode and IGBT mode. In Fig. IX-2-6a, the $J_{connect}$ reached 50A/cm^2, and this BV could be improved by elongated N/P column with the minimum sacrifice of Jconnect as shown in Fig. IX-2-4.

In Fig. IX-2-6a – 6c, the forward output V_c-I_c characteristics for the low, medium and high current density regions of SJ-RC-IGBT are shown in detail. The higher the N-column concentration is, the lower the $V_{CE(sat)}$ is and the higher the J_{cc} is (Fig. IX-2-6-a). But this tendency comes to a up-side-down, because the conductivity modulation is affected by the back ground doping and the lower doping is suitable for maintaining the charge neutrality in the higher current density.

Further optimization results for n-buffer and the n-drirft are list in table IX-2-2 as mentioned above. In Fig. IX-2-6 (a), line makers are list in the descending order in the lower Jc region. Top "Bd2" has the largest current density. Non-SJ MOSFET's V_c-I_c is too low to be indicated in this figure. Fig. IX-2-6 (b) and 7c are discribed as the same manner like Fig. IX-2-6 (a).



(a) a standard Jc around 200A/cm^2 (b) an extremely high Jc 3000A/cm^2

Fig. IX-2-7. UIS waveform for "Aa" structure[70]

The UIS SOA (Fig.IX-2-7) is large enough up to 3000A/cm^2, where is very close to the saturation current density as listed in table IX-2-2, in the isothermal condition of the room temperature in which it is more tough condition for device to turn off a large current density than hot temperature because of the higher impact ionization rate.

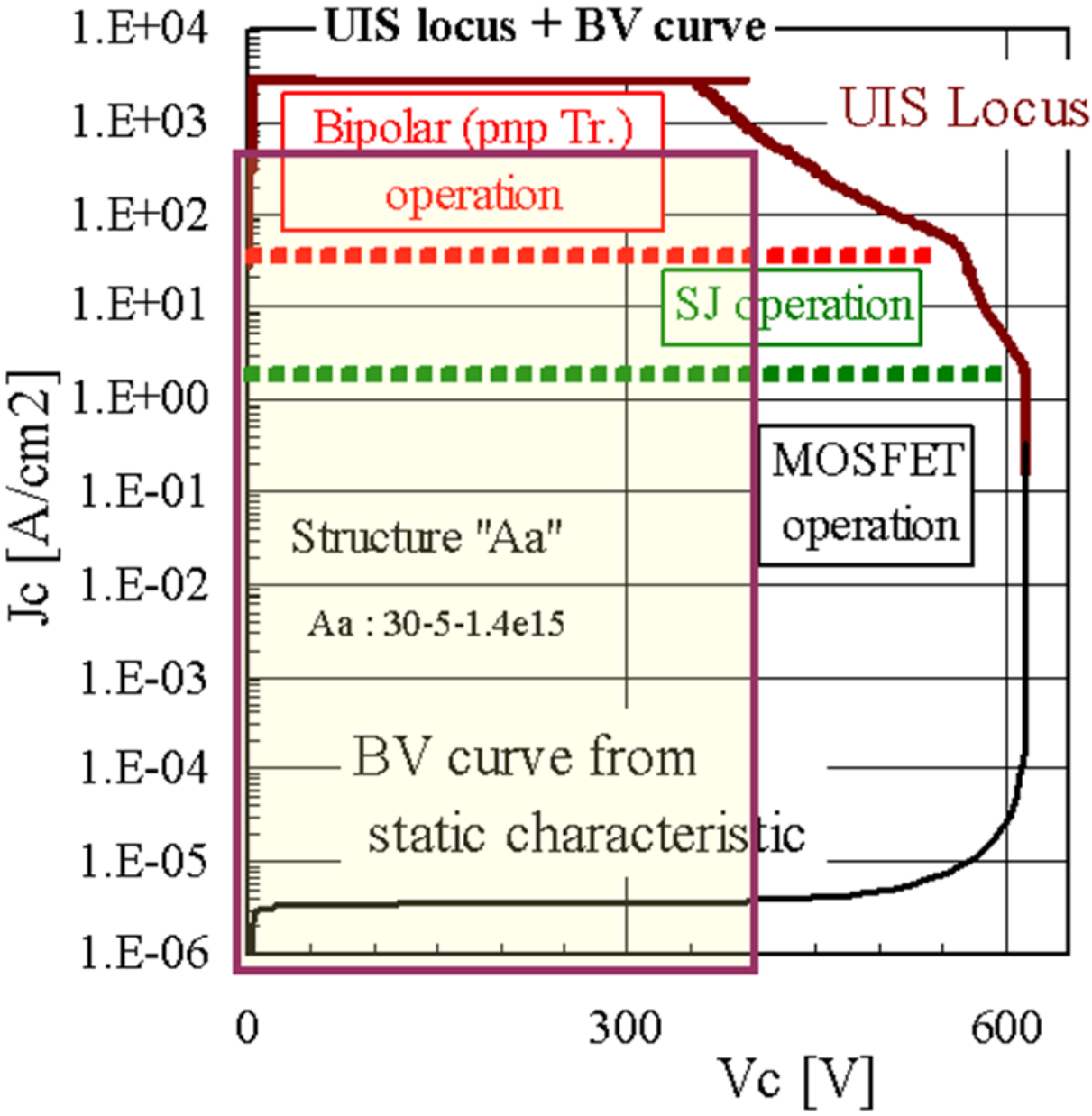


Fig. IX-2-8. UIS V_c-J_c locus with a static blocking characteristic[70]

Re-plotting UIS waveform into the static V_c-J_c locus with the conventional forward blocking V_c-J_c curve (Fig. IX-2-8), this very high UIS turn-off capability could be understood from the secondary breakdown point of view[31], where we found out two kinds of the secondary breakdown were observerd. The middle J_c range "SJ operation" means the charge imbalanced effect caused by the impact ionization generation. Too many holes generation in the N-drift region accelerates space charge of N-drift in the depletion mode, and too many electrons in the P-column, vice versa. The highest J_c region's "PNP" mode is the conventional one defined by the total N-drift thickness and the carrier lifetime characteristics.

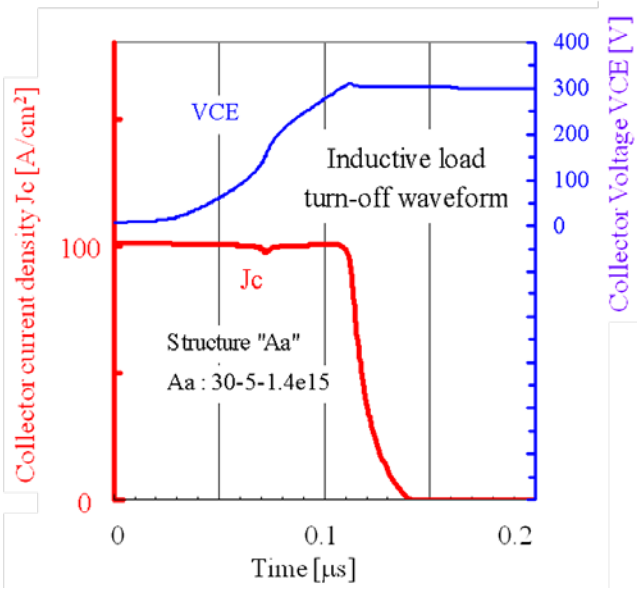


Fig. IX-2-9. Inductive load turn-off of of structure "Aa"[70]

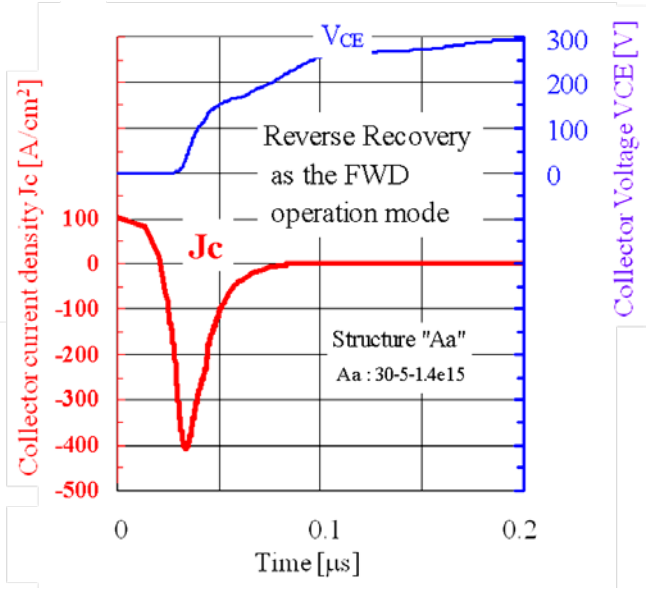


Fig. IX-2-10. Recovery waveform in FWD mode of structure "Aa"[70]

As the IGBT operation, an inductive load turn-off characteristic is confirmed. As shown in Fig. IX-2-9, no special characteristic is observed.

As the high injection rate of holes from the entire P-column sidewall in the N-drift region, a reverse recovery current I_{rr} of FWD operation is four times larger than the forward current (Fig. IX-2-10). But a turn-off failure could not be observed at least up to 100A/cm^2 of forward conduction current density J_c, and a recovery dJc/dt is kept the relatively low value on behalf of the relatively high doping concentration in the P/N column region of the main part of drift layer.

Summing up the switching characteristics for both forward and backward, both large E_{off} and I_{rr}-t_{rr}-E_{rr} (Reverse recovery current, reverse recovery time and reverse recovery energy loss) are the characteristics to be reduced in the next stage by optimizing carrier lifetime control method.

IX-3. Ideal forward output V_c-I_c characteristics

Not a standard IGBT but an RC-IGBT reason of a SJ-MOSFET with the well-tempered N-buffer is a good approach to improve the forward V_c-I_c characteristics in the low J_c region. In the 600V class, this SJ-RC combination device acts as the unipolar MOSFET in the J_c range of 50 A/cm^2, where is a quarter or a half of the rated current density for this voltage class device, without any sacrifice concerning about SOA. Assuming inverter operation, the third quadrant current conduction and reverse recovery characteristics might be improved in the next stage of development through the carrier lifetime control process.

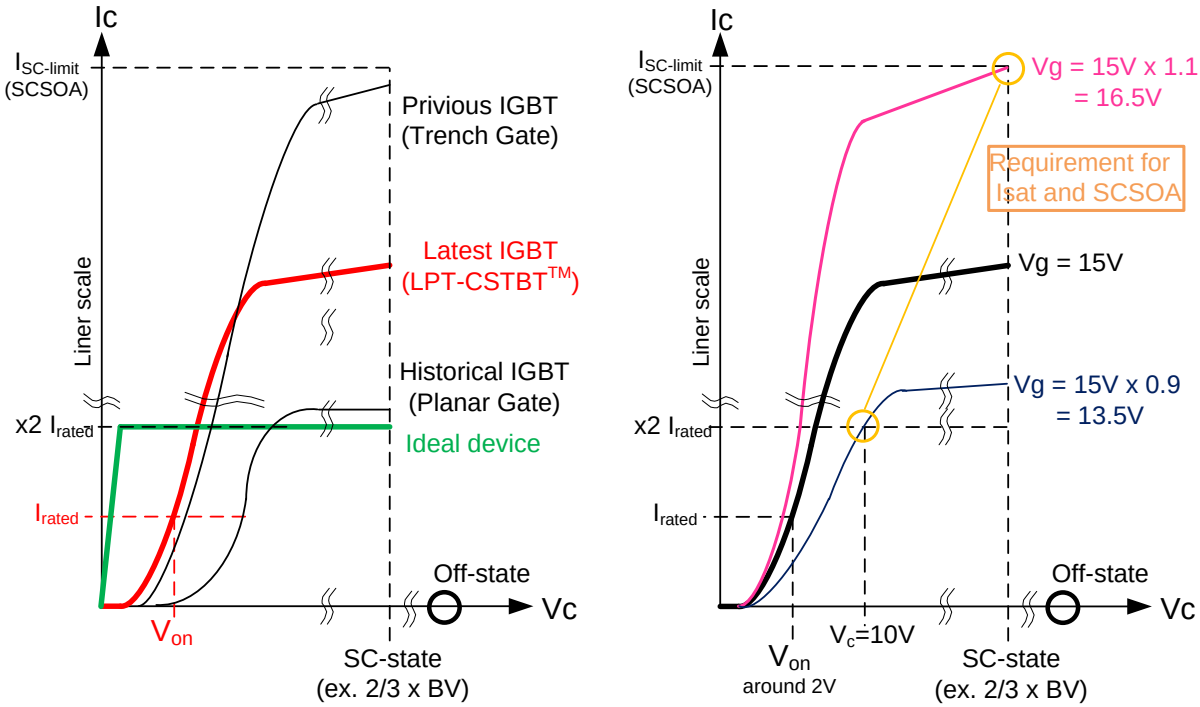


Fig. IX-3-1. Ideal V_{on} curve and industrial specification of IGBT

From the low V_{on} point of view, the ohmic and steep characteristic, which is illustrated in Fig. IX-3-1 (a) as the "ideal device", is favorable. At the same moment, I_{sat} should be as low as possible from the SCSOA point of view. That has been already deeply discussed in chapter VII. But there is no solution for this ideal V_{on} curve as far as being the bipolar device with the PN junction for the P-collector. The above SJ-RC-IGBT would be one of the possibilities as the hybrid device of the unipolar-bipolar operation.

X. Summary of SOA

In the medium and high voltage region (from 200V up to 6500V), the major application of IGBT, which is the gate controlled bipolar power semiconductor device with the conductivity modulation, is the L (inductive) load like a motor control in the converter/inverter circuit. In the L-load switching, the turn-on and turn-off locus in the first quadrant of the V_c-I_c plane extend very close to the FBSOA and RBSOA boundaries of device, respectively. That is quite different from the R-load switching, in which power MOSFET and a signal devices like an LSI are major, in the simple shape of the load-line. So, as the device design philosophy, it is extremely important to estimate the FBSOA and RBSOA in the R&D phase of device design.

According to the progress of the numerical device simulation technology, “along the industrial definitions”, direct simulation of FBSOA, RBSOA and SCSOA have come to be available as the transient switching characteristics. But each “transient” calculation brings one point data in the V_c-I_c plane, and those point data could be neither curve nor area to be identified as the SOA (area). So, this study suggested that those FBSOA, RBSOA and SCSOA could be easily estimated from the simple computation of the static characteristic such as V_{on} and BV up to the very high current density and the time integral of I_{sat}.

From the device evaluation and test point of view, the major technology has been established for digital signal deices like a Memory or Logic as LSI. The fundamental operations of these signal processing devices are basically R-load switching, which goes and comes between "0" of OFF state and "1" of ON state. The "test" for these kind of digital device needs only two position of "OFF" and "ON", which are very closely located along the X-Y axis in the V_c-I_c plane. In contrast, the test for the power device requires the area coverage including the right-upper corner point in V_c-I_c plane. Although Digital "OFF" and "ON" states are easily testified as the small signal DC test, it has been extremely difficult to find out the joint region of the FBSOA and the RBSOA of power device because of very large electrical power and energy coming from the product of high voltage of some hundreds or thousands and current in the order of hundred or thousand ampere, it sometimes reaches not only the destruction of DUT but also the literally explosion of the whole system of test facilities. For this electrical test procedure point of view, above the simulation approach for all the SOAs would give us very good and many hits which kind of value in the small power might be import and how to evaluate those. Visualization of SOAs are much interesting and useful task for even in the industrial test and specification procedure in the mass-production phase.

X-1. On the 2-dimensional V_c-I_c plane : SOA = FBSOA + RBSOA

These two figures are discussed in chapter VII. Again here is as the summary of visualization of SOA.

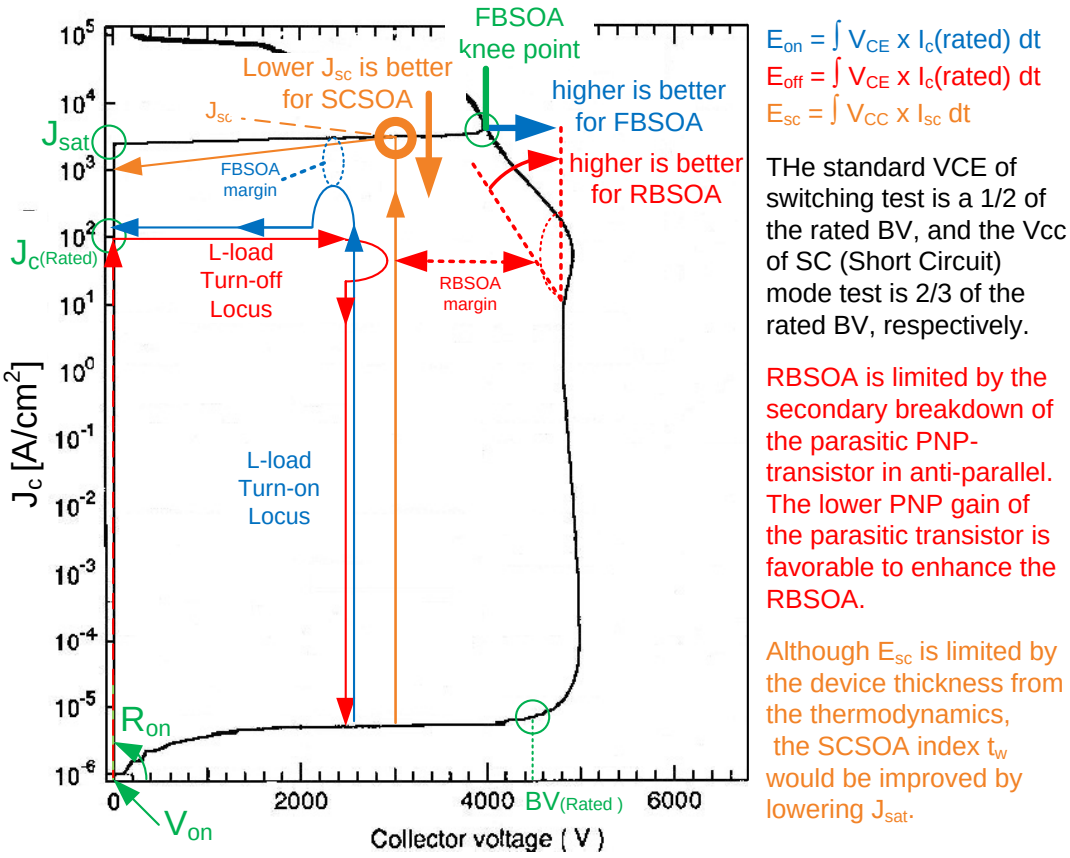


Fig. VII-9. Operational area as the combination of FBSOA and RBSOA in V_c-I_c plane

X-2. In the 3-dimensional V_c-I_c-time space: SCSOA

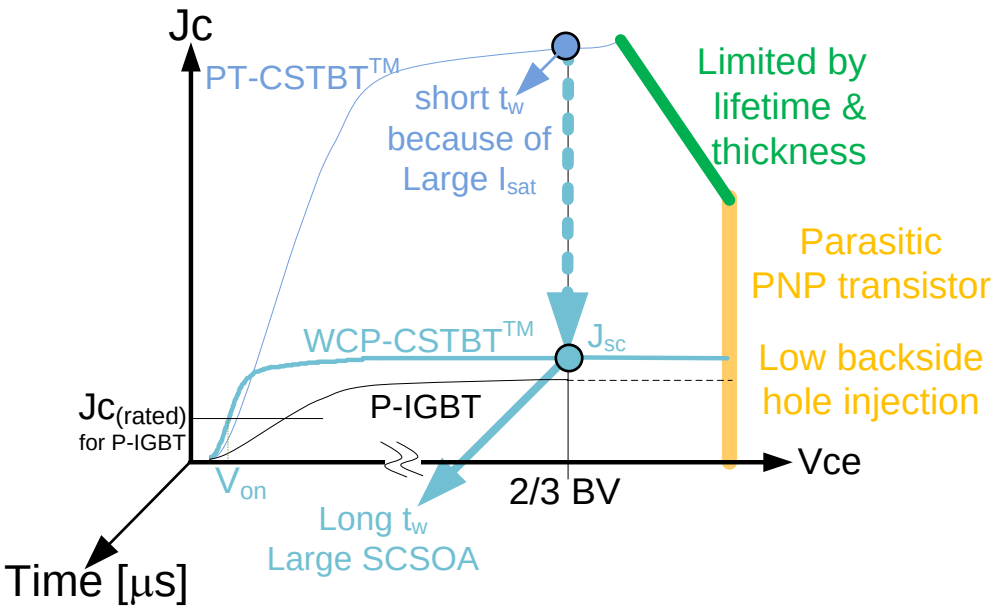


Fig. VII-8. Summary of schematic 2-dimensional and 3-dimensional SOA: FBSOA, RBSOA & SCSOA

XI. Conclusion

There is some conflict situation for the definition about SOAs from the industrial specification and from the physical meaning. Even in this compromising situation, it is worth to study detail about the boundaries of SOAs from the device physics point of view.

In this study, using the numerical simulation, it was found out that the extended DC characteristics of *BV* and V_{on} correspond to RBSOA and FBSOA, respectively. SCSOA can also be easily estimated through I_{sat} characteristics. This result is quite natural and easily understood through the visualization of whole SOA shape.

To expand the RBSOA, it is very useful to reduce the hole injection form the P-collector of the device's backside.

To improve the fundamental tradeoff of V_{on} -E_{off}, it is necessary to increase the electron injection from the N-emitter of the device's front-side with the control gate structure. But the V_{on} and the SCSOA are also in the strong tradeoff relationship.

To maintain the sufficient SCSOA, it is very effective for I_{sat} to be saturated in the low current density keeping the low V_{on} characteristic during the low current density region, for example using high injection gate structure of CSTBT™ with the wide-cell pitch structure.

As the next step of the application, this method is very useful and important to design the device structure for both the active cell structure and the peripheral region like the termination region. The most effective and attractive point of this approach is "time and cost saving". That has been achieved by the minimum test run or fabrication without the "cut and try" phase by using the simulation experiment.

There still are several limitations of using this simulation approach, such as, too long time or too large memory size for the three dimensional simulation, no clear models for the wafer fabrication process details, no authorized physical parameters for the WBG (Wide Band Gap) materials like a SiC or GaN and so on. So the wafer process technology has still taken an important role in the development power semiconductor device field, especially for the Thin Wafer Process Technology as the backside process of LPT type devices.

On the other hands, Diamond has a Negative electron Affinity characteristic which has a potential to achieve the vacuum tube having the pentagonal-electrode characteristic in the analog circuit usage. It is not potentially allocated in the Si material. So the WBG approach is necessary.

Moreover, many ideas still remain like a Super-Junction, which had been hit by the historical giant and has come to be realized recently. As far as silicon material is concerned, there would be more room to be improved or to leap to the several next generations. That is supported by the will for the sustainability of human-race.

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Chapter IV

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