A Phase Frequency Detector Constructed with Dynamic CMOS Gates for Low Power PLL

Yoshizawa, Hiroyasu
Department of Electronic Device Engineering, Faculty of Information Science and Electrical Engineering, Kyushu University : Graduate Student

Taniguchi, Kenji
Department of Electronic Device Engineering, Faculty of Information Science and Electrical Engineering, Kyushu University

Nakashi, Kenichi
Department of Electronic Device Engineering, Faculty of Information Science and Electrical Engineering, Kyushu University

https://doi.org/10.15017/1485032

出版情報：九州大学大学院システム情報科学紀要. 2 (1), pp.53-58, 1997-03-26. 九州大学大学院システム情報科学研究院
バージョン：
権利関係：

九州大学大学院
システム情報科学研究科報告
第2巻 第1号 平成9年3月

Research Reports on Information Science and
Electrical Engineering of Kyushu University
Vol.2, No.1, March 1997

A Phase Frequency Detector Constructed with Dynamic CMOS Gates for Low Power PLL

Hiroyasu YOSHIZAWA* , Kenji TANIGUCHI** and Kenichi NAKASHI**

(Received December 24, 1996)

Abstract: To reduce power dissipation of LSI drastically, it is very effective to lower supply voltage, for example from 5V to 3V or 3V to 1.5V, because power dissipation is proportional to the square of supply voltage. However, reduction of supply voltage results in the increase of propagation delay of the constituent gates. In case of PFD (Phase Frequency Detector) which is one of the components of PLL (Phase Locked Loop), increase of the propagation delay deteriorates its phase detecting characteristics and therefore pull-in characteristics of the PLL. One of the solutions to this problem is the construction of PFD with dynamic CMOS gates as we proposed in our earlier paper. In this paper, we propose a systematic and straightforward method to construct PFD with dynamic CMOS gates and clarify the effect of the dynamic structure on PFD and PLL performance.

Keywords: PFD, PLL, Dynamic CMOS, Low power, Low supply voltage

1. Introduction

Recently, power supply by battery has become important in many electronic equipments, especially in movable telecommunication equipments such as PHS, handy telephone system. For using the battery power supply, it is very important to reduce the power dissipation of the circuits and therefore to reduce the supply voltage[1]. However, reducing the supply voltage causes the reduction of drain current of the MOS transistor which is the charge/discharge current of the load capacitance such as the gate capacitance. Because of the reduction of charge/discharge current, the propagation delay of the gates increases.

In many electric equipments, especially with digital signal control, the performance are dependent on the operating frequency and the increase of the propagation delay limits the operating frequency. In the PLL used for retiming or clock recovery, the increase of the propagation delay also affect its pull-in characteristics. PLL is mainly composed of PFD[2),3)] (or PC), VCO and LPF (Low Pass Filter). Among these components, PFD is most strongly influenced by the increments of the delay.

In this paper, we construct PFD with dynamic CMOS gates instead of conventional static CMOS gates. The dynamic CMOS gate[4)] employed stores its information in the output capacitance (mainly succeeding gate capacitance and line capacitance) like in a DRAM. So it is called "dynamic".

Typically, *Domino* CMOS[5),6)] with precharge/evaluate control by clock has been used as a dynamic logic. However, for the asynchronous logic circuit like PFD, precharge/evaluate control is not suitable and other dynamic CMOS gate is required as we proposed in our earlier paper[7),8)]. However, clear and systematic construction method for the dynamic CMOS gates has not been established. In this paper, a new systematic construction method is proposed for the dynamic CMOS gate applicable to the asynchronous logic, and the evaluation results of the PFD and PLL at low voltage (VDD=3V) are shown. For evaluation, PSpice simulation is used.

2. Construction of PFD with dynamic CMOS gates

2.1 Construction method

The asynchronous logic circuit has not been easy to construct with dynamic CMOS gates compared with conventional static CMOS gates. This is because clear construction method has not been established. In this paper, the following construction method of dynamic CMOS gates is proposed.

procedure 1:

For basic dynamic CMOS gate, the logical relationship between inputs and output is extracted.

procedure 2:

To satisfy the logic equation of the circuit to be designed, the basic gates are combined according to the logical relationship extracted above.

* Department of Electronic Device Engineering, Graduate Student

** Department of Electronic Device Engineering

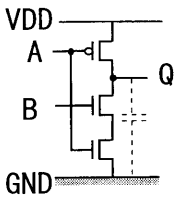


Fig.1 Example of dynamic CMOS gate

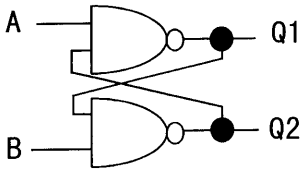


Fig.2 RS-NAND Flip/Flop

Table 1 Truth table of the dynamic CMOS gate

A	B	Q_n	Q_{n+1}
0	0	X	1
0	1	X	1
1	1	X	0
1	0	Q_n	Q_n

The procedure 1 is explained as follows. The circuit shown in **Fig.1** is a dynamic CMOS gate with two inputs and an output. Now, if it is assumed that Q_n is the voltage of the output capacitance at the present state and Q_{n+1} is one at the next state, the relationship between inputs and output becomes as shown in **Table 1**. In this table, "0" corresponds to "low" or "GND", "1" corresponds to "high" or "VDD", and "X" correspond to "don't care". As shown in the table, when input A is "1" and input B is "0", charging/discharging current path of output capacitance is cut off and then the output at the present state becomes the output at the next one. Using this table, the logic equation of this gate is obtained as follows.

$$Q_{n+1} = \overline{A} + \overline{B} \cdot Q_n \tag{1}$$

This logic equation is valid except for inadequate charged/discharged condition in transition or long pulse period where charge leakage occurs.

In the procedure 2, we extract the logic equation of the circuit to be designed at first. And next, according to the equation, we combine the basic dynamic CMOS gates and the logic equation. In general, it is easy to implement logic equation with static CMOS gates and therefore in this process, it is better to find the static CMOS gates corresponding to the logic equation and to transform the static CMOS gates to dynamic CMOS gates. For example, the static CMOS gate shown in **Fig.2** is the RS-NAND Flip/Flop which is widely used to implement many kinds of Flip/Flops. Now, extracting the logic equations of this Flip/Flop, the following two equations are obtained

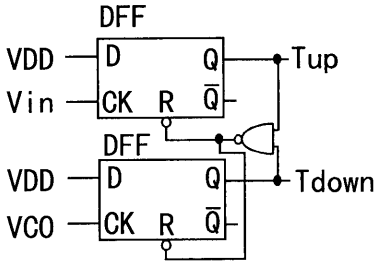


Fig.3 PFD circuit

$$Q1_{n+1} = \overline{\overline{A} \cdot \overline{B \cdot Q1_n}} = \overline{A} + B \cdot Q1_n \tag{2}$$

$$Q2_{n+1} = \overline{\overline{B} \cdot \overline{A \cdot Q2_n}} = \overline{B} + A \cdot Q2_n \tag{3}$$

These logic equations resemble the equation 1. Transforming the static CMOS Flip/Flop shown in **Fig.2** making use of such correspondence between equation 1 and 2, it is easy to implement the circuit with dynamic CMOS gates. Of course, the basic dynamic CMOS gate can not always find a part of static CMOS gates to replace directly and the simple transformation is not effected. And in implementing, we have to take care not to deteriorate the advantages of dynamic circuit.

2.2 Implementation of PFD

Figure 3 shows the PFD composed of DFFs (Delay Flip/Flops). This is the circuit to detect phase error or frequency error between input signal and VCO output in PLL. In this circuit, the pulse width difference of the two outputs(Tup and Tdown) corresponds to the phase error. In this type PFD, the performance of the PFD is directly influenced by DFF. So it is most effective to improve the performance of the DFF. Now, according to the method mentioned in Section 2.1, we implement this DFF with the dynamic CMOS gates. In this DFF, "D" is constantly "high" and "$\overline{Q}$" is not used, so it is able to regard this circuit as the Flip/Flop with two inputs (Input and $\overline{\text{Reset}}$) and an output (Q). In **Fig.4**,

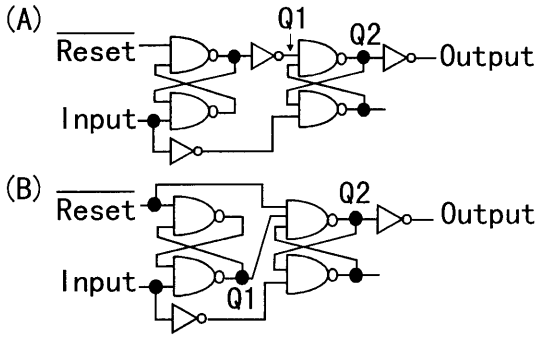


Fig.4 Implementation with static CMOS gate

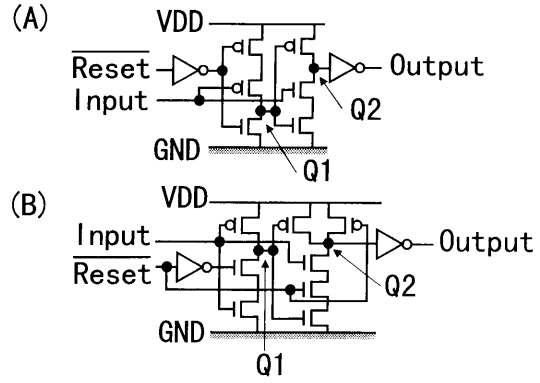


Fig.5 Implementation with dynamic CMOS gate

Flip/Flops implemented with static CMOS gates by two kind of logic equation are shown. In this figure, Flip/Flop (A) is constructed with only NOT and NAND ,and in the Flip/Flop (B), 3 inputs NAND is used in addition to NAND and NOT. For these circuits, following logic equations are derived.

F/F(A) :

$$\begin{aligned} Q1_{n+1} &= \overline{\overline{\overline{Reset} \cdot Input \cdot \overline{Q1_n}}} \\ &= \overline{Reset} \cdot (\overline{Input} + Q1_n) \end{aligned} \quad (4)$$

$$\begin{aligned} Q2_{n+1} &= \overline{Q1_{n+1} \cdot \overline{\overline{Input} \cdot Q2_n}} \\ &= \overline{Q1_{n+1}} + \overline{Input} \cdot Q2_n \end{aligned} \quad (5)$$

F/F(B) :

$$\begin{aligned} Q1_{n+1} &= \overline{Input \cdot \overline{\overline{Reset} \cdot Q1_n}} \\ &= \overline{Input} + \overline{Reset} \cdot Q1_n \end{aligned} \quad (6)$$

$$\begin{aligned} Q2_{n+1} &= \overline{\overline{Reset} \cdot Q1_{n+1} \cdot \overline{Input} \cdot Q2_n} \\ &= Reset + \overline{Q1_{n+1}} + \overline{Input} \cdot Q2_n \end{aligned} \quad (7)$$

In these equations, symbols (Q1, Q2, input, $\overline{Reset}$) correspond to those of **Fig.4** and the symbol "n" represent the present state. In both equations of F/F(A) and F/F(B), substituting the equation for $Q1_{n+1}$ to the equation for $Q2_{n+1}$, the following same logic equation is derived.

$$Q2_{n+1} = Reset + Input \cdot \overline{Q1_n} + \overline{Input} \cdot Q2_n \quad (8)$$

Next, transforming the static CMOS gate to the dynamic one according to these equations, the circuits shown in **Fig.5** are derived. In this transformation, the correspondences shown in **Fig.6** are used. With these derived dynamic CMOS Flip/Flops and

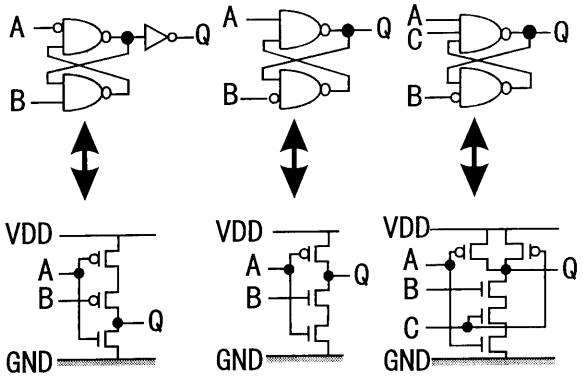


Fig.6 Correspondence between dynamic static CMOS gates and dynamic CMOS gates

a NAND gate, the dynamic CMOS PFD is implemented.

3. Evaluation by PSpice simulation

3.1 Evaluation of the Flip/Flop

To improve the performance, Flip/Flop has been implemented with the dynamic CMOS gates as described in Section 2. In this section, the effect of dynamic structure is evaluated by PSpice simulation.

Table 2 and **Figure 7** show the simulation results on the Flip/Flops shown in **Fig.4** and **Fig.5**. In this simulation, supply voltage VDD is 3[V] and 0.8[μm] CMOS model is used. Symbols (A), (B) in the table and the figure correspond to the Flip/Flop (A) and (B) in **Fig.4** and **Fig.5**.

In **Table 2**, the result mainly shows the delay characteristics of the output pulse. As shown in the table, comparing the static type (A) and dynamic type (B), both propagation delay and minimum limit of input and $\overline{Reset}$ pulse width become

Table 2 Characteristics of the parts circuit

	static		dynamic	
type	(A)	(B)	(A)	(B)
tpdr[ps]	1300	1610	490	680
tpdf[ps]	1330	720	930	600
minp[ps]	670	670	350	400
mres[ps]	590	610	430	420

tpdr : rise propagation delay
tpdf : fall propagation delay
minp : minimum Input pulse width
mres : minimum Reset pulse width

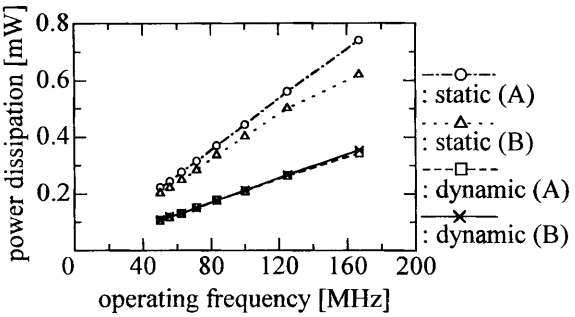


Fig.7 Power characteristics of the Flip/Flops

about half by dynamic structure. This improvement is dependent on the reduction of signal path length from input to output by dynamic structure. Considering the static type (B) and dynamic type (A), unbalance of propagation delays of rising and falling occurs. These are the case of somewhat reduced improvement, but roughly the performance of delay is improved by two times in dynamic structure.

On the other hand, **Fig.7** shows the power dissipation characteristics. In this figure, X axis shows the operating frequency and Y axis shows the power dissipation. As shown in the figure, the power of dynamic Flip/Flop is about half of the static one at the same operating conditions. This improvement is achieved by the reduction of nodes with the load capacitance to be charged/discharged. From these results, the performance of the Flip/Flop can be improved about twice by dynamic structure.

In the static type (B) and dynamic type (A), there is the big unbalance of propagation delay and this kind of big unbalance deteriorates the phase detecting characteristics of the PFD. So static type (A) is used to implement the static type PFD and dynamic type (B) is used to implement the dynamic type PFD.

Considering this result, it must be also taken care of the following point. Among these F/Fs, the better type in the static is not always better type in the dynamic and therefore it is necessary to check the power and the propagation delay whether the implemented circuit is better one. To evaluate propagation delay and power dissipation relatively, there is a simple way as follows. For propagation delay, measuring the signal path delay in unit of an inverter delay, relative propagation delay can be compared. For power dissipation, the number of output node normalized by unit gate corresponds to the relative power dissipation. For example, evaluating the propagation delay and the number of output node of the F/Fs implemented in Section 2, the result shown in **Table 3** is derived. In evaluating the delay, the delay of each gates are assumed as follows. These assumptions are dependent on the layout pattern. In the static CMOS gates, the rise propagation delay of NOT, NAND and 3 Input NAND are all 1 unit, and the fall propagation delay of NOT and NAND are 1 unit and that of 3 Input NAND is 2 unit respectively. In the dynamic CMOS gates, the propagation delay is 1 unit in case of the number of pass gate for charging/discharging is one or two, and the propagation delay is 2 unit in case of the number of the pass gate is three. Comparing **Table 2** and **Table 3**, the estimation result roughly correspond with the PSpice simulation result. Of course, these values are rough estimation and strictly, it is necessary to consider the effect of fan-in, fan-out and line capacitance for delay and the effective charging/discharging times (switching probability) and load capacitance of output node and direct current flow in state transition for power[9].

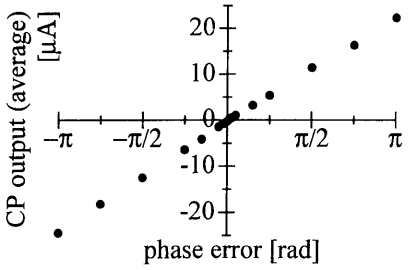
Table 3 Rough estimation of the F/Fs

	static		dynamic	
type	(A)	(B)	(A)	(B)
tpdr	4	5	2	3
tpdf	4	2	4	2
power	7	6	4	4

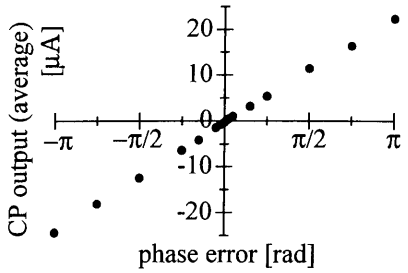
tpdr : rise propagation delay
tpdf : fall propagation delay

3.2 Evaluation of the PFD

The Implemented PFD detects the phase error between input signal and VCO output and then detected phase error is transformed into current by CP(charge Pump)[5]. In this type PFD, average CP output is proportional to the phase error. **Figure 8** shows the phase detecting characteristics of the implemented PFD at 125MHz operation. In these figures, (a) shows the result of static CMOS type



(a) static CMOS type



(b) dynamic CMOS type

Fig.8 Phase detecting characteristics of the PFD

PFD and (b) shows the result of the dynamic type PFD and X axis shows the phase error[rad] and Y axis shows the average CP output current[μA]. As shown in the figures, both PFDs have linear phase detecting characteristics. From this result, it is confirmed that the Flip/Flop implemented with dynamic CMOS gates performs properly in the PFD. At the low operating frequency such as 125MHz , the phase detecting characteristics does not show the influence of the delay. However, at high operating frequency, the propagation delay deteriorates the linearity of the characteristics or causes the misdetection of phase error. In the PLL, the deterioration of the phase detecting characteristics deteriorates the pull-in characteristics.

3.3 Evaluation of the PLL

In this section, performance of the PLL is evaluated. In this simulation, supply voltage is 3[V] and 0.8[μm] CMOS is used. **Figure 9** shows the block diagram of the PLL. This PLL consists of PFD, CP, LPF and VCO. Among these components, PFD is only implemented by both static CMOS and dynamic CMOS to evaluate the effect of dynamic structure in the PFD.

Figure 10 shows the power and pull-in characteristics of PLL. In this figure, X axis is pull-in frequency, Y axis is the power dissipation after pull-in, the solid line shows the result of the PLL with dynamic PFD and the broken line is the

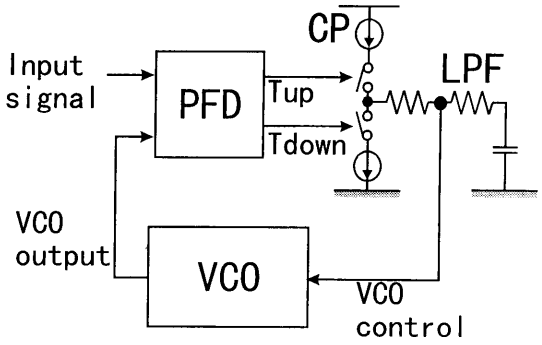


Fig.9 Block diagram of the PLL

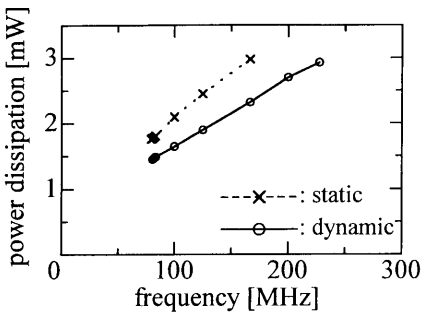


Fig.10 Power to frequency characteristics of the PLL

result of the PLL with static PFD. As shown in the figure, the pull-in range of the PLL is about 145MHz (225MHz-80MHz) with dynamic one and about 85MHz (165MHz-80MHz) with static one. And about the power dissipation, the dynamic one is about 80% of the static one at the same operating frequency. From these results, pull-in range is improved about 70% by reduction of propagation delay and the power dissipation is reduced about 20% by the reduction of the power dissipation of the Flip/Flops.

Well, if pull-in range of the static one is improved to the same range of the dynamic one, the static one will need about 5[V] as the supply voltage. Then, comparing the power dissipation, the dynamic one is about 30% of the static one at the same operating frequency. In other words, by dynamic structure, it is possible to reduce the supply voltage without deteriorating the performance achieved in static one.

4. Conclusion

In this paper, to reduce the propagation delay for low supply voltage and therefore at low power dissipation, we constructed the PFD with dynamic CMOS gates. To construct the circuit easily, a systematic and straightforward construction method

has been proposed.

By PSpice simulation, it has been confirmed that the component of PFD implemented according to proposed method has better performance compared with static CMOS one and the proposed method is effective in implementation. In this study, as an example, we implemented the F/F circuit of PFD, but it is possible to apply this method widely to other logic circuits.

From the results of evaluation about PLL, it has been confirmed that the supply voltage is able to be reduced by dynamic structure without deteriorating the performance achievable by static structure and that the construction with dynamic CMOS gates is effective for the reduction of supply voltage.

References

1) J. P. Uyemura, "Fundamentals of MOS Digital Integrated Circuits", Addition-Wesley,1988,pp.188-196.
2) C.A.Sharpe, "A 3-state Phase detector can improve your next PLL design",EDN,pp.55-59,1976.
3) B.Razabi, "Design of Monolithic Phase-Locked Loops and Clock Recovery Circuits", IEEE press, 1996, pp24-29
4) H.Notani, H.Kondou and Y.Matsuda, "A 622 MHz CMOS Phase-Locked Loop with Precharge-type Phase Frequency detector",1994 Symposium on VLSI circuits, pp.75-76, 1994.
5) R.L.Geiger, P.E.Allen, N.R.Strader, "VLSI design techniques for analog and digitalcircuit", McGRAW-HILL, 1990, pp.817-821
6) H.Fukuda, T.Matsumura, "A study of Dommino-type CMOS Multiple-valued Logic circuit with Pipelining Operations", proc. of the 1995 IEICE general conference, p194, 1995.
7) H.Yoshizawa, K.Taniguchi, H.Shirahama, K.Nakashi, "A Low Power 622MHz CMOS Phase-Locked Loop with Source-coupled VCO and PFD Uniquely Designed Inverters", proc. of ITC-CSCC'96,pp.318-321, 1996
8) H.Yoshizawa, K.Taniguchi, K.Nakashi, "A low power Phase Frequency Detector with dynamic structure", proc. of the 1996 IEICE general conference, p.284, 1996.
9) T.Douseki, S.Shigematu, S.Mutoh, "MTCMOS circuit performance using Energy-Delay Product", proc. of the 1995 IEICE general conference, p.270, 1995.