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https://doi.org/10.15017/1475363

出版情報：九州大学大学院システム情報科学紀要. 2 (1), pp.47-52, 1997-03-26. 九州大学大学院システム情報科学研究院
バージョン：
権利関係：

九州大学大学院
システム情報科学研究科報告
第2巻 第1号 平成9年3月

Research Reports on Information Science and
Electrical Engineering of Kyushu University
Vol.2, No.1, March 1997

RTD/HEMT Logic Circuits and Their Functional Circuits Application

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(Received December 24, 1996)

Abstract: This paper describes low-power and high-speed RTD/HEMT (Resonant Tunneling Diode / High-Electron Mobility Transistor) logic circuits. In order to estimate RTD/HEMT logic gates using ordinary GaAs/AlGaAs HEMT in detail by using real device parameters extracted from measured values, we have examined their characteristics. Fundamental characteristics of logic gates are examined and compared with resistor-load and depletion-mode HEMT (D-HEMT) load inverters. The results show that RTD/HEMT inverter is the fastest among them. Their application to functional circuits such as phase comparator (PC) and voltage controlled oscillator (VCO) used in PLL are also described.

Keywords: HEMT, RTD, DCFL, PLL, Low-power, High-speed, Quantum-effect

1. Introduction

Resonant-tunneling diode (RTD), one of the quantum effect devices, shows a unique I-V characteristics known as negative differential resistance (NDR) due to quantum effect. Because of its NDR characteristics, it has attracted wide attention in high-speed, low-power application fields. It has been reported that high-quality RTDs can oscillate up to 712GHz [1]. And high electron mobility transistor (HEMT) is widely used in the optical communication or broadcast satellite communication systems, because it has low-noise and high-speed characteristics. Combination circuits of these two devices are expected to be one of the candidates for the high-speed and low-power logic circuits [2]. We have reported RTD/HEMT PLL operates up to 1.4GHz and consumes 4.1mW [3]. Since it was assumed that device was a superior HEMT, 0.15μm gate InGaAs HEMT, i.e. the device used in the simulation was rather real, RTD/HEMT logic gates and the PLL showed optimistic results.

In this paper, in order to estimate the more realistic characteristics of RTD/HEMT logic gates using ordinary GaAs/AlGaAs HEMT in detail by using real device parameters extracted from measured values, we examine their characteristics and discuss about their application to functional circuits such as phase comparator (PC) and voltage controlled oscillator (VCO) used in PLL. In the RTD/HEMT logic gates, RTD acts as load device and HEMT as driver device. First, in order to show its effectiveness, comparison with conventional resistor-load or depletion-mode HEMT (D-HEMT) load direct-coupled FET logic (DCFL) configuration will be shown, especially in INVERTER and NAND representing combinational logic and in D-FF representing sequential logic. Next, PC and VCO characteristics will be described. The VCO consists of ring oscillator. In the VCO, new inverter configuration, inverter with voltage-controlled push-pull buffer, is used.

2. RTD/HEMT Primitive Logic Gates

Figure 1 shows a schematic device structure of RTD/HEMT inverter. RTD is integrated on the drain region of the HEMT. RTD can be integrated on the HEMT by almost the same fabrication technology as for pure HEMT. While conventional D-HEMT load DCFL gates occupies the area of about "$S_{D-HEMT} + S_{E-HEMT}$" at least, where S_{D-HEMT} and S_{E-HEMT} are D-HEMT and E-HEMT transistor size, respectively, RTD/HEMT requires only S_{E-HEMT}. Hence logic gate size can be smaller than conventional ones.

In general, logic gates using HEMT are ratioed logic, a careful design of transistor sizes or impedances is required to obtain a workable gate. **Figure 2** shows current-voltage curves of inverter for 1.0μm^2 RTD and 0.3μm gate length and 20μm wide GaAs/AlGaAs HEMT and logic level definitions. The RTD represents the load line. Resistor and D-HEMT load lines are also shown in the figure for comparison.

Like CMOS logic gates, RTD/HEMT gate is in-

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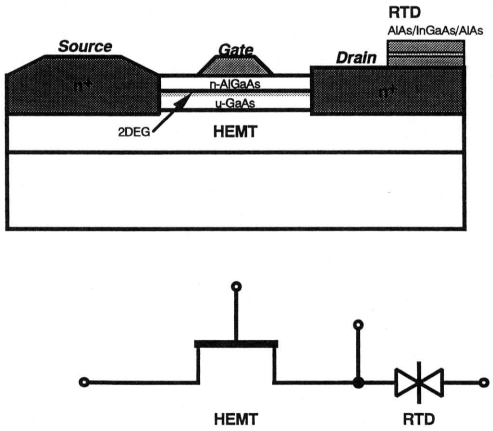
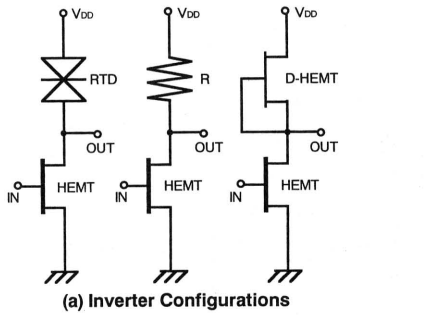
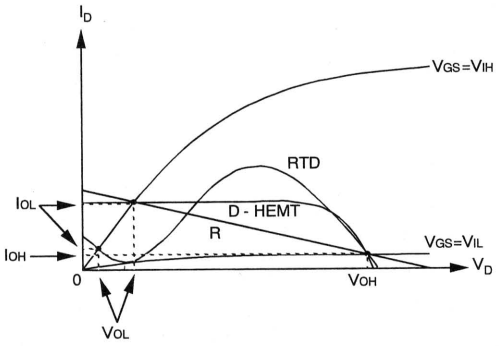


Fig.1 Device structure of an RTD/HEMT inverter, and its circuit schematic.



(a) Inverter Configurations



(b) Current-Voltage Curves

Fig.2 (a)Inverter configurations, (b)current-voltage curves for $1.0\mu m^2$ RTD and $0.3\mu m$ gate length and $20\mu m$ wide GaAs/AlGaAs HEMT.

verting, it means that RTD/HEMT gates implement functions such as NAND and NOR and are not possible to implement non-inverting functions such as AND and OR in one stage.

Figure 3 shows a circuit schematic of 3-input NAND gate. Three enhancement HEMTs (E-HEMT) in series form pull-down network (PDN), and RTD is pull-up network (PUN). The size of E-HEMT is three times larger than those of inverter to reduce serial resistance.

Figure 4 shows a circuit schematic of edge-trigger type D-FF with preset and clear. This D-

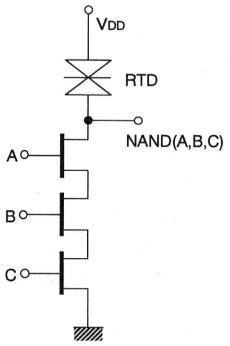


Fig.3 3-input NAND circuit schematic.

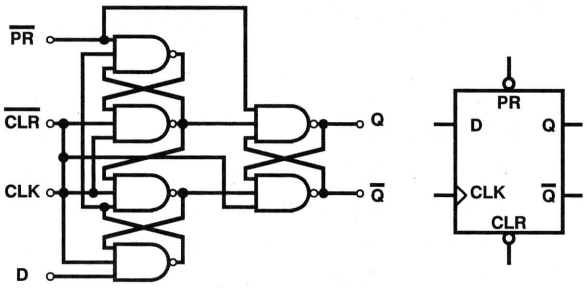


Fig.4 D-FF circuit schematic.

FF consists of six 3-input NAND gates mentioned above.

3. Logic Gates Characteristics

In this section, device models and simulation method are presented first, and next, the simulated characteristics of three primitive gates are described.

3.1 Device Models

RTD and HEMT device models are not usually implemeted in circuit simulators such as SPICE, hence such device models are required to simulate circuits. In this part, RTD and HEMT device models are described.

3.1.1 RTD

AlAs/InGaAs/AlAs RTD device [2] is used in the simulation. It consists of two 1.4nm-thick AlAs barriers and a 5.9nm-thick $In_{0.53}Ga_{0.47}As$ quantum well. Its peak current density J_P is $1.4 \times 10^5 A/cm^2$ and peak-to-valley current ratio (PVCR) is 12. The specific capacitance C_S is about $1.5fF/\mu m^2$ at the peak voltage. The equivalent circuit of the RTD is the Gering model [4] as shown in **Fig. 5**. C_S is the specific capacitance of RTD. Current source is expressed as polynomial function. And in the simulations, 7-th order polynomial function of V_D is used.

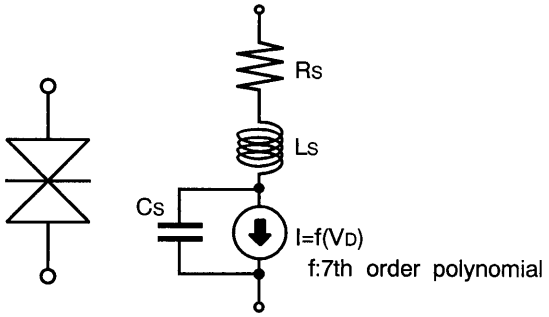


Fig.5 Equivalent circuit of RTD.

Table 1 Device Parameters

Parameter	Value
Design Rule	0.3μm
Driver Device	
HEMT ($L_g \times W$)	$0.3\mu m \times 20\mu m$
Threshold Voltage	+0.1V
Load Device	
RTD Area	$1\mu m^2$
Resistor	3.2KΩ
D-HEMT ($L_g \times W$)	$0.3\mu m \times 1\mu m$
D-HEMT Threshold Voltage	−1.045V

3.1.2 HEMT

The HEMT I-V characteristics used in the simulations are modeled by the PSpice level-2 MESFET model [7] and DC parameters are extracted from 0.3μ gate, 200μm wide GaAs/AlGaAs depletion-mode (D)-HEMT [5] DC measurements [6]. Small-signal equivalent circuit parameters are obtained from D-HEMT [5]. Since this HEMT is a discrete component, it shows relatively large capacitance. Though usually MESFET model is not suitable for HEMT, in the case of RTD/HEMT gates, HEMT operates in the almost linear region and the beginning region of the saturation. And power supply is less than 1V. Therefore MESFET model can be applied to HEMT less than 1V of drain voltage within about 4% error. It is assumed that E-HEMT has the same characteristics as D-HEMT except threshold voltage.

3.2 Simulation Method

We used PSpice [7], an analog/digital mixed circuit simulator. Power supply voltage is set at 0.7V. And interconnect wiring capacitance is assumed 10fF. **Table 1** shows device parameters used in the simulation.

3.3 Simulation Results

In order to compare three inverter configurations qualitatively, all inverters are designed so as to consume the same static power, namely I_{OL} for each inverter are almost the same, about 0.2mA. The static power consumptions are about 150μW for all inverters.

Figure 6 show the simulation results of inverters. On RTD/HEMT inverter, voltage transfer characteristics (VTC) show hysteresis. This inverter is Schmitt-trigger type inverter.

t_{pdHL} of RTD/HEMT inverter is not smaller than those of resistor load and D-HEMT load, but t_{pdLH} is about 3 times faster than those of them. While t_{pdHL} is dominated by the current drivability of the pull-down transistor, t_{pdLH} is dominated by that of the load device. In the RTD/HEMT inverter, large current through the RTD charges the load capacitance, when the driver HEMT is turning-on (V_{in} is going "High"). This causes t_{pdHL} longer than those of resistor and D-HEMT loads. On the other hand, when V_{IN} is going "Low", much more current due to NRD charges load capacitance than resistor and D-HEMT. Therefore t_{pdLH} is much shorter.

Noise margin, NM_H of RTD/HEMT inverter is about half of those of the counterparts, and NM_L is three times larger due to NDR characteristics. As mentioned above, VTC of RTD/HEMT inverter shows hysteresis, and hence both NM_H and NM_L are relatively large.

The simulation results on 3-input NAND show that rising time t_{pdLH} is much longer than falling time t_{pdHL}, and that t_{pdLH} are 4 to 7 times larger than those of inverters.

Figure 8 shows the simulation results on D-FF. RTD/HEMT D-FF is faster than those of resistor and D-HEMT load. But the dead zone is quite large, about 200ps. This is because that D-FF consists of two-stage NAND gates. In order to obtain faster D-FF, it is required that the delay time of NAND gate should be shorter.

Comparison results with previous work [8] show that both t_{pdHL} and t_{pdLH} are a little larger, and that driving capability is low due to the inferior HEMT characteristics. These results are summarized in **Table 2**.

4. Functional Circuits

PLL is a key component for clock recovery and clock generation. It should integrate both analog and digital circuits, i.e., so-called mixed signal circuits, on one chip. PC is pure digital circuit,

Table 2 Comparison Results of Three Inverter Configurations

Inverter

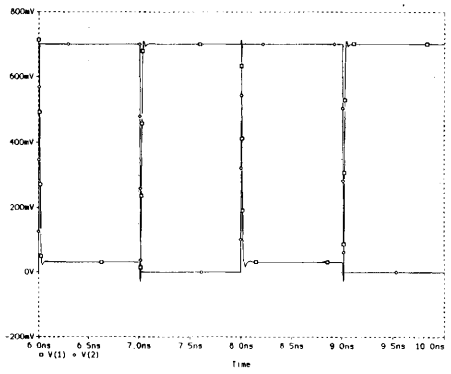
	RTD/HMET	Resistor Load	D-HEMT Load
t_{pdHL}[ps]	9.8	5.6	5.7
t_{pdLH}[ps]	15.6	51.1	49.6
NM_L[mV]	246.3	75.6	82.3
NM_H[mV]	189.4	445.0	440.0

3-Input NAND

	RTD/HMET	Resistor Load	D-HEMT Load
t_{pdHL}[ps]	22.4	18.8	18.7
t_{pdLH}[ps]	115.8	202.4	376.3

D-FF

	RTD/HMET	Resistor Load	D-HEMT Load
Toggle Freq. [GHz]	1.9	1.02	0.66



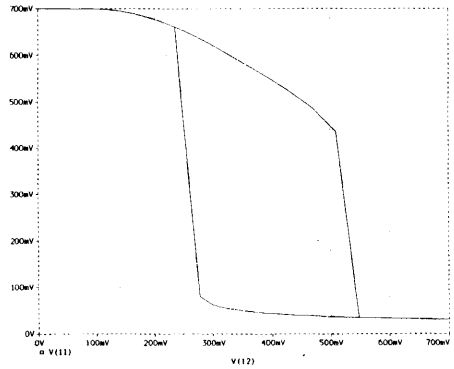


Fig.6 Characteristics of inverters, (a)transient analysis result (b)voltage transfer characteristics (VTC).

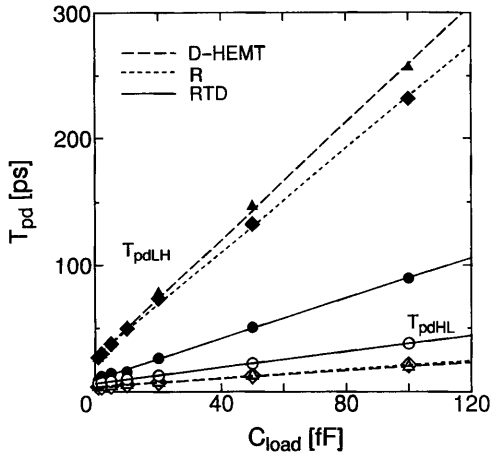


Fig.7 Load capacitance characteristics.

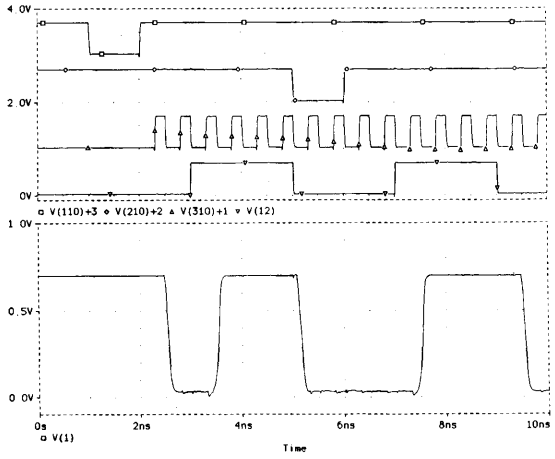


Fig.8 Characteristics of RTD/HEMT D-FF.

and VCO is analog one. So PLL is a good example for functional circuits. This section describes functional circuits such as PC and VCO used in PLL. VCO consists of ring oscillator. In the VCO, new inverter configuration, inverter with voltage-controlled push-pull buffer, is used.

4.1 Phase Comparator

PC compares the phase difference between input and VCO signals. **Figure 9** shows a circuit schematic of phase comparator (PC) and its timing chart. The PC consists of four D-FFs with clear

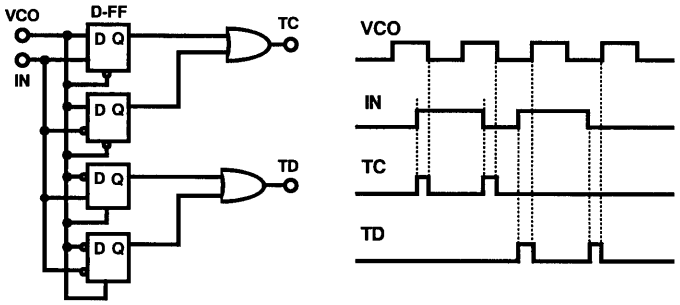


Fig.9 Phase comparator circuit and timing chart.

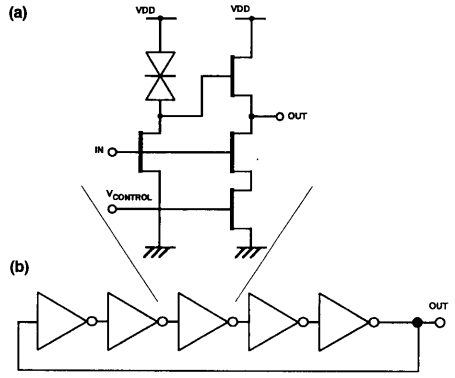


Fig.10 VCO schematic, (a)voltage-controlled inverter, (b)5-stage ring oscillator.

and two NORs. If the VCO signal leads the input signal, PC outputs T_D "DOWN" signal. On the contrary, if the VCO signal lags the input signal, PC outputs T_U, "UP" signal.

4.2 Voltage Controlled Oscillator

Figure 10 shows a voltage-controlled oscillator (VCO) schematic. The VCO consists of 5-stage voltage-controlled inverter (VCI) forming ring-oscillator. The VCI is an inverter with push-pull buffer in which discharging current hence delay time is controllable by the control voltage, V_{cntl}. Advantage of this circuit is that the buffer stage can be designed independent of inverter stage. Disadvantage is the threshold voltage loss of the logic swing. But this circuit is superior to variable-resistance current-controlled inverter [8] for wide variable frequency range. To vary oscillation frequency of the ring-oscillator, delay time of inverters have to be altered. In the CMOS ring-oscillator, starved VCO is usually used in which both charging and discharging current are controlled by the current mirror circuit. Since charging and discharging currents are almost the same, resulting rising and falling time are also same. RTD/HEMT inverter shows an asymmetric propagation characteristics, namely the falling time t_{pdHL} is shorter than the rising time t_{pdLH}. Therefore controlling of the discharge current is sufficient to vary the delay time of the inverter.

4.3 Simulation Results

Figure 11 shows simulation results on the PC. This result is for 500MHz of VCO signal, and 250MHz of input signal. It consumes about 3.5mW. Due to the dead zone of D-FF, the PC cannot detect the phase difference less than 200ps.

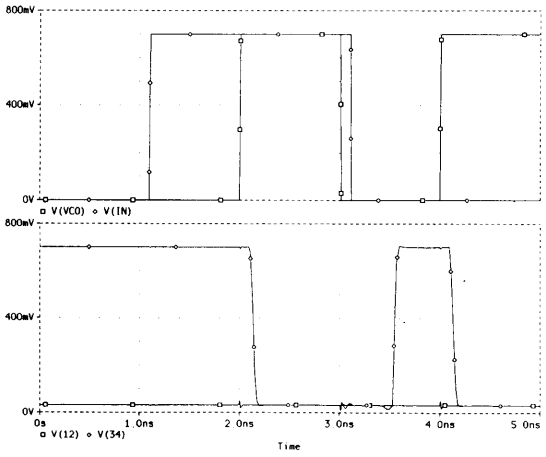


Fig.11 Result of the PC simulation.

Figure 12 shows results of the 5-stage ring oscillator VCO. The RTD/HEMT VCO dissipates about 1.4mW at 2GHz. Variable frequency range is from 1.9 to 2.3GHz. VCO gain, ratio of variable frequency range to control voltage V_{cntl}, is about 1GHz/1V. And variable frequency region is about $f_0 \pm 95\%$. VCOs of resistor and D-HEMT loads oscillates at 0.6 to 1.2GHz range and 0.6 to 1.3GHz range, respectively. VCO of the previous work [8], which is 3-stage ring oscillator, oscillates from 3.1GHz to 3.7GHz when control voltage is varied from 0.3 to 0.8V. Variable frequency region is about $f_0 \pm 88\%$. Therefore VCO which adopts new inverter configuration is about 7% faster than our earlier work [8].

It is expected that PLL consisting of these PC and VCO would operate up to 500MHz, and dissipate less than 10mW. The maximum operating frequency is limited by the PC perfomance.

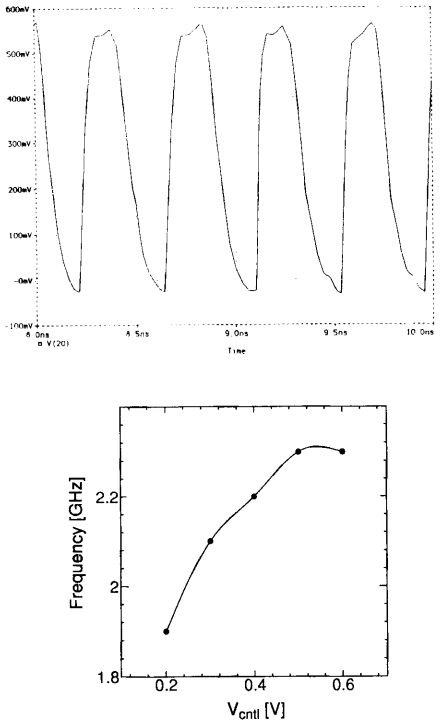


Fig.12 Results of the VCO simulation, (a)oscillator waveform and (b)frequency of VCO as a function of the control voltage V_{cntl}.

5. Conclusion

RTD/HEMT logic circuits have been examined in this paper. Fundamental characteristics of logic gates were examined and compared with resistor and D-HEMT load inverters. Comparison results with resistor and D-HEMT load DCFL logic show RTD/HEMT is faster than the latter two configurations. This is due to NDR characteristics of RTD. And also it consumes less power. And application to functional circuits such as PC and VCO used in PLL have also been described. It is expected that RTD/HEMT PLL would operate up to 500MHz at 0.7V power supply and consume less 10mW.

Acknowledgments

This work is partially supported by Grant-In-Aid for Scientific Research from The Ministry of Education, Science, Sports and Culture.

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