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The Evaluation of Temporary Degradation in Quarter Micron MOSFET by Hydrogen Passivation of Boron

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Abstract: This paper evaluates the outermost case of temporary MOSFET's characteristics degradation by hydrogen passivation of B (Boron) in low temperature process. A 1 μm p-MOSFET showed slight increase of drain resistance and about 40 % reduction of sheet resistance, experimentally. The simulation of 0.25 μm MOSFET's shows the channel length increase of more than 20 %, drain resistance increase about 40 %, as the results of 90 % passivation of dopant in lightly doped source and drain (LDD). To reduce the hydrogen passivation effects, the shortest LDD structure or heavily doped drain are required, and lower substrate impurity concentration must be chosen as far as possible to suppress the variation of threshold voltage. For the deep-submicron channel devices, however, it's difficult to make the sufficiently low resistive contact resistance.

Keywords: LDD MOSFET, Hydrogen passivation of Boron, Contact resistance, Reliability, Plasma cleaning

1. Introduction

Hydrogen atom passivates the electrical activity of many kinds of impurities in silicon such as donor impurities[1], acceptor impurities[1], heavy metals[2),3)], micro-defects[4], surface states[5] and so on. The passivation of heavy metal atoms and surface states causing deep levels might reduce generation recombination current which induce leak current in semiconductor devices, and might improve the holding time of dynamic circuits. The hydrogen passivation has also been used as hydrogen plasma annealing for TFT's for liquid crystal display on glass substrates, which need a very low temperature process, for improving electrical characteristics at the grain boundary in the channel between source and drain[7]. However, for the short channel MOSFET's on mono-crystalline silicon with high performance, the passivation of donor and acceptor impurities has a possibility to degrade the electrical characteristics of semiconductor devices such as threshold voltage, ohmic contacts, series resistance in the source and drain diffused layers, wiring resistance in poly-Si and diffused layers, and so on. Those should induce the designed operating point imbalance in the circuit, increase of power consumption by leak current, and degradation of the circuits switching speed, too.

We are studying the ultra low temperature, dry cleaning process for Si VLSI on MOS technology using the hydrogen radical[8], especially for multi-layer wiring process steps which require the low process temperature not to change the impurity profiles in very shallow junction depth. In this hydrogen plasma cleaning, however, the dopants passivation temporarily affects the device characteristics before the alloying step at the end of the current device manufacturing process. The electrical device characteristics is checked on the way of process, sometimes, and it is evaluated whether the device should be passed to next steps or not. Furthermore, the ultra low temperature process will be necessary to be used for the very tiny devices having atomic scale size. In these case, the electrical passivation of the dopants may remain in the electrical characteristics of the devices.

We reported that hydrogen penetrates into SiO_2, easily. On the other hands, poly-silicon, CVD Si_3N_4 and sputtered aluminum film protected the hydrogen penetration through the films[10]. Therefore, if we could use the bi-layer structure with SiO_2 ad Si_3N_4, we can eliminate the hydrogen passivation effects. However, we don't choose the structures in all cases. In this paper, we discuss another approach to eliminate the hydrogen passivation of dopants by optimization of the geometrical MOSFET structures. At first we summarize our experiential results about 1 μm p-MOSFET characteristics variation after the hydrogen passivation[9]. Then, using this experimental results, we speculate the outermost case of the temporary variation by the hydrogen passivation for two kinds of MOSFET's, conventional

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LDD devices and LDD devices having low channel impurity, with the process simulator, PROMIS, and the device simulator, MINIMOS, which are developed in TUV[11]. Channel length variation, subthreshold characteristics, I_{ds}-V_{ds} characteristics, and contact resistance change are evaluated by the device simulator, and the best structures for the quarter micron size MOSFET's which aren't affected by the hydrogen passivation are discussed.

2. Experimental Evidence for Simulation

The hydrogen passivation was done in the diffused hydrogen plasma without ion bombardment, after aluminum wiring process[9]. Langmuir probe measurement results showed the very low ion currents and a little potential difference less than 1 V between plasma and wafer. In this plasma apparatus, the hydrogen ion doesn't inpinge onto the wafer surface, practically. Fig.1 compares the I_{ds}-V_{ds} characteristics of p-MOSFET's with 40 nm gate oxide thickness which was fabricated with p^+-poly gate process for 1.0 μm channel length MOS, before and after the hydrogen plasma treatment. About 5 % reduction of drain conductance was observed at saturation region. The flatband voltage shift of MOS Diode fabricated in the same chip showed less than 30 mV. Table-1 shows the variation of active acceptor concentration in source and drain observed by the sheet resistance measurements with 4 terminal test structures, contact resistance measurements with contact chains and p^+-n junction capacitance under reverse bias. These three methods monitor the acceptor concentration at different points in depth. Contact resistance depends on the acceptor concentration at metal-semiconductor interface, sheet resistance gives mean value of the concentration in the diffused layer, and p^+-n junction capacitance represents the concentration in depletion layer edge. About 20 % to 80 % reduction of the electrically active acceptor impurity concentration was observed in the diffused layer at source and drain. Therefore, the drain conductance reduction in Fig.1 is speculated due to the increase of source and drain resistance after the hydrogen plasma treatment. In the following sections, the outermost case of 90% reduction of electrically active B will be evaluated.

3. Simulated Device Structures.

For n-channel devices, two kinds of MOSFET's were evaluated. One is a conventional LDD MOSFET, and the other is an LDD MOSFET with low impurity epitaxial layer under the gate. Fig.2 illustrates the cross-

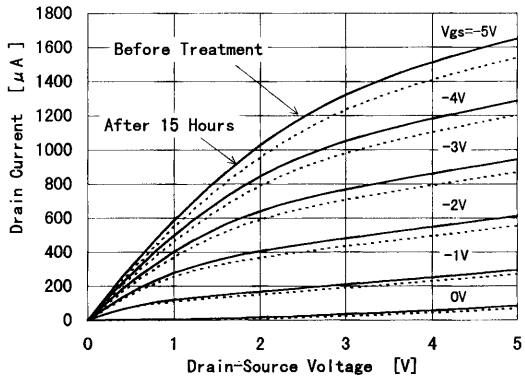

Fig.1 I_{ds}-V_{ds} characteristics of 1 μm p-MOSFET with L=1 μm, W=10 μm, which was fabricated with p^+-poly gate process before and after hydrogen plasma treatment.

Table-1 Electrically active acceptor concentration estimated with contact resistance, sheet resistance, and p^+-n diode capacitance, before and after H_2 plasma treatment.

Method	Before H_2 Plasma	After H_2 Plasma	Reduction
Contact Resistance	$/cm^3$ 3.23×10^{19}	$/cm^3$ 2.5×10^{19}	% 21
Sheet Resistance	$/cm^3$ 2.3×10^{19}	$/cm^3$ 1.3×10^{19}	% 43
p^+-n Diode Capacitance	$/cm^3$ 9.1×10^{18}	$/cm^3$ 1.86×10^{18}	% 78

sections of two 0.25 μm n-MOSFET's with gate oxide of 8 nm in thickness and LDD structure of 0.05 μm in depth and 0.2 μm in length. The highest donor concentration at the LDD diffusion layers is 2×10^{19} $/cm^3$. The junction depth under the metal contact is 0.1 μm, the highest impurity concentration is 2×10^{20} $/cm^3$. In this design, the dose and the acceleration energy of As ion implantation for LDD region, and source and drain are chosen as 1×10^{15} $/cm^2$, 20 keV and 1×10^{16} $/cm^2$, 20 keV, respectively. And the annealing temperature and time are 1000 °C, 2 min, respectively. The metallurgical channel length is designed as 0.25 μm before the hydrogen passivation. For the low impurity channel device shown in Fig.2(b), the abrupt doping profile of B in the substrate is assumed. The doping concentration and the thickness of the low impurity epitaxial layer on 1×10^{17} $/cm^3$ B-doped substrate are 1×10^{14} $/cm^3$ and 0.1 μm thick, respectively.

The simulated p-MOSFET's also have 8 nm gate oxide, 0.25 μm metallurgical channel length, the LDD structure of 0.1 μm length and 0.035 μm depth, and acceptor concentration of 2.1×10^{18} $/cm^3$ at the surface which was made by the ion implantation of 5×10^{15} $/cm^2$ B, 12 keV. The junction depth under the metal contact

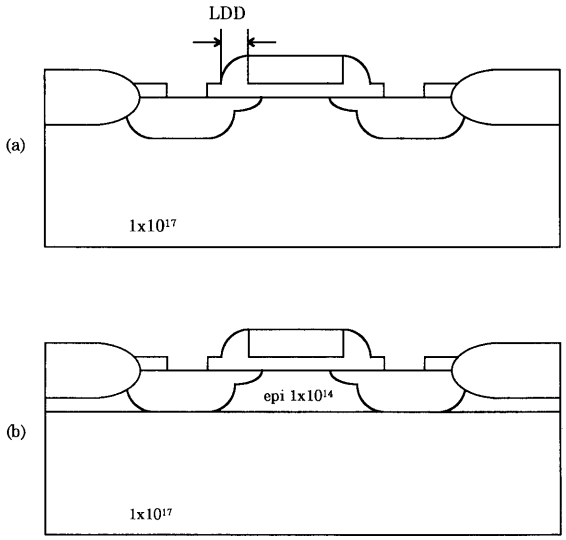

Fig.2 Simulated 0.25 μm LDD MOSFET's structures. (a) is the conventional LDD device and (b) is the fabricated one on high resistive epitaxial layer of 0.1 μm thick.

was 0.11 μm, the impurity concentration just under the interface between metal and silicon was 5.7×10^{19} /cm^3 using the 2×10^{16} /cm^2, 15 keV B ion implantation. The donor concentration in the substrate is assumed as 1×10^{17} /cm^3.

4. Simulation Results and Discussions

4.1 Channel Length Variation by Passivation of LDD Diffused Layer

The metallurgical channel length might be changed by passivation of dopant in source and drain. Fig.3 shows a simulated result of metallurgical channel length variation for the conventional LDD structured p-MOSFET's with about 0.25 μm channel length, after the passivation. After the heavy hydrogen passivation of B over 90 %, the channel length variation becomes an order of more than 20 %. For the MOSFET with 0.1 μm sidewall spacer, heavily doped B at source and drain under the metal contact to get good ohmic contact penetrates through the LDD region into channel region, and its effective channel length becomes shorter than the thicker sidewall devices when B is passivated at the same degree. Short channel effect permitting the shortest LDD length must be chosen to avoid the reduction of channel length by the hydrogen passivation.

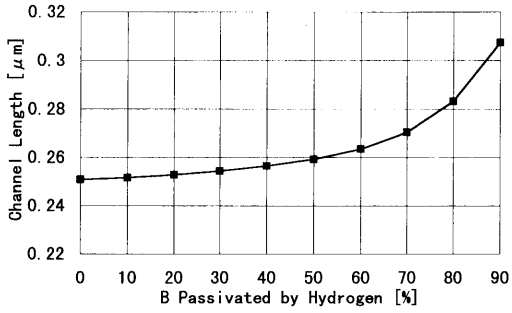

Fig.3 Simulated channel length variation of conventional LDD p-MOSFET's with about 0.25 μm channel length after the hydrogen passivation.

4.2 Channel Conductance Variation

Fig.4 shows the simulated I_{ds}-V_{ds} characteristics of MOSFET's before and after the hydrogen plasma treatment. Fig.4(a) is before the treatment, and (b) is after 90 % passivation of B. The metallurgical channel length is 0.25 μm before the hydrogen passivation. In all region, the reduction of the drain conductance is observed. Fig.5 shows the DC channel resistance V_{ds}/I_{ds} variation of the MOSFET's with different LDD length as a parameter of the passivated B concentration. The device having larger LDD length gives larger variation of the conductance. These characteristics changes include the variation of the parasitic diffusion layer resistance appears in the heavily doped drain and source, which exists between contact edge and LDD edge as shown in Fig.2. However, the parasitic resistance hardly affects the channel conductance, because the length from the contact to the LDD edge is the same order with LDD sidewall size but the sheet resistance are usually less than 5% of LDD region. Therefore, the variation shown in Fig.4 and Fig.5 depend on the resistance variation of LDD region which has rather lower impurity concentration than contact region. Considering drain conductance, LDD length must be as short as possible to reduce the effect of the hydrogen passivation.

4.3 Threshold Voltage Shift

The threshold voltage of n-MOSFET is affected rather than p-MOSFET by the hydrogen passivation of substrate dopant, B. n-MOSFET is made on B doped substrate, usually. Fig.6 shows the gate threshold voltage shift of n-MOSFET's as a function of hydrogen passivated B concentration.

The conventional MOSFET shows the larger threshold voltage shift rather than the MOSFET made on high resistive epitaxial layer. In both cases, however, the passivated B increasing the threshold voltages shift toward

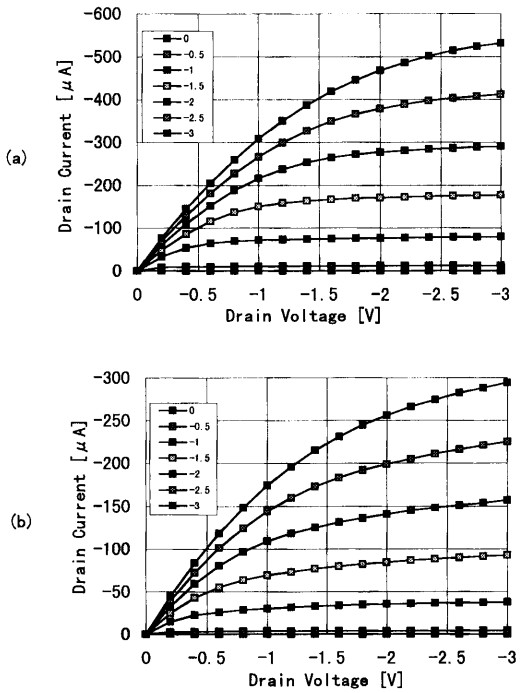

Fig.4 Simulated I_{ds}-V_{ds} characteristics of 0.25 μm p-MOSFET's. (a) is before passivation of B, and (b) is after 90 % passivation.

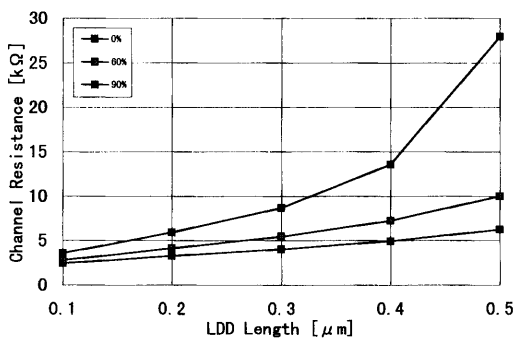

Fig.5 Simulated channel resistance variation depends on LDD length as a parameter of hydrogen passivation, at V_{ds}=3 V, and V_{gs}=3 V.

normally-on state. Fig.7 shows the subthreshold characteristics change by the passivation. The subthreshold coefficient hardly changed as shown in Fig.7. The MOSFET with lower channel impurity layer (dashed line in Fig.7) shows less dependence on the hydrogen passivation. This is because the most part of depletion layer expands into the low impurity concentration layer.

Another origin of threshold voltage shift by the impurity passivation is due to the source to substrate bias change induced by the voltage drop in the source LDD resistance when source current flows. This effect appears in p-MOSFET with B-doped source. However, this voltage drop is negligibly small, because the LDD

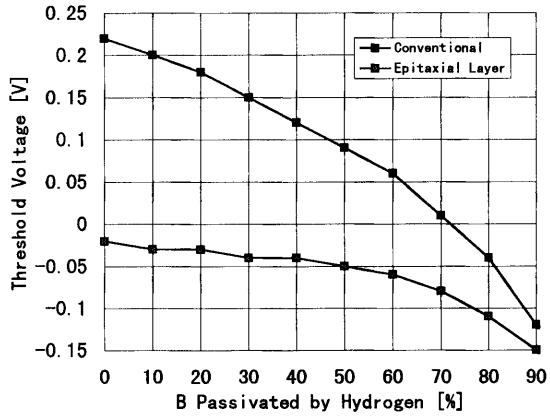

Fig.6 Simulated threshold voltage variation of n-MOSFET's as a function of B concentration passivated by hydrogen in %. Effective channel length is 0.25 μm and channel width is 2.5 μm. Threshold voltage is defined at I_{ds}=1 × 10^{-7} A/μm.

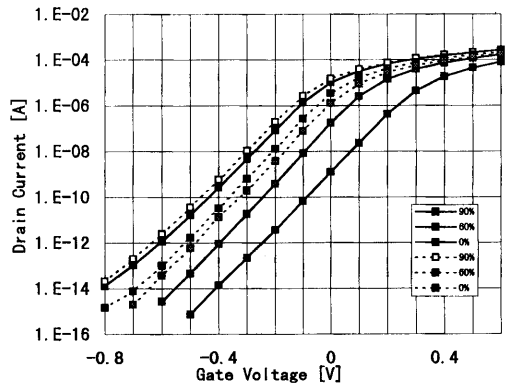

Fig.7 Simulated subthreshold characteristics variation as a parameter of hydrogen passivation of B in % for the two devices. Dashed lines are for the MOSFET's on epitaxial layer, and solid lines are for the conventional devices. FET's sizes are same as the devices in Fig.6.

resistance variation by the passivation is tens ohm at most, and the threshold voltage is defined at very low source current of 1 × 10^{-7} A/μm.

4.4 Contact Resistance Variations

The experimental results listed in Table-1 show that the contact resistance variation before and after the passivation was relatively small. However, the contact resistance at metal to semiconductor interface strongly depends on the dopant concentration at the interface, nonlinearly. For the deep submicron contact hole, if the rather low specific contact resistance of the $10^{-7}\Omega/m^2$ is gotten, the contact resistance of FETs with the size less than quarter micron area becomes comparable order with channel resistance in on-state. The value isn't acceptable for high performance circuit. Furthermore,

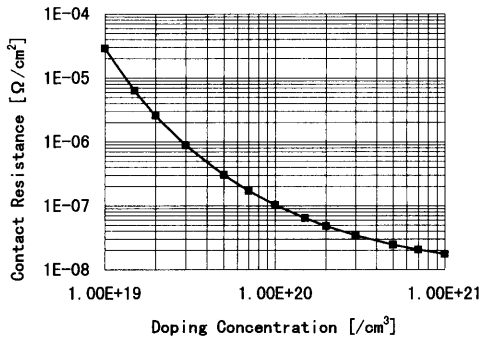

Fig.8 Contact resistance variation with B concentration. The absolute values are fitted the experimental value.

it's a very difficult work to make the heavily doped shallow p^+-n junction less than 0.1 μm at source and drain reagion because of high diffusivity of B. Therefore the deep submicron MOSFET must use improved structures instead of lightly doped p^+-n junction. In this section, contact resistance variation by hydrogen passivation is calculated with the following equation[12],

$$R_C \sim \exp\left(\frac{4\pi\sqrt{\varepsilon_S\varepsilon_0 m^*}\psi_B}{h\sqrt{N_a}}\right) \quad (1)$$

where ε_0 is the permittivity in vacuum, ε_S is the permittivity of Si, m^* is the effective mass of hole, ψ_B is the Schottky barrier height on p-type Si, h is the Plank constant, N_a is the acceptor concentration. In this calculation, N_a before hydrogen passivation is calculated with the device simulator according to the process parameter used practically in this experiment, and the absolute value of Rc is fitted to the experimental result before hydrogen plasma treatment. The barrier height ψ_B is chosen as 0.35 eV for aluminum to p^+-Si after the reference paper[12]. Fig.8 shows the result of the calculation. If electrically active B concentration at the interface reduced from 1×10^{20} /cm^3 to 1×10^{19} /cm^3, the resistance at quarter micron square contact changes from 160 Ω to 48 kΩ. It becomes comparable order with channel resistance in on-state.

It is difficult to design the very high acceptor concentration at the contact for the deep submicron LSI which requires very shallow junction depth as mentioned above. However, it requires acceptor concentration as high as possible to reduce the hydrogen passivation effect.

5. Conclusion

This paper evaluates the outermost case of temporary MOSFET's electrical characteristics degradation by hydrogen passivation of B. This effect remains in the devices after hydrogen plasma process at very low substrate temperature less than 200 °C which is expected to be used for manufacturing process of very tiny device and dry cleaning with hydrogen plasma, in future. Of course it is no problem in current LSI processes which accompany alloying step at rather high temperature at the end of the manufacturing process.

Several kinds of electrical test structures were made on B doped (100) Si and those were exposed in the diffused hydrogen plasma. The MOSFET with 1 μm channel length showed the slight reduction of the drain current after the hydrogen plasma treatment. 20 % to 80 % decrease of electrically active B were observed in the test structures of contact chains, sheet resistance, and reverse-biased p-n junction. The reason why the differences of the dopant quantity passivated among the test structures were observed has not been clarified, however, in the worst case the electrical passivation of B is possible to give a big problem in the circuit operation.

With a device simulator, the DC electrical characteristics was evaluated for two kinds of 0.25 μm channel length MOSFET's, one is conventional LDD device with higher substrate doping concentration, the other is LDD device with low channel impurity layer. Supposing the 90% passivation of dopant in source and drain region, the channel length increased by 23% in the conventional device. The passivation of dopant at LDD region also affects the drain resistance, it reduced the resistance by about 40 % at the saturated region after the 90 % passivation. Conventional LDD structure with highly doped substrate for decreasing short channel effects showed larger threshold-voltage shift, but devices made on low channel impurity substrate showed less threshold-voltage shift. The subthreshold coefficient hardly changed in the both devices.

To reduce the effect of hydrogen passivation, the shortest LDD length, the highly doped LDD region and the lower substrate impurity concentration must be chosen as far as possible. For the deep-submicron channel devices, however, it's difficult to keep the same sheet resistance as the longer channel devices at LDD region, especially for p-MOSFET because there are no dopants such as As for n-MOSFET, which show low diffusivity. Therefore, the novel FET structures such as self-aligned silicide source and drain without LDD region will be essential.

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References

1) Pearton, S.J., Corbett, J.W., and Shi, T.S., *Appl. Physics A* **43** (1987)153.
2) Sadoh, T., Nakashima, H., and Tsurushima, T., *J. Appl. Phys.* **72(2)** (1992)520.
3) Pearton, S.J., and Tavendale, A.J., *Phys. Rev. B* **26(12)** (1982)7105.
4) Brumi, M., Bisero, D., Touini, R., Ottaviani, G., and Bottini, R., *Phys. Rev. B* **49(8)** (1994)5291.
5) Cartier, E., Stathis, J.H., and Buchanan, D.A., *Appl. Phys. Lett.* **63(11)** (1993)1510.
6) Delfino, M., Salimian, S., Hodul, D., Ellingboe, A., and Tsai, W., *J. Appl. Phys.* **71(7)** (1992)1010.
7) Mimura, A., Konishi, N., Ono, K., Ohwada, J., Hosokawa, Y., Ono, Y.A., Suzuki, T., Miyata, K., and Kawakami, H., *IEEE Trans. Electron Devices* **36(2)** (1989)351.
8) Ramm, J., Beck, E., Zueger, A., Dommann, A., and Pixley, R.E., *Thin Solid Films* **228** (1993)23.
9) Kuroki, Y., and Tsukamoto, K., *Technical Report of IEICE* **SDM94-36**(1994-07)15, (in Japanese)
10) Tsukamoto, K., Iwasaki, S., Sadoh, T., and Kuroki Y., *Thin Solid Films* to be published.
11) Selberherr, S., Schütz, A., and Pötzl, H.W., *IEEE Trans. Electron Devices* **ED27(8)** (1980)1540.
12) Sze, S.M., *Physics of Semiconductor Devices, 2nd Edition, John Wiley & Sons, Inc.* (1981).