3次元実装FPGA用途向きの温度依存かつ消費電力指向型回路分割技術

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https://doi.org/10.15017/1470602

出版情報: Kyushu University, 2014, 博士（工学）, 課程博士
バージョン: published
権利関係: Fulltext available.
論文内容の要旨

In this era of deep sub-micron technologies for integrated circuits (ICs), applications demand aggressive decrement in the desired power budget, thus putting many challenges to the chip designers. Power becomes an ever-increasing concern due to the growing design complexity and the shrinking process technology. Designing for low power consumption demands power-efficient devices and good design practices to leverage the architectural features without compromising performance. It becomes necessary to understand the power consumption early in the design cycle to meet the desired power budget. Power estimation at an early stage of electronic design automation (EDA) flow is essential in order to handle the design issues much earlier.

Three-dimensional (3D) field-programmable gate array (FPGA) is one of the promising technologies which can lead to the reduction in delay, area and power. On the other side, 3D integration suffers from heat dissipation between the layers due the power consumed by various resources. Thermal issues are cited as critical concern in 3D integration which results in degradation of device performance. There is an absolute necessity to develop algorithms and software tools to exploit the advantages of the third dimension, and to solve the complex tasks associated with them.

This dissertation focuses on a temperature-dependent power-aware partitioning methodology for 3D FPGA based on the necessary metrics estimations. Following this, an application study for 3D FPGA is discussed as well by surveying a big data processing platform, features and recommendations. The main objective of the later discussion is to show the future prospects of 3D FPGA in real-time commercial world.

In details, this dissertation presents the methodology for distribution of power density among the layers of a 3D FPGA based on the thermal analysis performed during the distribution at the partitioning stage of design cycle. First, a methodology for estimation of required routing resources in 3D FPGA is proposed at the partitioning stage. Following this, a dynamic and leakage power estimation methodology is developed. The methodology also utilizes the thermal evaluation carried based on the power numbers. Next, a temperature-dependent power-aware partitioning algorithm is proposed and developed on top of the popular academic 3D place and route tool “Three-dimensional Placement and
Route’ (TPR). Solutions produced by the proposed algorithm suggests that there is a scope for achieving desired power density distribution across the layers well before the placement thus allowing the designer to take the decisions during the early stages of the design cycle to improve the device performance in terms of power and thermal behaviour. The proposed methodology can be applied early in the design cycle for reducing the design effort.

Following the above, a discussion is presented on big-data processing platform highlighting the growing role of FPGA. Recommended features and hardware systems are proposed based on the operations performed in big data processing. A close comparison of FPGA systems: 3D FPGA and multi-FPGA system is performed as well. The proposed study shows that FPGAs can play significant role in the development of future big data processing platforms.