Study of Orientation Rotation in Rapid-Melting Growth of Ge-on-Insulator

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Growth of Ge-on-Insulator

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Chapter 1

Introduction

This chapter presents the motivation and background of this research work on the development of orientation stabilized nano-structured Ge-on-insulator (GOI) by rapid melting growth (RMG) process. The technology trend in semiconductor device development leading to the renewed interest in Ge has been discussed. The limitation of current Si based complementary metal-oxide-semiconductor (CMOS) devices and the possible breakthrough by Ge-on-insulator structures are also discussed. A comparison of the rapid melting growth technique with other GOI growth techniques and the limitations of the RMG process are presented. The chapter is concluded by outlining the purpose of this work and the organization of this dissertation.

1.1 Motivation

The first bipolar transistor was built with germanium in 1947. Germanium dominated the first decade of semiconductor electronics before giving away to Silicon. Silicon has been the dominant semiconductor material in the field of electronics for nearly five decades now. Since the inception of Si device integration technologies in the 1960s there has been a continuous improvement in the processing
power of integrated electronics. For most of this time, the advancement in integration has closely followed Moore’s law,\(^1,\,^2\) which stated that the number of components in integrated circuits will double every 1.8 years. The trend is illustrated in Fig 1.1.\(^3\)

The pursuit of higher processing power has pushed integration to the atomic scale. Today, it is possible to fabricate a Si based processor containing billions of transistors with fabricated with 22 nm lithographic process while the processing power has increased over a million fold from what it was four decades ago.\(^4\)

However, the increased difficulty in maintaining electrostatic control in extremely scaled Si transistors has made it difficult to keep up with Moore’s law. With the current trend in Si scaling based CMOS processing technology, the

Fig. 1.1 The trend of semiconductor device count per chip and feature size.\(^3\)
improvement in processing power is projected to slow down significantly by 2020. Under these circumstances, it has become essential to develop technology in which further performance improvement is possible without extreme scaling. This is where Ge comes in.

1.2 The Comeback of Germanium

To break through the scaling limit of Si and continue the performance improvement, it has become necessary to develop alternative materials. The integration of high mobility germanium transistors with the current Si CMOS process is a promising technique for this purpose.

In this connection, let’s take a brief look at the history of germanium in electronics. Although the first decade of semiconductor electronics was dominated by germanium, it gave away to Si by the late 1950s with the advent of SiO₂ surface passivated planer process for device integration. Despite the higher mobility and low voltage operation of Ge devices, the transition to Si was the obvious choice because neither mobility nor operating voltage was the first priority. The thermally grown SiO₂ provided an excellent quality interface thereby improving the electrical characteristics of devices.[5] Early attempts to form oxide passivation of germanium surface were mostly unsuccessful. GeO₂ as the counterpart of SiO₂ was found to be thermally unstable and highly water soluble. Alternative passivation techniques for germanium were not investigated as the focus of research shifted to Si for the most part. Consequently a germanium based VLSI was never developed and germanium remained in the fabrication of discrete, mostly optoelectronic, devices.
Intensive research has been undertaken since the late 1990s in order to develop high quality gate stack in germanium metal-oxide-semiconductor (MOS) transistors. The development of ZrO$_2$ and HfO$_2$ based high-$k$ dielectrics opened up the possibility to achieve high quality Ge gate stacks.$^{[6]}$ Further development demonstrated that SiO$_2$/GeO$_2$ bi-layer passivation technique can produce excellent quality Ge gate stacks, achieving the low interface density of states ($D_{it}$) of $2.5 \times 10^{11}$ cm$^{-2}$ eV$^{-1}$. $^{[7]}$

However, a complete transition to Ge based fabrication process is not expected in the near future for several reasons. In addition to the less availability and higher cost of Ge wafers, it is also not feasible to effect a sudden transition from the ubiquitously established Si processing industry.$^{[8]}$ It is considered that the best course of action is the integration of Ge in the Si processing platform to reap the benefits of its high mobility. This leads to the development of the Ge-on-insulator (GOI) structure. In addition to improving transistor performance by reducing parasitic capacitances and leakage currents, the GOI structure can make it possible to achieve heterogeneous integration of multifunctional materials, for example, GaAs for optical and Fe$_3$Si for spintronic devices.

1.3 Necessity of High Mobility Channel in Nanoscale MOSFETs

The amazing increase in the processing power of microprocessors has been possible mostly by aggressive scaling of metal-oxide-semiconductor field effect transistors (MOSFETs). The calculated historical intrinsic FET switching delay time vs. gate length in the last twenty years is shown in Fig. 1.2.$^{[9]}$ Down to about 0.5 $\mu$m
gate length, the gate delay \((CV/I)\) was reduced by continuous increase in drive current \((I)\). The implementation of high-k dielectrics made it possible to push scaling down to few tens of nanometers. Recent development of gate control has made it possible to fabricate 14 nm MOSFET nodes in Si. At this rate of scaling, Si will soon reach a physical limit, where material characteristics become untenable for maintaining device operation. Consequently, research interest has been renewed in high mobility materials like germanium (Ge). Below is a brief description of how higher mobility can improve device performance in the scaling limit.

The carrier transport mechanism in nano-scaled MOSFETs has been described by a quasi-ballistic model by Lundstrom et. al.\(^{10-12}\) According to this model the drain current in saturation is given by the equation: 

\[
I_D = qN_{inv}^{source}v_{inv}'(1-r)/(1+r) = 
\]

Fig. 1.2  Calculated historical intrinsic FET switching delay time and gate length.\(^9\)
$I_{BL}(1-r)/(1+r)$; where $v_{inj}$ is the average thermal injection velocity at the virtual source (VS), $r$ is the back-scattering coefficient, and $I_{BL}$ is the ballistic limit of the drain current. The virtual source is defined as the peak of the potential barrier between the source and the channel, as illustrated in Fig. 1.3. The injection velocity is related to carrier effective mass by $v_{inj} = \sqrt{(2K_BT/\pi m^*)}$, thus indicating the possibility of maximizing $I_D$ by using material with lower carrier effective mass, $m^*$. The back-scattering coefficient, $r$, is related to both channel length and carrier mobility as $r = L_{KT}/(L_{KT} + \lambda \mu)$. The term $L_{KT}$ is a fraction of the channel length determined by the drain-source voltage ($V_{DS}$). For $V_{DS} >> K_BT$, $L_{KT}$ is a very small

![Diagram of virtual source](image)

Fig. 1.3 Illustration of the virtual source (VS) position in the channel.
fraction of the channel length. Therefore, $\lambda_{\mu}$ becomes the primary factor in determining the backscatter coefficient. Now, the carrier mean-free path $\lambda_{\mu}$ is directly proportional to the low-field mobility $\mu_{\text{eff}}$. Thus that larger the value of $\mu_{\text{eff}}$ is, the closer the MOSFET operates to the ballistic limit. Therefore, implementation of high mobility material can be seen to directly improve device performance.

![Diagram of Long Channel MOSFET and Short Channel MOSFET](image)

Fig. 1.4  Electron potential energy profile along the channel length of a long channel (a) and a short channel transistor (b).

### 1.4 Short Channel Effects in Nano-Scaled MOSFETs

In addition to implementing germanium for high mobility transistor channels, new device architecture is also necessary for the continuation of Moore’s law. The amazing increase in the processing power of microprocessors has been possible mostly by aggressive scaling of transistor channels as the switching delay is inversely proportional to the channel length. The transistor feature size is pushing 14
The ITRS roadmap predicts feature size nearing 10 nm by 2020. Scaling down the transistor channel has also given rise to difficult technological challenges.

One of the challenges is the short channel effect, which has been a problem since the channel length was scaled down below 100 nm. The short channel effect summarizes a range of effects that makes it increasingly hard for the gate voltage to pinch off the channel current as the drain gets closer to the source. The situation is illustrated in terms of the electron potential energy profiles along the length of a long and short channel MOSFET in Fig. 1.4. The result is an increase in the subthreshold leakage current and a corresponding increase in the subthreshold power dissipation.

Fig. 1.5  Trend in active power density and subthreshold power density with decreasing gate length.[13]
as the channel length gets shorter. The effect is illustrated in terms of the trend in active and subthreshold power dissipation for shrinking Si channel length in Fig. 1.5.[13] The extrapolation shows a crossover of the two power dissipation curves below 20 nm channel length, which means a complete breakdown of transistor operation.

1.5 The Semiconductor-on-Insulator (SOI) Channel Structure

An improved device architecture called the semiconductor-on-insulator (SOI) has been proposed to improve electrostatic control over extremely scaled transistor channels. The work presented in this dissertation is mainly focused on this architecture. This section describes the benefits of the SOI architecture.

The SOI channel can improve the gate electrostatic control over the channel and significantly reduce the short channel effects. The concept is illustrated in Fig. 1.6. In a conventional CMOS transistor, the channel is defined by the source and drain depletion zones, which are dependent on doping level and gate voltage. This makes it vulnerable to the short channel effects. In a semiconductor-on-insulator structure, the channel is defined by physical boundaries rather than doping levels, thereby improving gate electrostatic control over the channel and dramatically reduce leakage. There are two SOI channel models – partially depleted (PD) SOI and the fully depleted (FD) SOI. The PD-SOI channel is relatively thicker (50 – 100 nm for Si) and only partial depletion of the channel is achieved.[14] However, some advantages over bulk channel structure are expected. In FD-SOI, the channel is very thin (5 to 50 nm for Si) and the depletion zone can form over the entire channel depth.
In addition to eliminating short channel effects, this structure can significantly reduce power consumption and increase switching speed.

Fig. 1.6 Architecture of a nano-scaled planer bulk substrate MOSFET (a) versus a Ge-on-insulator (GOI) thin film MOSFET (b).
1.6 State of GOI Fabrication Technology

So far we have discussed how transistor channels with the germanium-on-insulator structure offer advantages like better electrostatic control of the channel, reduced parasitic capacitance and leakage currents, etc. However, finding a suitable method for the fabrication of such structures is still an open area of research. Several methods have been developed till date for the growth of germanium on insulator with various degrees of success. These are discussed in this section.

1.6.1 Graphoepitaxy

Yonehara et. al.\cite{15, 16} demonstrated the graphoepitaxy method for the solid-state surface energy driven granular growth of predominantly (110) and (100) oriented Ge on smooth and patterned SiO₂ surfaces, respectively. However, the process produced grains of only a few microns in size and the overall yield was less than 50%.

Fig. 1.7 Transmission electron micrograph of a secondary grain in 30-nm thick Ge film over 0.2 μm period surface-relief grating in SiO₂ after annealing for 1 h at 900°C.\cite{15}
1.6.2 Zone Melting

Takai et. al.\textsuperscript{[17]} demonstrated the formation of up to 250 x 100 μm area single crystalline germanium on SiO\textsubscript{2} by moving polycrystalline Ge islands under a graphite strip heater. However, there was no control on the crystal orientation. The crystallization occurred with a (100) predominance, although (111) orientation also occurred with a rather high frequency and the (110) orientation to a lesser extent.

![Optical micrograph of zone melted Ge islands on SiO\textsubscript{2}.\textsuperscript{[17]}](image)

1.6.3 Laser Annealing

Sakaike et. al.\textsuperscript{[18]} demonstrated the formation of [220] preferentially oriented Ge on quartz substrate by scanning with a semiconductor diode laser. Although the process achieves 100% crystallization, the Ge film becomes polycrystalline with [220] preferential orientation. It also produces grains with a typical length of 1 μm and width of 200 nm laterally aligned along the scanning direction.
Developed at the Advanced LSI Technology Laboratory of Toshiba corporation, the Ge condensation is a significantly improved technique for producing high quality GOI. In this technique strained GOI substrates can be fabricated with the Ge layer thickness of less than 10 nm by oxidizing a SiGe layer, grown epitaxially on an SOI substrate. Realization of high quality GOI layers with Ge fraction up to 99.5%
or higher has been shown possible. Such GOI layers were shown to be compressively strained (1.1%). Defect-originated hole concentration of the Ge layer was shown to be $1.3 \times 10^{17} \text{cm}^{-3}$.

1.6.5 Lateral Rapid Melting Growth (RMG)

The lateral rapid melting growth or RMG technique, which is also the technique that is investigated in this dissertation, is a lateral liquid phase epitaxy process that allows the growth of micro-structured GOI films on a Si substrate.[22-34] The sample structure is shown in Fig. 1.11(a).[26] The process employed Si substrates with a top insulating layer of SiO$_2$ or Si$_3$N$_4$. The Si substrate is used for seeding the epitaxial growth. Seed windows are opened onto the insulator layer by photolithography and wet etching. The a-Ge layer is deposited in ultra high vacuum ($5 \times 10^{-10} \text{Torr}$). Subsequently, photolithography and wet etching is used to make a-Ge strip patterns extending from the seed area over the insulator. The strips have been made with widths ($W$) of 2 – 15 μm and length ($L$) from few tens of μm to few hundred μm. The Ge strips are covered with a SiO$_2$ capping layer. The melting growth is performed in a rapid thermal annealing (RTA) system at a temperature (980°C) above the melting point of Ge (937°C). The Nomarski optical micrograph of a set of strips after the RTA process is shown in Fig. 1.11(b).[26] It can be seen that there is Ge agglomeration for strips wider than 5 μm. Such agglomeration occurs because the pressure from the molten Ge caused the capping layer to flex allowing the liquid to flow. Consequently, large area GOI patterns could not be made as it caused the capping layer to break resulting in severe agglomeration. Agglomeration
free strips were shown obtainable for width less than 5 μm. Also a minimum separation of 5 μm between strips was shown necessary to maintain adequate cap strength.

In recent years significant improvement has been made in this technique, which demonstrated the fabrication of chip length (~1 cm) single crystalline GOI strips (width: ~3 μm, thickness: 100 nm), the formation of mesh structures, hybrid integration of (100), (110), and (111) GOI on a single chip, and the fabrication of narrow-spacing strip arrays. Using this process it was possible to reduce defect generation to $6 \times 10^{16} \text{ cm}^{-3}$ resulting in high hole mobility (1040...

Fig. 1.11  Schematic of sample structure (a), Nomarski optical micrograph of GOI strips after RTA on Si$_3$N$_4$/Si(100) substrate (b), EBSD image of a 3 μm wide strip grown from Si(100) seed (c).
cm$^2$V$^{-1}$s$^{-1}$).[27]

However, the work was done mostly on achieving thick ($d \geq 100$ nm) GOI layers in micron width structures. Also, a significant drawback was the difficulty in the orientation-stability of (111) GOI, in that rotation of the crystal orientation occurred for strips grown along <112> and nearby directions (depicted in Fig. 1.11(c)), whereas stable (111) oriented growth was achieved in <011> direction.[28, 30]

1.7 Purpose of this Work

Over the last fifty years, the performance of Si based microprocessors has been improved continuously through device scaling and improving device architecture. However, Si transistor performance is fundamentally limited by the carrier mobility. Furthermore, the Si transistor is scaled into the nanometer scale where maintaining transistor operation becomes exponentially difficult. In these circumstances, implementation of high mobility semiconductors for next generation LSI development has become essential and significant research efforts are being exerted for such ends. This work is part of that effort.

The main purpose of this work is to develop orientation stabilized nano-structured GOI using the rapid melting growth process. This method was presented in the previous section. We have seen that the previous work on the RMG method was focused on fabricating large area Ge strips, achieving 3 μm x 1 cm strips at a thickness of 100 nm. In the discussion we identified several limitations in the current state of the process. Moreover, till date no demonstration has been done on the nanofabrication of GOI using RMG. As a result, we have undertaken the task to
develop the nanofabrication process of Ge-on-insulator structures using the promising RMG method. It is expected that growth characteristics and crystal quality will have a significant dependence on the fabrication process and structural dimensions. Hence, the crystal characteristics will also be extensively analyzed.

A major problem of the RMG technique is the rotation of crystal orientation along the strip length in the growth of (111) oriented Ge in <112> crystallographic direction. Recent development in Ge CMOS FET has shown that the electron mobility shows a strong dependence on crystal orientation. It was demonstrated that the effective electron mobility in a (111) Ge channel is 1.5 times higher than that in (100) oriented channel and also from that of universal Si electron mobility. Therefore, it is essential to obtain orientation stabilized (111) GOI using the RMG method, which is also a goal of this work.

1.8 Thesis Organization

In chapter 1, the motivation, background, and the purpose of this work have been presented.

In chapter 2, the nanofabrication process of GOI by RMG and the crystal characteristics of (100) oriented Ge nano-strips are presented. Here the growth characteristics and crystal quality on Ge strip dimensions are discussed. It is demonstrated here that thickness reduction of Ge strips tends to produce orientation instability. It is also shown that width narrowing is effective in suppressing the unstable growth. We find that shrinkage of Ge strips where width approaches thickness can improve growth characteristics, thereby demonstrating that growth of
high crystal quality Ge nano-structures is feasible and only limited by the resolution of the lithographic process.

Chapter 3 presents the results of the effort to obtain orientation stabilized growth of GOI from (111) seed. In this work we employed the knowledge of orientation stabilization by width narrowing, as learned from the work on (100)-GOI nanofabrication, is employed. Successful stabilization of crystal orientation in thick (100 nm) and thin (50 nm) (111)-oriented GOI strips by width narrowing has been demonstrated. Here too, we will see that growth characteristics improve with width approaching thickness value. However, a strong dependence on growth orientation is also found. Crystal characteristics are presented in detail in order to understand the cause of orientation instability and the how stability is obtained by width reduction. The data are analyzed in the next chapter.

Chapter 4 is the detailed analysis of crystal characteristics of rapid melting grown Ge in order to find the physical process of rotation and the reasons behind the observed effects of thickness and width reduction. Here, various previous propositions on the explanation of the process are discussed. A comprehensive model to explain lattice rotation is presented in this chapter.

Chapter 5 summarizes the main achievements in this work.
References


Chapter 2

Nano-Fabrication of (100) GOI

In this chapter, the nanofabrication process for the rapid melting growth of Ge nano-strip on insulator is presented. Micro- and nano-strip Ge growth is performed from (100) oriented Si seed and their crystal characteristics and growth characteristics are determined. It is shown that progressive lattice misorientation during growth is induced by decreasing Ge layer thickness. It is also shown that orientation stabilized growth is possible by width reduction. The results in this chapter will show that growth of high crystal quality Ge nano-structures is feasible.

2.1 Motivation for the Nanofabrication of GOI by RMG

In chapter 1, we discussed why the implementation of Ge-on-insulator (GOI) channel is necessary for performance improvement in extremely scaled transistors. We also discussed how the rapid melting growth (RMG) technique is promising for the fabrication of high quality GOI. However the current state of GOI fabrication by rapid melting growth is limited to relatively large structures, e.g., typical strip width of 3 μm with a thickness of 100 nm, as reported by Miyao et al.\textsuperscript{[1-8]} Till date no data is available on the feasibility of nano-scaled RMG process. This work is focused on examination of the feasibility of nano-fabrication of GOI by RMG. We want to
demonstrate this by reducing Ge layer thickness $d \leq 50$ nm and width $W \leq 0.5$ μm. We also want to investigate in detail on how the growth characteristics and crystal characteristics are affected by thickness and width reduction of Ge structures.

Fig. 2.1 Work flow of the study.
2.2 Workflow and Design

The workflow of this study is presented in Fig. 2.1. The development of the fabrication process is aimed at producing Ge patterns with feature size down to a few hundred nanometers. With the new fabrication process, GOI strips were fabricated with specifications similar to previously published works in order to compare the characteristics. Dimension shrinkage was done in steps in order for detailed investigation of the effects of such scaling on growth characteristics.

![Schematic side view (a) and top view (b) of GOI strips.](image)

Fig. 2.2 Schematic side view (a) and top view (b) of GOI strips.
The design concepts of the patterns in this investigation are shown in Fig. 2.2. The GOI strip patterns are arranged in dense strip arrays with strip width ($W$) ranging from 0.5 to 3 μm and spacing ($S$) from 0.5 to 1 μm. The length ($L$) is 200 – 400 μm. These patterns will test our ability to perform RMG on nano-structured GOI at reduced layer thickness.

### 2.3 Nanofabrication Process of GOI by RMG

In order to fabricate the nano-structured GOI using the rapid melting growth process, significant changes had to be made in the fabrication process. The fabrication process is described here.

The nanofabrication process flow is presented in Fig. 2.3. As in the previous

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Fig. 2.3 Nanofabrication process flow.
experiments, our primary substrate was Si (100) with a chemical vapor deposited top layer of Si$_3$N$_4$. For high resolution and position accuracy, all the patterning was done by electron beam (EB) lithography.

Fig. 2.4 Nomarski optical micrograph of a set of Au/Ti reference marks used in EBL alignment (a) and schematic diagram explaining the lithography process for pattern creation (b).

In the first step, gold reference marks, necessary for pattern positioning in the lithography process, were made. A positive resist, ZEP520A, was used as our primary EB resist. In the positive resist, the electron beam exposed areas become soluble in a suitable developer due to suppression of polymer cross linking. The lithography exposure was performed with an 80 kV electron beam in an Elionix EBL system. Oxylene, which is a high resolution developer for ZEP, was used to remove the exposed areas followed by a rinse in isopropyl alcohol (IPA). Using an electron beam evaporation system, a 5 nm layer of Ti followed by an 80 nm layer of Au was
deposited on the patterned resist. The Ti layer was necessary to provide stronger adhesion to the Si$_3$N$_4$ surface. Metal lift off was performed in organic solvent (ZDMAC) to leave the reference marks on the Si$_3$N$_4$/Si substrate. The reference marks pattern we used is shown in Fig. 2.4(a).

In the next step, selected areas (seed windows) of the Si$_3$N$_4$ layer were removed to expose the Si substrate for seeding. The process is illustrated in Figs. 2.4(b) and 2.5(a). The seed patterns were created on ZEP in the EB lithography process. Rectangular patterns with area of 30x50 μm were used as the seed windows. Wet etching of Si$_3$N$_4$ by HF solution was found to be unsuitable for pattern transfer as the EB-resist was seen to be damaged by the etching solution. To overcome the problem, we used an anisotropic dry etching process with Ar-ion milling. This was

![Fig. 2.5 Seed window opening by dry etching (a) and a-Ge deposition from the Ge K-cell in ultra high vacuum (b).](image)
also very important in cases where the GOI layer thickness was smaller than the Si$_3$N$_4$ layer. A steep seed edge was found to cause breaking of the molten Ge layer from the seed onto the insulator during growth. In such cases, we performed the dry etch at an angle of 30°, resulting in a sloped seed edge that enabled the continuation of growth without breaking at the seed edge. After the etching, the resist were removed in the usual process.

Fig. 2.6  Electron-beam lithography for GOI pattern creation (a), and pattern transfer on to Ge layer by dry etching (b).

In the following step, the layer of amorphous germanium (a-Ge) was deposited on the sample in a molecular beam epitaxy (MBE) system (illustration in Fig. 2.5(b)). Prior to loading into the MBE chamber, the samples were cleaned in acetone, IPA, and deionized water followed by an HF (1%) treatment to remove natural oxides. In addition, in-situ thermal cleaning was performed at a temperature of 550°C in vacuum for 30 minutes. Deposition of Ge was performed using a Knudsen-cell with
the sample at room temperature. The deposition chamber base pressure was about 5\times 10^{-10} \text{Torr}. Post deposition annealing was performed at 300°C for 30 min.

After we obtained the a-Ge layer, it was patterned by EB lithography (Fig. 2.6(a)). The process was optimized to produce high resolution patterns. The ZEP520A resist was diluted with Anisole to give a resist thickness of about 250 nm in order to produce the narrow patterns down to about 100 nm. The exposure was performed at a beam current of 50 pico-ampere with an acceleration voltage of 80kV. Development was performed in Oxylene followed by sample rinse in IPA. The pattern transfer was performed with a combination of Ar-ion milling and CF$_4$ reactive ion etching (RIE) to etch the 100 nm thick GOI without damage (Fig. 2.6(b)). For thin (~50 nm) Ge layers, only CF$_4$ RIE was used. Afterwards the resist was removed using O$_2$ plasma ashing.

Once the GOI patterning was completed, the samples were carefully cleaned to remove organic and metallic contaminants, finishing with an HF (1%) treatment, and quickly loaded in a magnetron plasma sputtering system for capping layer deposition. It was found that a SiO$_2$ capping layer of a minimum thickness of 800 nm was necessary for agglomeration free growth of the nano-strips.

After deposition of the appropriate capping layer, the RTA process (Fig. 2.7(a)) was performed on the sample to induce the lateral melting growth. The typical RTA heating pattern is shown in Fig. 2.7(b). The peak temperature was set between 980 and 1000°C for 1 sec, which raised the sample temperature just above the melting point of Ge (937°C). From previous experiments,$^{[10]}$ it has been found that a slow cooling of the sample after melting is necessary to reduce random nucleation and
allow the lateral growth to proceed uninterrupted. A heating step at 800°C for 1 min prior to the melting peak obtained a slow cooling rate of about 11°C/s that allowed the lateral growth to complete without random nucleation. After the RTA process, the capping layer was removed in 15% HF solution to bare the grown GOI strips for characterization.

![Diagram of RTA process](image)

**Fig. 2.7** Schematic representation of rapid thermal annealing (RTA) of the sample consisting of the SiO₂ capped (~800 nm) GOI strips (a) and typical heating patterns used in the RTA process.

The surface morphology of the GOI strips was observed and imaged with Nomarski optical microscope. The grown strip thickness was measured with a surface profiler. The structures of the strips were observed by scanning electron microscopes (SEM). The crystallinity of the grown strips was confirmed by Raman spectroscopy. The crystal orientation was measured by electron backscatter diffraction (EBSD) analysis. The detailed results are described in the next section.
2.4 Characteristics of Thick GOI Micro-Strips

The first trial was to fabricate (100) oriented micro-strips using the nanofabrication process and compare the growth characteristics to previously published results. The results for thick \(d = 100 \text{ nm}\) 2 μm-wide strips with a spacing of 0.5 μm are presented in Fig. 2.8, which shows the Nomarski micrograph and also the crystal orientation map obtained from EBSD analysis along the three axes.

![Fig. 2.8 Nomarski optical micrograph and EBSD images of a successfully grown wide strip array \((W = 2 \mu m, S = 0.5 \mu m)\) from Si (100) seed and the crystal misorientation profile along the length of the strip.](image)

---

**EBSD Legend**

- **ND(z)**
- **RD(x)**
- **TD(y)**

**Axes:**

- **TD(y)** <110>
- **ND(z)** <100>
- **RD(x)** <110>

**Angles:**

- 100
- 111
- 110

**Images:**

- Seed
- 2 μm wide
- 0.5 μm spacing
- 100 nm deep

**Distance from seed (μm):**

0 10 20 30 40 50 60

**Misorientation (°):**

0 10 20 30 40 50 60

**EBSD Legend:**

- Nomarski optical micrograph
- EBSD images
- Crystal orientation map
- Misorientation profile
It can be seen that the strips grown from Si (100) seed are single crystalline in the same orientation as the seed for the entire length. No randomly nucleated crystal grains were observed. The lattice misorientation from the seed orientation was measured by EBSD analysis. The misorientation analysis measures the lattice frame
at the point of measurement and calculated the angular distance with the lattice frame at the reference point (seed area). By making this measurement at points along the length of the strip, a misorientation profile that represents the total angular deviation of the lattice from the seed orientation can be obtained. The misorientation profile, as shown in Fig. 2.8, shows no deviation in crystal orientation from seed orientation along the length of the strips.

To determine the crystal quality, Raman spectroscopic measurements were performed on the strips. The laser wavelength was 532 nm with a beam spot size of 1 μm. The sharp Ge—Ge vibration mode peaks at different positions on the strips, shown in Fig. 2.9(a), indicates the formation of crystalline Ge. As shown in Fig. 2.9(b), the full width at half maximum (FWHM) values of the Ge—Ge peaks are very close to that obtained from a c-Ge wafers (3.2 cm⁻¹) and indicates a high crystal quality. From the Raman spectrum analysis, we also determined the Si diffusion profile along the length of the strips according to the method described by Mooney et al. The profile is plotted in Fig. 2.9(c). The initial Si concentration of about 3% at the seed edge drops below measurable level within about 50 μm. Therefore pure Ge crystal is obtained for the rest of the strip length. These results are similar to previously published results on rapid melting grown GOI micro-strips and indicate that the newly developed nanofabrication process is capable of producing high quality GOI structures.
2.5 Characteristics of Nano-Strip GOI

The GOI strip growth was performed with \( W = 0.5, 1, \) and \( 2 \, \mu m \) and \( S = 0.5 \) and \( 1 \, \mu m \). Here the Ge layer thickness was reduced to \( 50 \, nm \). The growth morphologies are shown in the Nomarski optical micrographs of Fig. 2.10. It can be seen that growth of uniform strips was possible with strip widths of \( 0.5 – 2 \, \mu m \) and spacing of \( 0.5 \, \mu m \). This is a significant improvement over the previous reports \((W = 3 – 5 \, \mu m, S = 5 \, \mu m, d = 100 \, nm)\). Even higher density patterns may be possible by tuning the EB lithography conditions. These results indicate that the RMG process can be applied for the fabrication of nano-structured GOI.

![Fig. 2.10](image.png)

EBSD analysis was performed to determine the crystal orientation of these strips. Surprisingly, severe crystal misorientation was observed in \( 1 \) and \( 2 \, \mu m \) wide
strips. These results can be seen in Fig. 2.11, where the crystal orientation is color mapped on the SEM images of the strips. The color coded EBSD images reveal that crystallization initiates from the Si seed (on the left) but gradually changes along the length of the strips. This means that there is rotation of the crystal along the growth length. This kind of rotational growth was previously observed only in thick (100 nm) (111)-oriented GOI strips grown along <112> direction. To analyze the rotational behavior in detail, the misorientation profiles of the strips along the length

![Strip array: W = 2 μm, S = 1 μm](image)

![Strip array: W = 1 μm, S = 0.5 μm](image)

![Strip array: W = 0.5 μm, S = 0.5 μm](image)

Fig. 2.11 Crystal orientation maps obtained by EBSD analysis of 2 μm, 1 μm, and 0.5 μm-wide GOI strips (d = 50 nm)
direction were obtained from EBSD analysis. These are plotted in Fig. 2.12. It becomes clear from these profiles that gradual crystal rotating is taking place along the strip length. Compared to the wide strips, no discernible misorientation can be observed in the 0.5 μm wide strips, whose EBSD images are shown in Fig. 2.11, where the entire length of the strips appear to be in (100) orientation. The misorientation profile for the 0.5 μm wide strips, plotted in Fig. 2.12 along with the wide strips, shows no orientation deviation along the length.

![Fig. 2.12 Crystal misorientation profiles of thin (d = 50 nm) GOI strips as a function of distance from the seed.](image)

To determine possible degradation of crystal quality by thickness reduction, Raman spectroscopic analysis was performed on these strips. The laser beam spot size for the Raman measurement was 1 μm. Therefore, the spatial resolution is limited to 1 μm. The sharp Ge—Ge vibration mode peaks at different positions on the
Fig. 2.13  Raman spectra of thin \((d = 50 \text{ nm})\) GOI strips \((W = 0.5 - 2 \mu m)\) grown from Si (100) seed observed at different positions along the strip length \((x = 0, 10, \text{ and } 220 \mu m)\) (a), FWHM values of the Ge—Ge vibration mode Raman peaks (b), and the Si diffusion profile along the length of the strips (c).
strips, shown in Fig. 2.13(a), indicates the formation of single crystalline Ge. As shown in Fig. 2.13(b), the full width at half maximum (FWHM) values of the Ge—Ge vibration mode peaks are very close to that obtained from single crystal Ge wafers (3.2 cm⁻¹). These characteristics are similar to that of the micro-strip GOI and indicate that the GOI structures can be grown with consistent quality regardless of nano-scaling.

From the Raman spectrum analysis, we also determined the Si diffusion profiles along the length of the strips. The profiles are plotted in Fig. 2.13(c). The Si concentration at the seed area can reach about 5% and rapidly drops below measurable level within few tens of microns. Therefore pure Ge crystal is obtained for most of the strip length. Also, no significant difference is found in the profiles obtained from strips of different width. However, the profiles appear steeper compared to the Si concentration profiles of thick (100 nm) strip GOI strips, shown in Fig. 2.9(c), and literatures.\[1\]

The physical process of suppression of lattice rotation by width narrowing will be discussed in detail in chapter 4.

### 2.6 Summary

The feasibility of nano-scaling of Ge-on-insulator structures by rapid melting growth was demonstrated in this chapter. It was shown that at the Ge layer thickness of 50 nm and a SiO₂ cap thickness of ~800 nm, GOI strips can be reliably grown without any agglomeration. It is expected that further reduction of strip width is possible. In the course of the scaling efforts, it was found that stability of growth
orientation is greatly dependent on Ge strip thickness and width. We saw progressive misorientation of lattice along the growth direction in thin \((d = 50 \text{ nm})\) Ge strips, whereas no such misorientation was observed in thick \((d = 100 \text{ nm})\) strips. Surprisingly, it was also that orientation stabilized growth of thin Ge strips is possible by width shrinkage, where we saw progressive improvement of orientation stability with width reduction. In the case of 50 nm thickness Ge strips, stable growth was obtained by width shrinkage to 0.5 μm. Detailed explanation of the physical process of misorientation in thin Ge strips is given in chapter 4. The crystal quality of the nano-scaled Ge strips was also examined by Raman measurements and no deviation in quality was found. The results obtained in this study indicate that it is possible to fabricate high quality nano-strip Ge-on-insulator and demonstrate the promise of the RMG process for implementation in next generation CMOS process.
References

Chapter 3

Orientation Stabilized Growth of (111) GOI

In chapter 2, the ability to achieve orientation stabilized growth of (100) oriented Ge-on-insulator (GOI) strips by shrinking the strip width was demonstrated. It is possible that the physical process underlying this effect is universal to Ge grown by rapid melting process and can be implemented to stabilize the lattice rotation previously observed in the growth of GOI from (111) Si seed along <112> direction. In this chapter, the successful application of this method in the orientation stabilization of (111) GOI is presented. With a view to understanding the physical process of lattice rotation, detailed experimental results of the dependence of growth characteristics on strips dimensions are presented.

3.1 Background

For the continual improvement of performance of large-scale integrated circuits (LSIs), intensive investigation is being carried out to develop high mobility functional materials to replace Si.[1-6] The recent development of high quality and stable passivation layers on Ge has opened up the possibility to implement its high electron and hole mobility for the next generation LSI.[7-9] In the development of Ge complementary metal oxide semiconductor (CMOS) technology, control of the
crystal orientation is essential, since the maximum electron and hole mobility are orientation dependent. The (111) oriented Ge is necessary for high-speed n-channel transistors, because the inversion layer mobility of electrons in Ge metal-oxide-semiconductor structures shows the maximum value on the (111) plane. Research has also been focused on the development of Ge-on-insulator (GOI) structures, which is fundamental for developing Ge based fully depleted (FD) channel transistors. The (111)-oriented GOI is a key material structure because not only can it be implemented for high-speed transistor channels, it can also be used

![Diagram of sample structure showing strip orientation with respect to wafer flat (a), Nomarski optical micrograph of a 2 μm-wide (111)-GOI strip (b), and EBSD images of (100) and (111) oriented GOI strips grown along different wafer directions (c).](image)

Fig. 3.1  Schematic of sample structure showing strip orientation with respect to wafer flat (a), Nomarski optical micrograph of a 2 μm-wide (111)-GOI strip (b), and EBSD images of (100) and (111) oriented GOI strips grown along different wafer directions (c).[21]
as templates for the integration of optoelectronic (e.g. GaN) and spintronic materials (e.g. Fe₃Si) with the Si CMOS process.¹⁰⁻¹⁴

In order to integrate the much needed GOI with the Si CMOS process, the rapid melting growth (RMG) process has been developed, which enables lateral growth of microstructured GOI from Si substrates over insulating films.¹⁵⁻²⁶ In the effort to grow (111) oriented GOI using the RMG process, instability of growth orientation was observed. Here, rotation of the crystal lattice was found to occur for strips grown along <112> and nearby directions, whereas stable (111) oriented growth was achieved in <011> direction.²¹,²³ Such rotational growth was attributed to the weak bonding force between lattice planes along <112> which results in lattice plane slipping at the growth front.²¹ The results from these reports are reproduced in Fig. 3.1. In this work we investigated the techniques for the stabilization of crystal orientation during rapid melting growth.

3.2 Design

In our work on the development of thin (100) oriented GOI, we observed that the orientation stabilized growth becomes possible when the strip width is sufficiently narrowed, as described in Chapter 2. This led us to speculate that similar orientation stabilization can be achieved in (111) GOI growth by controlling the thickness and narrowing the strip width. Therefore, the focus of this work is:

(i) Orientation stabilization of thick (100 nm) GOI grown from Si (111) seed along <112> direction by width narrowing.

(ii) Detailed investigation of Ge strip dimensions on growth characteristics.
The strips were designed based on the above assumption. The design schematics are presented in Fig 3.2.

![Diagram of sample structure](image)

**Fig. 3.2** Schematic structure of sample used for (111)-GOI growth (a), and schematics structure and explanation of orientation of GOI strips (b).

### 3.3 Fabrication Process

The fabrication of the samples was done in a similar process as described in Chapter 2. The sample structure used for the rapid melting growth of the (111) GOI is shown in Fig. 3.2(a). The substrate was (111)-oriented Si with a 100 nm thick top layer of Si$_3$N$_4$. Seed windows were opened through the Si$_3$N$_4$ layer by electron beam...
lithography and dry etching. The samples were cleaned using the RCA process to remove organic and metallic contaminations. The a-Ge layers were deposited on these substrates at room temperature using a Knudsen-cell in a molecular beam epitaxy (MBE) system under ultra high vacuum (5x10^{-10} Torr). In-situ thermal cleaning at 550°C for 30 min was performed prior to the deposition. Patterning of the Ge layers into strip structures (W = 0.2 – 2 μm, L = 250 μm, and S = 0.5 – 1 μm) was performed by electron beam lithography and reactive ion etching using CF4. The schematic structure of the patterns is shown in Fig. 3.2(b). In the schematic, θ is the angle between <011> of the Si substrate and the strip growth direction. Strips were fabricated with θ = 0°, 30°, 60°, 90°, and 120° corresponding to <011>, <112>, <101>, <211>, and <110> direction of the substrate, respectively. The a-Ge strips were capped with a SiO2 layer (thickness: ~800 nm). The melting growth was performed by rapid thermal annealing (RTA) at 1000°C (1 sec). After RTA, the capping layer was removed for electron backscatter diffraction (EBSD) and Raman spectroscopic analysis.

3.4 Thick (100 nm) (111)-GOI Growth Characteristics

Growth features were characterized by Nomarski optical microscopy and electron backscatter diffraction (EBSD) analysis. The results of the <011>-directed samples (W = 0.5 – 2 μm) are shown in Fig. 3.3. For all samples, completely (111)-oriented growth is achieved in the entire growth regions. EBSD analyses of the crystal orientation along the three axes show no misorientation from the seed orientation. These results agree with previously reported work on (111) GOI.\(^{[21]}\)
Fig. 3.3  Explanation of sample orientation (a) and Nomarski and EBSD images for 2 μm-wide (b), 1 μm-wide (c), and 0.5 μm-wide (d) thick (100 nm) GOI strips grown from Si (111) seed along <011> direction.
The <112>-direction growth results are shown in Fig. 3.4, where we can see the EBSD images of crystal orientation along the three axes. We can see that the growth initiates from the Si seed in the same orientation but deviates along the length in 1 and 2 μm-wide strips. The gradual change of colors in the color mapped EBSD images indicates that the misorientation occurs by crystal rotation. Such rotational
growth was observed in previous experiments for growth along <112> and was explained on the basis of the weak binding force between lattice planes at the growth front.\textsuperscript{[21]}

Fig. 3.5 Crystal misorientation profile for the set of thick (100 nm) GOI strips along <011> (a) and <112> directions with various strip widths (b).
For a closer examination of the growth behavior, crystal orientation of the strips in the normal direction (ND), the transverse direction (TD), and the growth direction (rolling direction or RD in EBSD image) were obtained from the EBSD analysis and given in Fig. 3.4. Please refer to Fig. 3.3(a) for an explanation of these directions. From following the color map along the length of the strips, we find that crystal rotation is minimal in the transverse direction (TD), which is the (011) plane (color coded as green). This indicates that the rotation occurs predominantly about the <011> axis. Interestingly, the degree of misorientation appears to decrease with strip width narrowing and seems to be completely suppressed at the width of 0.5 μm, as can be seen in Fig. 3.4(c). Here, no rotation was observed in any of the three axes and (111) orientation was observed along the entire length of the strips.

To investigate the growth features quantitatively, the misorientation angle of strips grown along <011> and <112> were evaluated for different strip widths as a function of the distance from the seed. The results are summarized in Figs. 3.5(a) and 3.5(b), respectively. For growth along <011>, the misorientation angle is almost zero and does not increase in any strip width, which indicates completely orientation-stabilized formation of (111) GOI along <011>. On the other hand, for growth along <112>, the misorientation profile indicates the rotation of crystal orientation along the length of the wide strips. The 2 μm-wide strips appear to be the most unstable as the rotation occurs rather quickly and reached to ~40° within about 20 μm from the seed. In the 1 μm-wide strip, the rotation appears to be slightly gentler. A maximum misorientation of about 20° is seen at a distance of over 50 μm from the seed. This indicates an improvement of orientation stability over the 2 μm.
wide strips. The complete suppression of rotation is evident in the 0.5 μm-wide strips, where the misorientation is negligible and shows no increase at all. This trend of stabilization of growth orientation with decreasing strip width is very clear. The effects of width shrinkage on the crystal orientation of thick (100 nm) GOI strips growth along different directions are summarized in the plot of Fig. 3.6. These results demonstrate a successful method for the fabrication of (111) GOI with any growth direction.

Raman spectra of the samples were obtained by using a 532 nm wavelength excitation laser with a beam spot of 1 μm. The FWHM of Ge—Ge vibration mode peaks of the Raman spectra obtained from the thick GOI strips are plotted in Fig. 3.7. The dashed line corresponds to the FWHM value obtained from single crystal Ge
wafer (3.2 cm$^{-1}$). The observed values confirm that the crystal quality of the GOI strips are comparable to that of single crystal Ge wafers. The narrowing does not seem to effect the crystalline quality as FWHM remains almost the same. It is also interesting to note that the misorientation in the crystal (as observed in 1 and 2 μm...
wide <112> direction strips) does not degrade the crystalline quality either, as the FWHM values remain almost the same as that of single crystal Ge wafers.

Explanation of the rotational phenomena observed in GOI strips is difficult because of the complicated dynamics of the rapid melting growth process. However, we shall analyze the possible physical process involved based on experimental results in detail in Chapter 4.

3.5 Thin (~50 nm) (111)-GOI Growth Characteristics

For application to fully depleted transistors, the RMG process must be capable of producing very thin (≤50 nm) GOI strips. To investigate the effects of Ge layer thinning on growth characteristics, ~50 nm thick GOI strip growth was performed from Si (111) seed. Similar to the previous experiments, 0.5, 1.0 and 2.0 μm wide strips were fabricated under the same processing conditions. The results of the <011> and <112> directed growth is given in Fig. 3.8 and Fig. 3.9, respectively. Not so surprisingly, the thinning of the Ge layer resulted in the appearance of misorientation even for the <011> direction. Crystal orientation measurement shows that the growth does initiate from the Si seed and the orientation deviates gradually along the growth direction. The EBSD analysis of crystal orientation along the normal, growth, and transverse directions of the strips indicated the misorientation results from rotation of crystal orientation along the <011> axis. This can be seen in the color mapped EBSD images of Fig. 3.8(a), where we see the (011) plane (color coded as green) in the growth direction (RD) remains mostly unchanged while rotation occurs in the other
Growth Direction: <110>
(Strip array: \( W = 2 \, \text{μm}, \, S = 2 \, \text{μm} \))

EBSD: Normal Direction (ND)

EBSD: Growth direction (RD)

EBSD: Transverse direction (TD)

(a)

Growth Direction: <110>
(Strip array: \( W = 0.5 \, \text{μm}, \, S = 0.5 \, \text{μm} \))

EBSD: Normal Direction (ND)

EBSD: Growth direction (RD)

EBSD: Transverse direction (TD)

(b)

Fig. 3.8  EBSD images for 2 μm-wide (a) and 0.5 μm-wide (b) thin (50 nm) GOI strips grown from Si (111) seed along <011> direction.
Fig. 3.9 EBSD images for 2 μm-wide (a), 0.5 μm-wide (b), and 0.2 μm-wide (c) thin (50 nm) GOI strips grown from Si (111) seed along <112> direction.
directions. This means the rotation process is similar to that seen in the 100-nm-thick (111) GOI strips ($W = 1 – 2 \, \mu m$) along <112>. Also, similar to the thick (111) GOI, the stabilization of growth orientation appears to improve with decreasing strip width. Similar phenomena was observed in (100) oriented thin GOI also.

Significant difference in the misorientation behavior is seen between strips along the <011> and <112> direction, where <112> directed growth appears more susceptible to misorientation than <011> directed growth. The maximum values of misorientation observed at a growth distance of 50 μm are summarized in Fig. 3.10. In 2 μm-wide strips, the maximum misorientation from the seed orientation reaches

![Fig. 3.10](image-url)  
Maximum crystal misorientation as a function of strip width recorded at $L = 80 \, \mu m$ for thin (50 nm) (111) GOI grown along <011> and <112>. The range of the error bars are obtained from the misorientation profiles of 7 to 12 strips.
to about 45° in <112> direction strips, while it is only about 15° in <011>-direction strips. Narrowing the strips resulted in reduction of misorientation for both directions. At the strips width of 0.5 μm, misorientation in the <011>-direction strips was completely suppressed. In the <112>-direction strips, a maximum misorientation of
about 15° is observed in 0.5 μm strips. This is unlike that of thick (100 nm) strips, where complete suppression was achieved at 0.5 μm strip width. However, the above trend indicates that further narrowing of the strip width can suppress the rotation in <112> direction strips completely. For this purpose, we fabricated thin GOI strips down to 0.2 μm width. Interestingly, as shown in Fig. 3.9(c), we see a complete suppression of rotation in these strips.

Raman spectroscopic analysis of the thin (111) GOI strips, performed with a 532 nm wavelength laser with a beam spot of 1 μm, confirmed high crystalline quality of grown strips regardless of growth direction and width. The FWHM of Ge—Ge vibration mode peaks of the Raman spectrum for <011> and <112> direction strips are given in Fig. 3.11(a) and 3.11(b), respectively. The values are very close to that of a single crystal Ge substrate (dashed line at 3.2 cm⁻¹ in figure). Even for the 0.2 μm wide strips the FWHM value is unchanged. Therefore, crystal quality is not compromised by GOI dimension shrinkage.

### 3.6 Guideline for (111) GOI Fabrication

The growth features obtained for stripes aligned to <011> and <112> directions are summarized as functions of strip width and Ge thickness in Fig 3.12. For growth along <011>, (111)-oriented GOI (100 nm thickness) is obtained for all strip widths. However, crystal rotation is observed for thin (50 nm) GOI in wide strips (1 - 2 μm). Such orientation rotation phenomena are effectively suppressed by narrowing the strips (≤0.5 μm). On the other hand, for growth along <112>, crystal rotation occurs
even for thick (100 nm) GOI with strips width of 1 - 2 μm. The rotation is suppressed for narrow stripes (≤0.5 μm). For thin (50 nm) GOI, orientation stabilization is achieved only for strip width below 0.2 μm. It is noted that more narrowing is necessary to realize complete orientation stabilization along <112>, compared with
<011>. This is attributed to the weak bonding of lattice planes of (112) growth fronts. Based on these findings of the effects of strip dimensions on orientation stability of GOI grown from Si (111) seed, a guideline for the fabrication of orientation-stabilized (111) GOI structures has been quantitatively obtained.

3.7 Summary

The effects of Ge strip dimensions on growth characteristics during rapid-melting growth of GOI from Si (111) seed were investigated. It was found that crystal orientation becomes unstable at reduced Ge layer thickness. In general, crystal orientation of GOI strip-growth along <112> direction was shown to be more unstable compared to growth along <011> direction. The complete suppression of crystal misorientation by sufficient narrowing of the strip width was also demonstrated. At 100 nm Ge thickness, misorientation was observed in <112> directed strips only, where stabilization was achieved at a strip width of 0.5 μm. At 50 nm GOI thickness, misorientation occurred in strips with all growth directions, however with a higher intensity along <112>. For <011>-directed strips, stabilization was achieved at 0.5 μm width, whereas for <112>-directed strips narrowing down to 0.2 μm was necessary for stabilization. This technique is an important step towards developing the next-generation LSIs, where multi-functional devices can be integrated on the Si platform.
References


Chapter 4

Analysis and Modeling of Lattice Rotation

In this chapter, the overall trend in lattice rotation and the effects of Ge strip dimensions are discussed in detail. Previously proposed explanations for lattice rotation are evaluated in light of current results. It will be shown that Si diffusion from the seed into the Ge strips is the primary cause of the observed rotation. The suppression of rotation by strip width narrowing will be shown explainable by the difference in strain relaxation mechanism in wide and narrow strips with the help of a comprehensive strain relaxation model.

4.1 Overall Trend in Lattice Rotation

In chapters 2 and 3, detailed EBSD analysis of Ge strips on insulator grown from (100) and (111) oriented Si substrates were performed to establish the nature of misorientation in different crystal orientations and the dependence on Ge thickness and strip width. In these analyses, the lattice rotation was found to be dependent on the width and thickness of Ge strips as well as on crystal orientation. The results of the analyses are summarized in this section.
Fig. 4.1 Maximum rotation angle vs. strip width for GOI strips grown from (111) seed along <112> (a) and <011> (b) directions, and from (100) seed along <110> direction (c).
In Fig. 4.1, the maximum rotation angles of Ge strips with different orientation and thickness are summarized as a function of strip width. Here, the maximum rotation angle is defined as the maximum deviation from the seed orientation in which the crystal orientation of a strip stabilizes. It is apparent from these plots that orientation stability can not only be improved but completely stabilized by Ge strip width narrowing. Examination of these plots also reveals that Ge strips grown from (111) seed along <112> direction are most unstable as these are the only strips affected by misorientation at a thickness of 100 nm. The misorientation in this case increases with reduction of thickness from 100 to 50 nm. The maximum misorientation angle decreases by about 10° by the strip narrowing from 2 μm to 1 μm. Below 1 μm width, the suppression of misorientation is more rapid. In the 100 nm thick strips complete orientation stabilization is achieved at a strip width of about 0.5 μm while in 50 nm thick case a further narrowing to about 0.2 μm is necessary. In both cases, complete misorientation suppression appears to be possible by decreasing the strips width (W) to less than five times the thickness (d); that is orientation becomes stable in (111) growth along <112> when the approximate condition (W < 5d) is fulfilled.

The growth from (100) and (111) oriented seed along <011> direction appears more stable compared to (111) along <112> as no misorientation is seen in 100 nm thick strips. However, significant misorientation occurs in these strips at reduced thickness (~50 nm). Similar stabilization effect of width reduction is seen here too. However, the data shows that complete stability is achievable at a width less than that required for (111) growth along <112>. In both these cases, the misorientation is
found to be completely suppressed at a strip width of about 0.5 μm which is ten times the strip thickness. That is, growth stability is obtained when $W < 10d$. The trend with all the above cases indicates that stable growth of Ge-on-insulator is possible as the strip width approaches its thickness; that is where the nano-strip essentially becomes a nanowire.

![Graph and Crystal orientation maps](image)

Fig. 4.2 Effects of Ge layer thickness on misorientation rapid melting growth from Si (111) seed along <112> direction for 2 μm (a) and 1 μm (b) wide strips.
In order to further investigate the effect of Ge layer thickness on growth stability, growth of GOI strips with the thickness of 180 nm, in addition to 50 and 100 nm, were performed from Si (111) seed along <112> growth direction. The results are shown in Fig. 4.2(a) for 2 μm wide strips along with the results for the 50 and 100 nm thick Ge strips. The thickness increase from 50 nm to 100 nm results in a slight improvement of orientation stability, where the maximum misorientation decreases by less than 10°. However, the thickness increase to 180 nm results in significant improvement in growth stability as we can see the maximum misorientation drops to less than 10°. The reduction of strip width from 2 μm to 1 μm yields improved stability, as can be seen from the plots of Fig. 4.2(b). Although the maximum rotation at 50 nm thickness is almost the same as in 2 μm-wide strips, the maximum rotation at 100 nm thickness shows good improvement with the maximum rotation angle being similar to that of 180 nm thick Ge strips. The trend indicates that orientation stability of rapid melting grown Ge strips improves as the difference between thickness and width values are minimized; that is more stable growth is obtained as width approached the thickness value of the strips.

4.2 Defect Generation in Lattice Rotation Region

The progressive crystal misorientation observed along the length of the strips from the seed towards the growth direction links the phenomenon directly to the growth process. This implies that the crystal defects that result in the misorientation are induced during the solidification of the Ge melt.
Fig. 4.3 EBSD image of a thick (100 nm) 2 μm wide GOI strips array grown form Si (111) along <112> direction highlighting the defected area (a), EBSD image quality map where darker areas correspond to defects in the crystal (b), and EBSD grain boundary map showing no grain boundaries are formed along the length of the strips (c).
To understand the nature of the lattice rotation, we performed detailed electron backscatter diffraction (EBSD) analysis of the samples. To relate the rotation areas to high crystal defect areas on the strips we used the EBSD image quality mapping, where crystal defects appear as dark areas. Fig. 4.3(a) shows the crystal orientation map of an array of thick (100 nm) GOI strips ($W = 2 \mu m$). Here the area in which extensive rotation occurs is highlighted by the dashed rectangle. The image quality of the same strip array is given in Fig. 4.3(b). We can see that the defect areas, appearing as dark regions, correspond directly to the rotation regions. On the other

Fig. 4.4  EBSD image of a thick (100 nm) 0.5 μm wide GOI strips array grown form Si (111) along <112> direction (a) and color coded EBSD image quality map (b).
hand, the regions of the strips where crystal orientation appears stable (no change in color) correspond to the light areas of the image quality map. In addition, in order to confirm the color gradation is not due to randomly nucleated grain formation, the grain boundary map obtained from EBSD analysis of the strip array is given in Fig. 4.3(c). It shows no grain formation along the length of the strips.

Fig. 4.4 shows the crystal orientation map and the image quality map obtained from EBSD analysis. Here the image quality map has been color coded for better visibility of defect areas. We can see that there is no deviation of crystal orientation. Also no bad areas are observable in the image quality map, indicating the minimization or suppression of defect creation in the narrow strips. Thus, the stable orientation along the strip length corresponds to the suppression of defects.

Fig. 4.5 shows the crystal orientation map in the z-plane (normal direction) and the x-plane (growth direction) of a 1 μm-wide thin \( (d = 50 \text{ nm}) \) Ge strip array grown from (100) seed along \(<112>\) direction. We can see the variation of the crystal orientation in the color shift of the z-plane image. The figure also includes the typical misorientation profile along the length of the strips as a function of distance from the seed. The misorientation profile is a measure of the maximum deviation of the lattice from the seed orientation. We can clearly see the progressive deviation in orientation, which implies lattice rotation. The lattice rotation is initiated within a few microns from the seed and a maximum rotation of about \(25^\circ\) is produced over a length of about 60 μm. From this point, the crystal seems to acquire stability and no further rotation is observed. On the other hand, the x-plane crystal orientation map shows no observable shift in color. This implies that the rotation axis is parallel to the \(<110>\)
Fig. 4.5 Crystal orientation map in the z-plane and x-plane showing the rotation axis in a thin \( (d = 50 \text{ nm}) \) 1 \( \mu \text{m} \) wide GOI strips (shown in dotted box) grown from Si(100) seed along <110> direction, and misorientation and defect density plots. The dashed line indicates the defect density at which 60% strain relaxation occurs in epitaxial SiGe-on-insulator structures.\(^3\)
Fig. 4.6 Crystal orientation map in the z-plane and x-plane along with the SEM image showing the rotation axis in thin ($d = 50$ nm) 0.5 μm wide GOI strips grown from Si (111) seed along <112> direction, and misorientation and defect density plots. The dashed line indicate the defect density at which 60% strain relaxation occurs in epitaxial SiGe-on-insulator structures.\(^3\)
axis which is also the growth direction. The orientation of a unit cube, as obtained from the EBSD analysis, is also indicated on the z-plane map, where we see the gradual rotation of the cube in the <110> axis.

Similar analysis of the crystal orientation was also performed on the 0.5 μm-wide thin \(d = 50\) nm Ge strip array grown from (111) seed along <112> direction. The results are shown in Fig. 4.6. Here, the misorientation profile shows progressive lattice rotation over a length of about 50 μm that achieves a maximum deviation of about 12° from the seed orientation. The crystal orientation maps along the z, y, and x axes were analyzed to find the rotation axis.

As can be seen from the y-plane orientation map that the rotation axis is <011>, which is equivalent to that in the (100) oriented growth. This similarity shows that the lattice rotation mechanism is similar in both cases.

The observed uniaxial nature of lattice rotation can be described as resulting from the generation of geometrically necessary dislocations (GND) in the Ge crystal. The misorientation occurring at the growth front can be thought of consisting of regularly spaced parallel arrays of screw dislocations that are orientated normal to the rotation axis.\(^1\) A continuous rotation of the crystal lattice can be accommodate in such a case if the arrays of screw dislocations are continuously spaces along the crystal lattice.\(^2\) In such a case the rotation per unit length is directly related to the dislocation density.

Kubin and Mortensen\(^1\) proposed a simple method to calculate the minimum required dislocation density that can be applied to the above describes case. They assume two perpendicular arrays of screw dislocation, in which case the dislocation
density $\rho_{GND}$ required to produce a rotation angle of $k$ per unit length can be given by

$$\rho_{GND} = \frac{2k}{b} \quad (1)$$

Here $b$ is the length of the burgers vector having a value of 0.4 nm (corresponding to 1/2 [110] in the Ge crystal lattice).

The calculated dislocation density values are plotted with the misorientation profiles of Fig. 4.5 and 4.6. We can see that dislocation density is the maximum at the beginning of the strips and trails off along the length. The maximum calculated density was close to $1 \times 10^{14}$ m$^{-2}$ in both cases. Also, in both cases, the defect density approaches $1 \times 10^{12}$ m$^{-2}$; the value at which 60% lattice relaxation has been shown to occur in epitaxially grown SiGe layers.$^{[3]}$

However, this value is the minimum limit of dislocation in the crystal and does not account for the formation of more complex dislocation arrangements or statistically stored dislocations in the lattice. Nevertheless, in addition to causing lattice orientation instability, the value of the generated dislocation is significantly high to make such crystal unsuitable for device fabrication since such defects act as carrier recombination centers.$^{[4]}$ Therefore, elimination of such dislocations becomes essential for device grade Ge-on-insulator fabrication.
4.3 Possible Driving Forces of Lattice Rotation

Several previous reports on the rapid melting growth of Ge on insulator have dealt with lattice rotation and provided different explanation of the process. A summary of the possible driving forces of lattice rotation in rapid melting grown Ge strips is given in Fig. 4.7, where the possible stabilizing mechanisms for the respective causes are also shown. The cited driving forces and stabilizing mechanisms are governed by the bonding strength between lattice planes along the growth direction. In the previous section we have discussed how the formation of...
dislocations in the crystal at the growth front during the melting growth process drives the lattice rotation. We have demonstrated the greater propensity for lattice rotation for growth along <112> direction compared to <011> direction. Previous study has linked this phenomenon to the difference in the bonding force among lattice planes in the <112> and <011> direction growth.\textsuperscript{[5]} It can be proposed that the weaker bonding among lattice planes in the <112> directed growth enhances the formation of dislocations, where it is subsided in <011> directed growth because of the stronger bond among lattice planes in this direction. The total bonding strength among the lattice planes depend on the cross sectional area of the growth front. Thereby, it can also be proposed that reduction of the cross sectional area, e.g., by Ge layer thinning, will result in an enhancement of dislocation formation and the corresponding lattice rotation. In the following sections, we will discuss the possible driving mechanism of lattice rotation in light of the results obtained in this work.

### 4.3.1 Minimization of Interface Energy

Toko et al.\textsuperscript{[5]} described rotation in Ge micro-strips grown from (111) Si seed along <112> direction as resulting from the tendency to minimize the interface energy between Ge and insulator (SiO\textsubscript{2} or Si\textsubscript{3}N\textsubscript{4}). It was demonstrated that micro-strip Ge growth initiated from Si (111) seed along <112> rotated to (100) orientation in order to minimize the Ge/insulator interface energy. Their conclusion was arrived at from the demonstration of interface energy driven crystallization of Ge on SiO\textsubscript{2} using the microzone melting growth process in the 1980s that showed preferential (100) oriented Ge growth and was attributed to the lowest interface
energy of the (100) surface with SiO$_2$.[6] However, the data in our work shows that minimization of interface energy cannot be the primary driving force for rotation, for reasons we will explain next. First of all, the implications of ref. [5] is that no lattice rotation occurs in (100) Ge growth because of its lowest interface energy with the insulator. But we have found rotation occurring in thin (d = 50 nm) (100) oriented Ge growth which cannot be explained by a tendency to minimize interface energy. Secondly, we found from the growth of a large number of strips that the lattice rotation from (111) to (100) orientation is incidental and quite infrequent. No particular preference for the sense of rotation was found either; that is the lattice is equally likely to rotate clockwise or counterclockwise about the rotation axis. Although improved growth stability with strips width scaling implies improvement by the reduction of interface, the above observations show that interface energy cannot, by itself, explain the overall rotation phenomena.

4.3.2 Cooling Rate Dependence

Lattice rotation in rapid melting grown Ge strips on insulator was also investigated by Tweet et al.[7] They demonstrated melting temperature dependent lattice twist in 2 x 20 μm (100) Ge strips with the amount of twist increasing with higher melting temperature. The data shows about 10° of twist in 200 nm thick Ge strip at a melting temperature of 960°C that increases to over 25° at the melting temperature of 1010°C. They also showed that the twist can be minimized by using thicker Ge layer. However, no explanation of the source of twist in Ge strips was given.
Recently Wen et al.\cite{8} published further results on the observance of lattice rotation in (100) Ge at higher melting temperatures in the RMG process. They related the rotation directly to high cooling rate of the sample after melting in the rapid thermal annealing process. It was demonstrated that at cooling rates close to 60°C/s lattice misorientation initiates in (100) oriented Ge and escalates with further increase in cooling rate. They argued that the increased lateral growth rate at higher cooling rate produced a steeper temperature gradient at the growth front that resulted in a higher thermal strain. Such thermal strain and the associated stress were explained to be the driving forces for lattice rotation. However, this explanation does not correspond very well with our experimental results. In our work, the rapid melting growths were performed at cooling rates of 10 – 12°C/s, which is far below the cooling rates shown to cause lattice rotation by Wen et al.\cite{8} In addition, it does not explain why enhanced misorientation is observed by thinning the Ge layer or as to why misorientation is suppressed with width scaling. It is possible that the cooling rate dependent growth rate has an important effect on strain generation and relaxation mechanism. However, in terms of our results, it cannot be explained to be the primary driving force for lattice rotation.

### 4.3.3 Si Concentration Gradient

Till date the most convincing explanation of the driving force for lattice rotation has been given by Tanaka et al.\cite{9} in the rapid melting lateral growth of SiGe micro-strips on insulator.

Their work correlated the lattice rotation to a steep Si concentration gradient,
given as $|dn/dx|$, at the beginning of strips resulting from Si segregation and diffusion from the seed area (reproduced in Fig. 4.8). The results showed that rotational growth is not observed in regions where $|dn/dx|$ is smaller than 0.1 %/μm. Rotation is seen for $|dn/dx|$ larger than 0.1 %/μm with the rate of rotation $|dθ/dx|$ being linearly related to $|dn/dx|$ in this region. The explanation of such relationship is that lattice strain is generated in the SiGe crystal because of the difference in the atomic radii of Si (0.117 nm) and Ge (0.122). The strain field generated in the high concentration gradient region serves as the driving force for the progressive lattice rotation as the growth propagates.

In the growth of Ge strips from Si seed, diffusion of silicon occurs from the seed region into the strips. It is possible a sharp concentration gradient generated

![Fig. 4.8 Correlation between rotation ratio $|dθ/dx|$ and Si concentration gradient $|dn/dx|$ in rapid melting grown SiGe strips with different initial Si content as reported by Tanaka et al.\cite{9}](image)
near the seed region from this Si diffusion causes the observed lattice rotation.

It is expected that the weaker bonding strength in (111) oriented growth along \(<112>\) will result in a shift of the relation in rotation gradient and Si concentration gradient, where we will see rotation at a lower Si concentration gradient. If the assumption on width effect is correct, we can also expect to see left shift of the rotation gradient vs. Si concentration gradient relation for Ge strips grown along \(<112>\) direction. In the next section the effects of Si diffusion on the lattice rotation will be discussed in detail.

### 4.4 Effects of Si Diffusion on Lattice Rotation

In the investigation of the rapid melting growth of SiGe on insulator from Si(100) substrate seed,\(^{9-11}\) correlation has been made between the Si concentration gradient and crystal rotation. The RMG of SiGe results in a laterally graded SiGe profile due to segregation during the melt-back process. It was demonstrated that the amount of crystal rotation is directly related to the lateral Si concentration gradient in the SiGe strips.

During the melting growth process Si-Ge mixing occurs at the seed region; that is the Si in contact with the Ge strips partially melts and diffuses along the length of the strips. The amount of diffusion depends on the annealing temperature and duration. It is possible that the Si concentration gradient formed along the strip length from diffusion can influence the rotational behavior. To analyze the effect of Si in the rotational growth of wide Ge strips, the enhancement of rotation in thin GOI, and rotation-free growth in narrow strips, it is necessary to determine the Si
concentration profiles in the strips. That is, we can expect to find a dependence of the Si diffusion on the strip dimensions.

For this analysis we focused on the \textless 112\textgreater direction strips grown with the thickness of 100 and 50 nm, since the rotational effects are most prominent in these cases. The concentration profiles of Si along the strip length was determined from the Ge—Ge and Si—Ge vibration mode peaks in the Raman spectrum using a method similar to that in chapter 2 and 3. The corresponding results for thick (100 nm) GOI along \textless 112\textgreater are plotted in Fig. 4.9. Examination of the plots shows that lateral diffusion of Si from the seed area does indeed occur. It was expected that the suppression of lattice rotation in 0.5 μm wide strips is due to a suppression of Si diffusion into the

Fig. 4.9 Si concentration profiles in a set of 100 nm thick Ge strips grown from Si (111) seed along \textless 112\textgreater direction at different strip widths.
strips. However, the results show identical diffusion profiles in all of the strip widths.

We can see from Fig. 4.9 that the initial Si concentration of about 3% at the edge of the seed decreases to zero within a few tens of microns. In order to obtain an accurate correlation between rotation and Si diffusion region, the Si concentration gradients

![Graphs showing Si concentration gradient and rotation angle gradient as a function of distance from the seed along the strip length for different strip widths.](image)

**Fig. 4.10** Si concentration gradient and rotation angle gradient as a function of distance from the seed along the strip length for different strip widths.
and rotation gradients were plotted vs. the distance along the strips with different widths and presented in Fig. 4.10. From these plots it becomes clear that there is a strong correlation between the two quantities for the wide strip samples.

![Graph showing relation between rotation gradient and Si concentration gradient in thick (100 nm) Ge strips grown from Si (111) seed along <112> direction with strip widths of 0.5, 1.0, and 2.0 μm. The data for SiGe strips (thickness: 100 nm) grown from Si (100) seed along <011> direction with an initial Si concentration of 6%, as reported by Tanaka et al.\cite{9}, is also plotted for comparison.]

Fig. 4.11  Relation between rotation gradient and Si concentration gradient in thick (100 nm) Ge strips grown from Si (111) seed along <112> direction with strip widths of 0.5, 1.0, and 2.0 μm. The data for SiGe strips (thickness: 100 nm) grown from Si (100) seed along <011> direction with an initial Si concentration of 6%, as reported by Tanaka et al.\cite{9}, is also plotted for comparison.

To compare the relations among different strip widths, the rotation gradient vs. Si concentration gradients are plotted in Fig. 4.11. Here the data of rapid melting grown SiGe strips in (100) orientation as reported by Tanaka et al.\cite{9} are also plotted. The shift of the relation towards the left confirm the prediction that the growth along the <112> direction would show enhanced rotation at lower Si concentration.
Fig. 4.12  Si concentration profiles in thin (50 nm) Ge strips grown from Si (111) seed along <112> direction at different strip widths (a), Si concentration gradients (b), and rotation gradient (c) as a function of distance from the seed along the strip length.
gradient. The plots show that rotation occurs at Si concentration gradient as small as 0.03%/μm, where in the previous results suppression of rotation was shown for Si concentrations below 0.1%/μm. This enhancement of rotation results from the weaker bonding force among lattice planes in the <112> direction.

![Graph showing relation between rotation gradient and Si concentration gradient](image.png)

**Fig. 4.13** Relation between rotation gradient and Si concentration gradient in thin (50 nm) Ge strips grown from Si (111) seed along <112> direction with strip widths of 0.2, 0.5, 1.0, and 2.0 μm. The data for SiGe strips (thickness: 100 nm) grown from Si (100) seed along <011> direction with an initial Si concentration of 6%, as reported by Tanaka et al., is also plotted for comparison.

The Si diffusion profiles in thin (d = 50 nm) GOI strips grown from Si (111) seed along <112> direction is shown in Fig. 4.12(a). Here too we see almost identical
Si diffusion in strips with different widths (0.2 – 2 μm). However, higher Si concentration gradient was found, as shown in Fig. 4.12(b), compared to 100 nm thick Ge strips. Nevertheless, the rotation gradients for different strips widths, plotted in Fig. 4.12(c), show similar correlation with Si concentration gradient. At the same time, the decreasing rotation gradient with strips width narrowing is also evident. The relation between the rotation gradients and Si concentration gradients, as plotted in Fig. 4.13, show a further shift of the plot to the left. This could result from a further weakening of the binding force among lattice planes due to the reduction of the strip cross section because of the thinning.

The above discussion has established the strong correlation between the Si diffusion and lattice rotation. However, it also demonstrated that the Si diffusion profile does not depend of Ge strip width as nearly identical profiles were found in strips of different widths at a given thickness. Such results indicate that in narrow strips the lattice stress generated from Si concentration gradient is released without initiating dislocation formation. In the next section, the strain relaxation mechanism is examined in detail.

### 4.5 Effects of Ge Strip Geometry on Strain Relaxation

From the discussions in the previous sections, it becomes clear that the observed lattice rotation in rapid melting grown Ge strips on insulator is effected by the generation of dislocations in order to release the lattice stress caused by a Si concentration gradient along the length of the strips. It also becomes clear that the suppression of lattice rotation by strip width narrowing cannot be explained by the Si
diffusion effect as the Si concentration gradient was found largely independent of the strips width. On the other hand, the gradual suppression of lattice rotation with strip width narrowing is indicative of a strain relaxation mechanism that is dependent on Ge strip geometry. In this section we examine the dependence of strain relaxation mechanism on Ge strip geometry and present a comprehensive model to explain the process.

Fig. 4.14 Plane view TEM images of 150 nm thick Si$_{0.8}$Ge$_{0.2}$ films epitaxially grown on a Si (100) substrate with patterned SiO$_2$ windows of 2.5×2.5, 4.5×4.5, and 9.0×9.0 μm$^2$.\cite{12}

The structural dependence of strain relaxation was previously examined by Nishida et al.\cite{12} Their report demonstrates that generation of dislocation in the epitaxial growth of strained SiGe on Si substrate can be suppressed by limiting the growth area to 2.5×2.5 μm$^2$. Some results from ref. [12] are shown in Fig. 4.14. Nishida et al. also showed that the residual strain is significantly lower near the edge of the SiGe structures. Their data indicated that the residual strain in the island structures fall of exponentially near the edges. It was reasoned that the edge of the SiGe structures can be considered are free surfaces and the strain in this area is
released by local deformation. It is possible that such shape dependent strain relaxation mechanism is also active in the rapid melting grown Ge strips.

Recently, the strain relaxation mechanism in strained Si$_{0.703}$Ge$_{0.297}$ mesas on Si substrate has been investigated by Tomita et al.$^{[13]}$ They measured the stress states at different distances from the edge of such mesa structures. It has been demonstrated that the stresses in such structures are relaxed within a distance of about 1 μm from the edge. Their results show an exponential stress profile with the distance from the edge, where the stresses are mostly relaxed in a range of 200 nm from the edge. They also showed by finite element method (FEM) simulation that the strain relaxation can be explained by elastic deformation along the free edges.

The references discussed above indicate that significant difference in the strain relaxation mechanism between wide and narrow strips is possible. However, unlike the above cases, the GOI strips are confined by insulator layers during the growth procedure. Therefore, an investigation of the change of shape of the strips during growth is necessary. To examine the difference in shape between the wide and narrow strips, we obtained cross sectional SEM images of two Ge strip grown with an initial thickness of about 55 nm and widths of about 0.625 μm and 0.15 μm. These are shown in Figs. 4.15 and 4.16, respectively. In the wider strip, we can see that the edge has become rounded while the surface has remained flat. There is a slight change in thickness which could be due to shape change by surface tension.

However, the flat top surface means the cap is hard enough to contain the melt and prevent agglomeration. On the other hand the shape of the 0.15 μm wide strip appears significantly different from the wider strip. Here we observe from the cross
sectional SEM image that the initially rectangular strip has changed into an almost cylindrical cross section. In this case also, slight change in thickness is seen. This difference in shape between wide and narrow strips can have a significant effect on the generation and relaxation of strain in these structures.

Fig. 4.15 Cross sectional scanning electron micrographs of a ~0.625 μm wide (thickness = ~60 nm) strips showing rounded edges and flat surface.

Fig. 4.16 Cross sectional scanning electron micrographs of a ~0.15 μm wide (thickness = ~65 nm) strips showing overall rounded surface.
The above observations indicate that while the top and bottom surfaces are bound by insulator confinement, the side edges are not tightly bound and can be considered as free surfaces. Based on this observation, we can now explain how the strain relaxation mechanism differs between narrow and wide strips. To better illustrate the changes in the shape of wide and narrow strips as they go from the amorphous \((a\text{-Ge})\) through the liquid \((l\text{-Ge})\) and finally to the crystalline \((c\text{-Ge})\) form, are shown in Fig. 4.17. The \(a\text{-Ge}\) strips are fabricated with a square cross section as shown in the figure. When the Ge is melted during the RTA process, it goes through a volume contraction of about 5.2\%\(^{[14]}\). Also, because of the surface tension of the liquid Ge, the strips try to acquire a rounded shape. Although the capping confinement prevents it from acquiring a circular shape, the side edges are free to do so as they are not restricted by insulator due to the volume contraction. However, the final shape of the liquid Ge can acquire greatly depends on the width and thickness of the initial strips. The shape acquired by the Ge melt is maintained during solidification. Now the free side edges created in the molten state plays a significant role in releasing the stress generated in the lattice from the Si concentration gradient. It can be thought that the stress near the edges is released by a lateral expansion or shape change made possible because of the free space. The volume of the strip over which the stress is released by such shape change can be assumed to be proportional to the surface area of the free edge.
Fig. 4.17  Illustrative explanation of shape and volume change of Ge strips from the amorphous state to single-crystalline state through melting growth process.
On the other hand near the center of the strips where a supposedly rigid confinement is imposed by the insulator layers at the top and bottom surfaces, release of the lattice stress by shape change becomes impossible or greatly minimized. Instead, in the center regions, the stress release is facilitated by formation of dislocations.

In a wide strip with $W \gg d$, the ratio of free edge area to cross sectional area of the strip is significantly small compared to the same ration in a narrow strip where $W$ approaches $d$. Therefore, it is reasonable to assume that the primary mode of stress release differ greatly between the wide and the narrow strips and play the significant role in determining occurrence of lattice rotation. In the next section we present a model to describe the process of stress release mechanism and its dependence on Ge strip dimensions.

4.6 Strain Relaxation Model

In section 4.2, we have discussed how that the rotational phenomena are directly related to defect formation in the crystal structure. We also calculated the minimum density of defect to produce the amount of rotation seen in some of the cases. We have also discussed how the rotation is dependent on both width and thickness of the Ge strips. Results were shown that indicate that the amount of rotation, i.e. defect formation, is enhanced by Ge strip thickness reduction. It was also shown that the rotation by defect formation is minimized or fully suppressed by scaling the width of a Ge strips closer to its thickness. We account for these effects in the strain relaxation model here.
The strain relaxation model for Ge strips grown by the rapid melting growth process is presented in Fig. 4.18. The model applies the necessary boundary conditions on the growth front during the crystallization process. The top and bottom surfaces of the strips are assumed to be confined by rigid insulator layers that prevent any shape change in this direction. It is also assumed that there is enough free space...
at the side edges that they can be considered as free surfaces. The side edges are shown to be in a rounded shape in accordance with the observation (Figs. 4.15 and 4.16).

![Strain relaxation model](image)

Fig. 4.19 Strain relaxation model showing effects of thickness reduction on the lattice stress ($\sigma$) profile in the growth front cross section of a Ge strip. The thickness reduction shifts the critical slip length $r_{\text{slip}}$ closer to the edge.

The strain generated from Si diffusion in the Ge strip is compressive in nature due to the smaller lattice constant of Si (0.5431 nm) compared to Ge (0.5658 nm). Since we are assuming rigid confinement by the capping layers for the sake of simplicity, the stress resulting from the strain gradient in the central region of the
strip can be assumed to obtain a uniform value $\sigma_{\text{sat}}$ along the cross section, such that $\sigma_{\text{sat}}$ above a certain critical value would initiate the generation of dislocations in the crystal. If we ignore, for the moment, stress released by the generation of dislocations, the stress profile can be shown as that in Fig. 4.16, where it falls off gradually as we move closer to the edge. This fall off is from the relaxation of strain by a lateral expansion of the strip volume in regions near the free edge aided slip along the Ge/insulator interface. The distance from the edge into the strip where the deformation can occur is termed as $r_{\text{slip}}$. Therefore, it can be concluded that in the area covered by $2 \times r_{\text{slip}}$ of the width, strain relaxation is caused by shape change in the crystal and thereby no dislocation formation occurs in this area. On the other hand, in the width of $(W - 2 \times r_{\text{slip}})$ of the strip, strain relaxation should occur by the formation of dislocations.

Now $r_{\text{slip}}$ can be reasonably thought to be proportional to the area of free surface and consequently proportional to the thickness of the strips. Reduction of the strip thickness causes a corresponding reduction of the free surface area and moves $r_{\text{slip}}$ closer to the edge. This situation is illustrated in Fig. 4.19 where the strip width is reduced compared to the illustration of the previous figure. The reduction of $r_{\text{slip}}$ means that a greater area of the cross section is now subject to strain relaxation by dislocation generation. Thereby, an enhancement of lattice rotation is expected in this case. This corresponds well with the observed aggravation of rotation in thin (50 nm) Ge strips compared to thick (100 nm) strips.
Fig. 4.20  (a) Strain relaxation model showing effects of strip width reduction such that the half width R approaches the critical slip length \( r_{\text{slip}} \). (b) relation of normalized lattice stress with strip width at \( d \) and \( r_{\text{slip}} \) values corresponding to thin (111)-GOI strips along <112>.

\[
\sigma(r) \propto \frac{W - 2r_{\text{slip}}}{W}
\]

\( d = 50 \text{ nm} \)
\( r_{\text{slip}} = 0.1 \mu\text{m} \)
Now let’s consider what happens when the strip width is reduced at a given thickness. Since in this model $r_{\text{slip}}$ is considered constant at a given strip thickness, the narrowing of strip width while keeping the thickness constant will move the $r_{\text{slip}}$ areas on the two side edges closer. This results in a reduction of the area where strain relaxation can occur by dislocation generation. The cross sectional geometry and the expected stress profile in such a case is illustrated in Fig. 4.20(a) with the assumption that $r_{\text{slip}}$ approaches the half width (R) of the strip. The plot of Fig. 4.20(b) shows the dependence of the normalized stress on the strip width. In limit $r_{\text{slip}} \to R$, the free surface to cross sectional area ratio is the maximum and strain relaxation by shape change is possible in the entire area. As a result, defect formation from the lattice strain is greatly reduced with the corresponding suppression of lattice rotation.

4.7 Summary

Detailed analysis of crystal characteristics was performed to understand the physical process behind the observed crystal misorientation and its suppression by strip width scaling. The progressive lattice misorientation along the length of GOI strips clearly indicates that the high density defects are generated during the lateral crystallization process. It was shown that the underlying physical process of lattice rotation is the same regardless of the observed growth orientation dependence. The uniaxial rotation about the $<110>$ or equivalent axes seen in the strips made it possible to calculate the density of geometrically required dislocations in the lattice. Through the establishment of a direct correlation between the Si concentration
gradient and rotation gradient, it was shown the primary cause of lattice rotation is lattice strains generated from the Si concentration gradient. However, the Si concentration gradient was found not to be dependent on strip width. A comprehensive strain relaxation model based on previous reports and current observation was proposed, which accurately explain the observed trend in lattice misorientation and its dependence on strip geometry. It was shown that in wide ($W \approx 1 – 2$ μm) strips lattice strain is primarily relaxed by defect generation at the growth front and is manifested as progressive lattice misorientation. On the other hand, the geometry of narrow strips ($W \leq 0.5$ μm) allows stress release occur by shape change of the crystal along the free edges of the strips, thereby minimizing defect formation or misorientation.
References


Chapter 5

Conclusions

With the view to develop a new material processing technology for next generation large scale integration (LSI), the nanofabrication and crystal orientation stabilization of Ge-on-insulator (GOI) structures by rapid melting growth (RMG) process has been investigated and presented in this dissertation. This chapter summarizes the major findings of this work.

In the last few years, the lateral rapid melting growth technique has been shown to be effective in fabricating high crystal quality GOI thin films on Si substrates. The previous works with this technique successfully demonstrated the growth of chip length (~1 cm) 100 nm thick GOI strip structures with feature width 3–5 μm. In order to implement this method in advanced LSI fabrication process, it was necessary to investigate in detail the characteristics on nano-structured GOI grown by the rapid melting process. Also, because of the orientation dependent mobility in Ge n-MOSFETs, it was necessary to find a way to stabilize the rotational growth seen in (111) oriented GOI.

In order to grow nano-structured GOI, the nanofabrication process for RMG was developed and presented in chapter 2. Successful scaling of GOI micro-strips to nano-strips with small thickness \((d \leq 50 \text{ nm})\) and width \((W \leq 0.5 \text{ μm})\) was
demonstrated, which is a significant improvement over previously reported results. The current work was limited by the resolution of the lithographic process, however it is expected further shrinkage of nano-strips is possible. In the course of the work on thickness and width shrinkage, a strong dependence of growth characteristics on strip dimensions was observed. It was found that stability of crystal orientation becomes weak with reduction of Ge layer thickness. In the growth of thin \((d = 50 \text{ nm})\) 2 \(\mu\text{m}\) wide Ge strips, progressive misorientation of Ge crystal lattice from the seed orientation was noticed. On the other hand, shrinking the strip width appeared to provide gradual improvement of orientation stability. Maximum instability was seen in the widest (2 \(\mu\text{m}\)) strips, while scaling to 1 \(\mu\text{m}\) width reduced both frequency and magnitude of misorientation. For the 50 nm thick Ge strips with (100) orientation, completely stable growth was achieved at the strip width of 0.5 \(\mu\text{m}\). The trend indicates that crystal misorientation at any Ge layer thickness can be suppressed by narrowing of the strips. The above observation represents a critical feature in the growth of thin GOI by RMG.

Consistent crystal quality was observed regardless of strip dimensions as Raman spectrum analysis showed the FWHM values of Ge—Ge vibration mode peaks are very close to that of single crystal Ge wafers.

The observation of orientation stabilization by strip narrowing in (100) GOI leads us to believe that this effect is a general feature of rapid melting grown GOI and can be applied to stabilize the lattice rotation previously observed in the growth of thick \((d = 100 \text{ nm})\) GOI from (111) seed along \(<112>\) direction. The results of this effort were presented in chapter 3. Detailed investigations were performed on the
effects of strip thickness and width reduction on the growth characteristics of (111) GOI with growth along different crystallographic directions. It was found that the effects presented in chapter 2 were indeed general characteristics of rapid melting grown GOI. In addition a strong dependence of the stability effects on crystal orientation was found. The results presented in chapter 3 show that GOI growth form (111) seed along <112> direction in most vulnerable for misorientation. Here further deterioration of orientation stability occurred with thickness reduction. Nevertheless, Stabilization of the growth orientation was possible by strip narrowing. Whereas rotation free (111) growth in thick \((d = 100 \text{ nm})\) GOI strips was achieved at 0.5 \(\mu\text{m}\) strip width, stabilization of thin \((d = 50 \text{ nm})\) strips required further narrowing to 0.2 \(\mu\text{m}\) for complete stabilization. Also, quite similar to (100) oriented GOI, misorientation was induced in thin \((d = 50 \text{ nm})\) (111) oriented GOI strips along <011> direction, where stable growth was obtained by narrowing the strips to 0.5 \(\mu\text{m}\).

To understand the physical process behind the observed crystal misorientation and its suppression by strip narrowing, detailed analysis of crystal characteristics was performed and a model to explain the phenomenon was presented in chapter 4. The progressive lattice misorientation along the length of GOI strips clearly indicates that the high density defects are generated during the lateral crystallization process. Examination of the crystal orientation maps obtained from electron backscatter diffraction (EBSD) analysis revealed that even though the clear dependence on crystal orientation and growth directions, the physical process of lattice rotation is the same. The correlation of rotation to defective areas of the strips was shown. It
was found the lattice rotation occurs about the $<110>$ axis whether it is the growth direction or the transverse direction. This uniaxial rotation made it possible to calculate the density of geometrically required dislocations in the lattice.

The Si concentration gradient resulting from the diffusion of Si from the seed area during the melting growth process was found to be the primary cause of lattice rotation. However, the Si diffusion was shown not affected by strip width narrowing and could not explain the suppression of rotation in narrow strips. In order to explain the suppression of lattice rotation by strip width narrowing, a comprehensive model describing the effects of lattice strains at the growth front of Ge strips during crystallization on the induction of lattice misorientation and its dependence on strip dimensions were presented. Here, the lattice strain is generated in the Ge crystal due to Si diffusion. It was shown by this model that the misorientation appeared as a result of the difference in the dominant strain relaxation mechanism between wide and narrow strips. The dominant mode of strain relaxation in wide ($W \approx 1 – 2 \mu m$) strips is defect formation in the as crystallized growth front as it progresses along the length of the strips and is manifested as progressive lattice misorientation. On the other hand, in narrow strips ($W \leq 0.5 \mu m$) the stress release occurs mainly through shape change of the crystal along the free edges of the strips, thereby minimizing defect formation or misorientation.

These findings are expected to play a significant role in the realization of next-generation LSI by facilitating the integration of Ge with the Si CMOS process.
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