A Multi-Performance Processor for Low Power Embedded Applications

Oyama, Yuichiro
Kyushu University

Ishihara, Tohru
Kyushu University

Sato, Toshinori
Kyushu University

Yasuura, Hiroto
Kyushu University

出版情報：Proceedings of Cool Chips X, pp.138-138, 2007-04-19
バージョン：
権利関係：

A Multi-Performance Processor for Low Power Embedded Applications

Yuichiro OYAMA Tohru ISHIHARA Toshinori SATO Hiroto YASUURA

Kyushu University
3-8-33, Momochihama, Sawara-ku, Fukuoka, JAPAN, 814-0001

Abstract *– This paper proposes an energy efficient processor which can be used as a design alternative for the dynamic voltage scaling (DVS) processors in embedded system design. The major advantage over the DVS processors is a small overhead for changing its operating voltage. The supply voltage and the clock frequency can be changed in a few clock cycles with low bounce noise in power and ground lines.*

1. Introduction

Dynamic voltage scaling (DVS) is one of the most popular approaches for reducing the energy consumption of processors. In past years, a lot of DVS processor architectures have been proposed. However, only a few of them have been used in embedded systems. One major reason is that many DVS processors involve large mass production cost including test cost, design cost and the cost of on-chip DC-DC converters. The other reason is a delay overhead for dynamically changing the supply voltage and the clock frequency. In this paper, a new processor which can be used as a design alternative for the DVS processors is proposed. An overview of the architecture, a design flow and a power management strategy for the processor are presented in the following sections.

2. Multi-Performance Processor

The proposed processor core consists of multiple clusters [1] and scalable set-associative cache memories as shown in Figure 1. The clusters are functionally equal to each other but use different supply voltages. Therefore, speeds and energy consumptions are different from each other. Only a single cluster is activated at a time and the other clusters are deactivated using power gating and/or clock gating techniques. The cluster which should be activated and associativity value of the cache memory can be changed at boot time or run time by software running on the processor core. If designers need more run-time parallelism, we can easily implement a chip multi-processor (CMP) by integrating some of our processor cores on a chip.

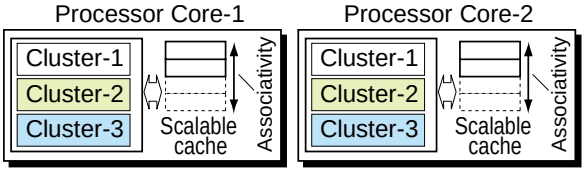

Figure 1. An Example of Multi-Performance Processor

3. Design Flow and Synthesis Result

Figure 2 shows synthesis results of clusters optimized for 0.8V, 1.0V and 1.2V voltage supplies, respectively. A 90nm CMOS process technology of ASPLA Corp. and a Media embedded Processor (MeP) of Toshiba Corp. are used for the experiment. Our processor can be easily synthesized using conventional design flow without taking care of multiple timing constraints which should be considered in conventional DVS processor design.

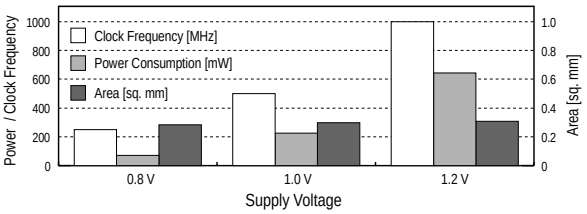

Figure 2. Synthesis Results of Clusters

4. Power Management

The basic strategy of power management for the multi-performance processor is shown in Figure 3. A software task starts running on the lowest power cluster and gradually shifts up its operating speed. For reducing the bounce noise of ground and power lines, the supply voltage of clusters should be powered on slowly. Even if it takes several thousands of cycles to worm-up the next used cluster, our technique can hide this overhead by powering on the cluster prior to using it.

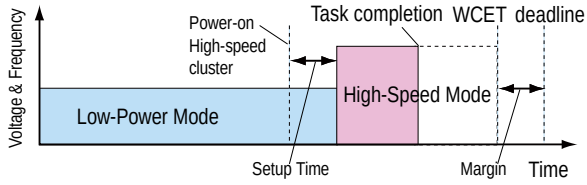

Figure 3. Power Management for Our Processor

5. Summary

More detailed architecture descriptions, power management strategies and experimental results will be presented at the poster presentation.

Acknowledgement

This work is supported by Toshiba Corporation and VDEC, the Univ. of Tokyo with the collaboration of STARC, Panasonic, NEC Electronics, Renesas Technology, and Toshiba. This work has been also supported by CREST project of JST and the grant-in-aid for scientific research. We are grateful for their supports.

Reference

[1] T. Sato and A. Chiyonobu, “Multiple Clustered Core Processors”, in Proc. of SASIMI, pp.262-267, Apr., 2006.