A High Precision Current Source Circuit by Means of Switched-Capacitor and PLL for BOST

Li, Tianmao

Department of Electronics, Graduate School of Information Science and Electrical Engineering, Kyushu University : Graduate Student

Tashiro, Hiroyuki 九州大学大学院システム情報科学府電子デバイス工学専攻

Uchihata, Haruki 九州大学大学院システム情報科学府電子デバイス工学専攻

Kuroki, Yukinori 九州大学大学院システム情報科学研究院情報エレクトロニクス部門

https://doi.org/10.15017/1654539

出版情報:九州大学大学院システム情報科学紀要.13(1), pp.19-23, 2008-03-26.九州大学大学院シス テム情報科学研究院 バージョン: 権利関係:

A High Precision Current Source Circuit by Means of Switched-Capacitor and PLL for BOST

Tianmao LI* , Hiroyuki TASHIRO* , Haruki UCHIHATA* and Yukinori KUROKI**

(Received December 15, 2007)

Abstract: In this work, a high precision current source circuit by means of switched-capacitor and PLL(phase-locked loop) for BOST(build-out-self-test) is presented. A relationship between the reference current value and switching-frequency is analyzed to improve the precision of current source circuit. The proposed circuit operates under 3.3V supply with a 100μ A reference current source according to Hspice simulation and shows a precision less than 0.8%.

Keywords: Build-out-self-test(BOST), Switched-capacitor, Phase-locked loop(PLL)

1. Introduction

BOST (Built-Out-Self-Test) is an important method for testing a system LSI, in which a part of testing signals are provided from the chip on a load board of an LSI tester ¹⁾. Since BOST can put many test units on the performance-board, and achieve high speed, low cost measurement, it will be widely used for test system. 10000 LSI can be tested at the same time by using this technology. Each current source, which embedded with the BOST chip, will be proofed when the power set in "ON". This proof operation's requirement is aimed to complete in 1 minute, in other words, one chip must be proofed in 6m second.

High precision current source is demanded for BOST technology. The basic idea is use V (voltage) and R (resistor) to make the current source. About the part of "V", we can use the conventional bandgap circuit provide a definite voltage with 0.24% precision under the -50° C $\sim +120^{\circ}$ C. The resistor's value variation at present the manufacture level is nearly $\pm 30\%$, it is too big and not sufficient for the high precision demand. In systems where a precise clock frequency is available, the resistor R can be replaced by a switched-capacitor equivalent to achieve a somewhat higher accuracy. The capacitor's variation is less than R nearly 15%, but its accuracy is also not enough.

In this paper, a high precision current source circuit by means of switched-capacitor and PLL was presented. The proposed circuit's specification is 3.3V power supply with a 100μ A reference current source.

****** Department of Electronics

2. Architecture

A conventional voltage-current conversion by means of a switched-capacitor resistor ²) was shown in Fig.1. An average resistance which equals to $1/C_s F_{ck}$ was established between the source of M1 and ground, where F_{ck} denotes the clock frequency. Capacitor C_B is added to shunt the high-frequency components resulting from switching to ground. Since the temperature coefficient of $capacitors(-52ppm/^{\circ}C)$ is much smaller than that of resistors $(-102ppm/^{\circ}C)$, this technique provides a higher reproducibility in the bias current and transconductance. Because the + and - terminal's voltage of Amp is same, the voltage value of node A will be fixed by the reference voltage V_{ref} . If the switching frequency can be regulated when the I_{ref} at a wanted value point, a high precision current source will be achieved by using this architecture.



Fig. 1 A conventional voltage-current conversion by means of a switched-capacitor resistor.

The switched capacitor which using a reference current source was shown in **Fig.2**. We use PMOS

^{*} Department of Electronics, Graduate Student

and NMOS pair to replace the switch S_1 and S_2 , so the MOS's capacitor C_{DS} and C_G must be considered. Because the target value of V_0 is 1.25V, and the reference current is 100μ A, from the equation, R = V/I, we must product a 12.5K Ω resistor. Making the resistance, capacitor $C_1 = 10pF$ is set in this design, from the equation, $R = 1/C_s F_{ck}$, a 8MHz clock signal should be supplied to Switched-Capacitor part. The circuit operation is described as follows (the approximate waveform of V_0 and V_1 were shown in **Fig.3**): After the discharging of C_1 , switch S_1 become on at period (1), in this time S_2 is OFF, and a part of the stored charge in C_0 will be infused into the C_1 to get a balance state. So we can get

$$V_{01+} = V_{11+} = \frac{C_0 + C_{DS}}{C_0 + C_1 + 3C_{DS} + C_G} V_{01-} \quad (1)$$

where V_{01+} and V_{11+} means the voltage value at the eve of V_0 and V_1 , respectively. V_{01-} means the value just after the V_0 . Here, the resistor of switch is ignored.

In the balance state (period (2)), C_0 and C_1 are charged by current source, and their voltages V_1 and V_0 will increase. So far V_1 equals to V_0 . Therefore V_0 is as follows

$$V_0 = V_{01+} + \frac{I}{C_0 + C_1 + 3C_{DS} + C_G}(t - t1) \quad (2)$$

At period (4) S_1 become OFF (S_2 is ON), only C_0 is charged,

$$V_0 = V_{03+} + \frac{I}{C_0 + C_{DS}}(t - t3)$$
(3)

From (1), (2) and (3), we get the voltage of V_0 is

$$V_{0_{peak}} = \left(\frac{2}{\overline{C_1 + 2C_{DS} + C_G}} + \frac{1}{\overline{C_0} + C_{DS}}\right) \cdot \frac{I}{2f}$$
(4)

Ignoring the C_{DS} and C_G , equation (4) become simple,

$$V_{0_{peak}} = \frac{I}{C_1 f} + \frac{I}{2C_0 f}$$
(5)

In this design, C_1 and f are constant value, so V_0 's variation is only related with C_0 . From equation (5), the precision of V_0 can be improved by adjusting the value of C_0 .

The block diagram of clock decision's method for each chip was shown in **Fig.4**. The overall system



Fig. 2 The switched capacitor proof circuit which using a reference current source.





structure consists of three major parts: a switchedcapacitor proof part, a memory storage unit and a PLL circuit. This process can be considered as a two step work. At first, the switched-capacitor frequency is proofed by using the reference current source, and make the resistor's value equal to $12.5k\Omega$. In the second step, the stored frequency value in the memory part is supplied to drive the PLL circuit, which supply a clock into the proofed switched capacitor. The clock2 will be used to proof the C(capacitor)'s variation on each BOST chip in high precision.

The block diagram of generating switching frequency by means of reference current source is shown in **Fig.5**, which consists of four parts: a switched-capacitor resistor and current source, the V-bias circuit, the VCO and a differential amplifier. Because there no other phase variations exist



Fig. 4 The block diagram of clock decision's method for each chip.

in this closed loop except differential amplifier, we have the necessary only to observe the stability of the differential amplifier part. The frequency response of the proposed amplifier is shown in **Fig.6**. The PM(phase margin) is nearly 35°. So it does not oscillate in the closed feedback loop. When the switching frequency is 8MHz, the input(V_0) and output(V_{cont}) transient response of the differential amplifier are shown in **Fig.7**. Both of them are converged in a little variation range. The output V_{cont} 's variation decide the precision of the circuit.



Fig. 5 The block diagram of generating switching frequency by means of reference current source.

Figure 8 shows the PLL circuit, which is composed of six main components: phase/frequency detector (PFD), low-pass filter (LPF), VtoV circuit, VCO(II), counter and scaler. The purpose of the charge pump type PFD is to convert the logic states of the PFD into analog signals suitable for regulating the voltage-controlled oscillator (VCO). In this design, a passive RC filter (attached outside of the chip) is used to smooth the output voltage of the PFD, and to provide the VtoV circuit a DC signal having the least ripple. Capacitor C_2 integrates the



Fig. 6 Frequency response of the proposed differential amplifier.



Fig. 7 The input-output transient response of the differential amplifier.

CP current, R_1 and C_1 reduce the ripple on the DC signal to VtoV circuit. About the parameters of the R_1, C_1 , as the reference ³⁾, the optimum conditions is the $C_1 = 8 * C_2$. The product of R_1 and C_1 are set to larger value than the repletion time of the PLL reference signal. The VCO(II) is composed of 32 basic delay cells(starved-current inverter) and one inverter. The VtoV circuit is inserted between the LPF and the VCO, which generates two bias voltages V_{cp} and V_{cn} , then provides them to the VCO. In this design, scale circuit is used to replace the conventional divider. Two counter (consists of 9 scaler circuit) and a DLATCH circuit constitute a programmable counter through some logic calculation. The upper counter and the DLATCH's output signals will be compared by means of 9 EXOR, 9 input NAND circuits and 1 OR circuit. The circuit will be reset if two compare signals are same. The logic relationship of V_{quartz} , V_{FB} (PLL's reference signal and feedback signal), STOP signal (a signal for stop reading of standard current, supplied from outside of the chip), VCO(I) and VCO(II)'s oscillate signals and Reset signal (reset the counter, at the rising edge of V_{quartz}) are shown in **Fig.9**.



Fig. 8 The diagram block of PLL circuit (include the programmable counter).



Fig. 9 The logic relationship of V_{quartz} , V_{FB} (PLL's reference signal and feedback signal), STOP signal (a signal for stop reading of standard current, supplied from outside of the chip), VCO(I) and VCO(II)'s oscillate signals and Reset signal (reset the counter, at the rising edge of V_{quartz}).

3. Simulation Results and Discussions

The proposed circuit was simulated with the TSMC018 process model by Hspice. The performances of the switched capacitor circuit, PLL circuit are verified through the simulation.

The aim of this design is to achieve high precision by setting the switching frequency, so we must predict the variation of this frequency. Since the switching frequency was generated by VCO(II), it is necessary to observe the V_{cont} (control voltage). The variations of the input and output signal of differential amplifier are shown in **Fig.10** and **Fig.11** when we set the switching frequency equal to 8MHz and C_0 equal to 1000pF. From the simulation results, we get the variations are 10mV and 1mV, respectively.



Fig. 10 The simulation results of differential amp's input signal(supplied by SC).



Fig. 11 The simulation results of differential amp's output signal(provided to VCO(I)).

More than 45MHz of VCO(I) tuning range is achieved for a $0 \sim 3.3V$ control voltage variation (**Fig.12**). The important parameter, K_{vco} (gain of the VCO) equals 64.15MHz/V when the control voltage is $0.9V \sim 1.5V$. Back to the V_{cont} , since the variation of V_{cont} can be converged in 1mV range, it means the switching frequency's variation is only 64.15KHz. $(1mV * K_{VCO})$. Because the clock1's value is 8MHz, the precision of this circuit is less than 0.8% and achieved the goal of 1% precision for BOST current source. Another important point is C_0 , since it is attached outside to the board, we can adjust the circuit precision by changing its value.

4. Conclusion

In this paper, a high precision current source circuit by means of switched-capacitor and PLL for BOST has been designed in CMOS process. By observing the $V'_{cont}s$ (control voltage of the VCO) variation and K_{VCO} (gain of VCO) of the Switched-



Fig. 12 VCO(I) tuning range.

capacitor circuit, we get the proposed circuit can achieve a precision less than 0.8%. It is suitable for

BOST current source which precision demand is at least 1%.

References

- Hisayoshi. Hanai, Shinji. Yamada, Hisaya. Mori and Eisaku. Yamashita Built-out self-test (BOST) for analog circuits in a system LSI test solution to reduce test costs, Proceedings of the 10th Asian Test Symposium, 19-21 Nov. 2001 pp. 460
- Behzad Razavi, Design of Analog CMOS Integrated Circuit McGraw-Hill Series in Electrial and Computer Engineering, pp.392-393
- Akira. Matuzawa and Sirou. Dosho, CMOS Analog Design Technology, System LSI Center, Co Ltd