DEVELOPMENT OF FBAR BASED ULTRA LOW PHASE NOISE RADIO FREQUENCY OSCILLATOR

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Abstract

In future generation wireless communication systems, the demand of low cost and high performance integration RF transceivers is rapidly growing. High performance oscillators such as low phase noise frequency reference and voltage controlled oscillators (VCO) are the main issues to satisfy the increasing requirement of RF transceivers.

In this thesis, low phase noise monolithic FBAR oscillators are realized by employing high Q-factor FBAR resonators, which have the potential to replace the quartz crystal oscillators as frequency reference and replace the normal Ring-VCO and LC-VCO as local oscillators of RF transceivers. The contributions of this thesis can be divided into three parts. The first part is that a low phase noise monolithic Pierce FBAR-DCO and an inverter based FBAR-DCO are designed, which demonstrated the possibility of monolithic FBAR oscillator and the over 20 dB improvement of phase noise. The second part is that in the design of cross-coupled FBAR-VCO, the novel methods based on capacitor or series inductor-capacitor are proposed to solve low frequency instability; the novel phase noise optimization method based on considering the effect of transistors’ size on the Q-factor of FBAR is proposed, which makes the proposed FBAR-VCO has a phase noise below -150 dBC/Hz at 1 MHz offset frequency; the possibility of a multiband VCO using FBAR-VCO as a core circuit has been demonstrated. The third part is that instead of LC-VCOs in the traditional PLL, we employ the presented cross-coupled FBAR-VCO to design an FBAR-VCO based PLL. A new charge pump design based on complementary logic switches is adopted to reduce the mismatch current and the current noise. The proposed PLL proves the possibility of FBAR-VCO based PLL and the simulation result shows the phase noise of FBAR-VCO is further improved.
Chapter I
Introduction

1.1. Background

Wireless communication applications such as mobile, wireless sensor network and wireless local area network, have an explosive growth in recent years. With the rapid growth, the requirement of low cost, high performance and high integration radio frequency (RF) integrated circuits (RFIC) is also increasingly higher. In the past decades, complementary metal-oxide-semiconductor (CMOS), a low cost technology for constructing integrated circuits (IC), has been employed by RFIC researchers and a number of high integration RFICs such as RF transceivers [1-3] which integrate phase lock loop (PLL) or voltage controlled oscillators (VCO), filter, mixer, power amplifier (PA), low noise amplifier (LNA), variable gain amplifier (VGA), analog to digital converter (ADC), digital to analog converter (DAC), and have both transmission and receiving functions, as shown in Fig. 1.1, have been designed successfully.

Fig. 1.1 Block of CMOS transceiver
However, despite the characteristics of low cost, high integration, CMOS technology also reveals thin metals, high loss substrate disadvantages, which brings challenges in the design of high quality (Q) factor inductors and filters, low phase noise VCO, and high efficiency PA.

In recent years, micro electro-mechanical systems (MEMS) technology has become new solutions to compensate the demerits of CMOS. High performances RF-MEMS devices, such as RF-MEMS switches [4-6], variable capacitors [7-9], filters [10-12], and resonators [13-15] have been reported and several approaches for integrating MEMS with CMOS [16-18] have been published, which makes monolithic MEMS-CMOS RFIC possible and become the trend of development of RFIC in the future.

1.2. Motivation

Oscillators which are used to generate local oscillation signals such as voltage controlled oscillator or reference frequency signals such as quartz crystal oscillators are one of the most important building blocks of RF transceivers. To realize a high performance RF transceiver, a high accuracy frequency reference and a VCO which has the features of low phase noise, low power consumption and small area are required. For frequency reference, quartz crystal oscillators are usually adopted as the low phase noise and high accuracy. But the frequency of quartz crystal oscillators is very low and they cannot be integrated because of the incompatibility of the silicon substrate and the large size of quartz crystal. For VCOs’ design, two main topologies, which are usually adopted, are ring and inductor-capacitor (LC). Ring VCOs are composed of a series of back-to-back-connected inverters, and LC-VCOs employ CMOS transistors as driving circuits and
oscillate at the resonance frequency of inductor-capacitor based resonator. However, since the low quality (Q-) factor of on-chip inductors, the phase noise of LC-VCOs is always very poor, normally about -120 ~ -130 dBc/Hz at 1 MHz offset frequency [19, 20]. For ring VCOs, because no resonator is used, the phase noise is even as poor as -90 ~ -100 dBc/Hz at 1 MHz offset frequency [21, 22]. In practice, to overcome the poor phase noise problem, when designing RF transceivers, researchers always employ low phase noise quartz crystal oscillators as frequency reference and make up PLL based frequency synthesizers which can generate GHz frequency signals by multiplying the reference frequency by factor $N$ [23]. By PLLs, although the in-band phase noise can be improved by the low phase noise frequency reference, the out-band phase noise is still poor and spurious caused by reference frequency is not easy to suppress. Thus, it is necessary to find other solutions to create a kind of oscillators which have low phase noise and is able to be integrated with CMOS technology.

Film bulk acoustic resonators (FBAR), a kind of MEMS resonator, have very high estimated Q-factor around 1000 or even more [24-26]. Using them to replace the low Q-factor on-chip inductors to design low phase noise GHz-range oscillators, has been of great interest and some FBAR-oscillators which have low phase noise around -140 dBc/Hz at 1 MHz offset frequency are able to obtain by some published papers [24-26].

Based on the introduces above, it can be shown that FBAR-oscillators have the potential to satisfy the low phase noise and integration requirement, but the challenges to design FBAR-oscillators are multi-frequency, differential output, the further improvement of phase noise, low frequency instability and monolithic integration. The low phase noise potential and those challenges give the motivation for this research.
1.3. Research Objective

The first objective of this research is to design a low phase noise FBAR based digital controlled oscillator (DCO) using for 2.4GHz frequency. The proposed designs employ Pierce oscillator based architecture and inverter based architecture.

The second objective is to design a low phase noise differential output FBAR-VCO operating at 1.9 GHz and a low phase noise multiband FBAR-VCO for 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz. The designs use cross-coupled architecture and extend oscillation frequency by divider and multiplier.

The third objective is to design a 1.9 GHz FBAR-VCO based PLL to further improve the in-band phase noise of FBAR-VCO.

1.4. Thesis Organization

This thesis is organized as follows. In Chapter II, in the first, the basic of FBAR resonator is introduced. Then a brief introduction to oscillators is presented, covering basic LC-tanks, negative resistance theory, tuning method model and phase noise.

Chapter III focuses on analysis and design of Pierce FBAR-DCO and inverter architecture based FBAR-DCO. Circuit’s analysis based on oscillation condition and post-layout simulation results are discussed.

In Chapter IV, the design of cross-coupled architecture based FBAR-VCO and multiband FBAR-VCO is explained with their specifications such as oscillation frequency and low phase noise. Post-layout simulation results are provided.
In Chapter V, the design of FBAR-VCO based PLL is explored. Each part of PLL including phase frequency detector (PFD), charge pump (CP) and divider has been designed, and the simulation of phase noise has been completed.

Finally, summarizes the contributions of this research, and suggests future research in Chapter VI.
Chapter II
FBAR Resonator and Oscillator Fundamentals

2.1. Introduction

An FBAR-oscillator mainly consists of two parts: FBAR resonator and CMOS active circuit. Thus, in this chapter, firstly the structure and equivalent circuit of FBAR resonator is described briefly. Then the oscillator fundamentals included Barkhausen criteria, negative resistance theory, frequency tuning methods and phase noise model are introduced.

2.2. Review of FBAR Resonators

Micro-electro-mechanical system (MEMS) resonators with hundreds of micrometers sizes, have a number of eigen frequencies and transduction mechanisms. Transduction mechanisms cause MEMS resonators to vibrate, if appropriate excitation signal which is of a frequency close to one of the eigen frequencies of MEMS resonators is input. According to the different implement approaches, the micromechanical and the acoustical, MEMS resonators can be divided into two categories. FBAR resonators are one kind of acoustical wave resonators.

2.2.1. Structure of FBAR Resonators

FBAR resonators are composed of one piezoelectric film and two metal electrodes, which employ metal-piezoelectric-metal structure, as shown in Fig. 2.1. FBAR is fabricated above Si substrate and two metal electrodes are always made of aurum (Au) or
chromium (Cr). For the piezoelectric layer, many piezoelectric materials such as aluminum nitride (AlN), zinc oxide (ZnO), or cadmium sulfide (CdS) can be explored. Considering the high acoustic wave velocity, low temperature coefficient and the possibility of CMOS compatibility, AlN is chosen in this research. The air gap is used to reduce the electromechanical coupling to the substrate to obtain high Q-factor.

![Structure of FBAR](image)

**Fig. 2.1 Structure of FBAR**

### 2.2.2. Equivalent Circuit of FBAR Resonators

The equivalent circuit of FBARs can be represented by the Butterworth-Van-Dyke (BVD) model which is also suitable for crystal resonators and other MEMS resonators [27]. It is shown in Fig. 2.2 that the BVD model has two parallel branches which are called the static capacitance arm and the motional arm respectively. The static capacitance arm is composed of the parallel-plate capacitance $C_0$ formed between the top and bottom electrodes of FBARs while the motional branch is formed by the series motional inductance $L_m$, capacitance $C_m$, and resistance $R_m$, which relates to process-dependent parameters and material constants.
Because the two branches are connected in parallel, two resonance frequencies of FBARs, the series resonance frequency \( f_s \) and the parallel resonance frequency \( f_p \), are presented by the BVD model. The two resonance frequencies can be calculated by:

\[
f_s = \frac{1}{2\pi \sqrt{L_mC_m}} \tag{2.1}
\]

\[
f_p = \frac{1}{2\pi \sqrt{\frac{C_mC_0}{C_m + C_0} L_m}} \tag{2.2}
\]

The series resonance frequency \( f_s \) is always referred to as the resonance frequency, as the impedance at this frequency is minimized, while the parallel resonance frequency \( f_p \)
is often called the anti-resonance frequency, since the impedance at this frequency is maximum.

The parameters of BVD model can be calculate by follow [28]:

\[ C_0 = \frac{\varepsilon A}{t} \]  
(2.3)

\[ \frac{C_m}{C_0} = \frac{8k_{eff}^2}{N^2 \pi^2} \]  
(2.4)

\[ L_m = \frac{\nu}{64f_s^3 \varepsilon A k_{eff}^2} \]  
(2.5)

\[ R_m = \frac{\eta \varepsilon}{16f_s \rho A \nu k_{eff}^2} \]  
(2.6)

where \( A \) is the area of the parallel-plate capacitor; \( \varepsilon, t, \rho \) and \( v \) are the absolute permittivity, thickness, density, and speed sound of the piezoelectric material, respectively; \( N \) is the acoustic mode, and \( \eta \) is the acoustic viscosity related to the imaginary part of the wave vector; \( k_{eff}^2 \) is the piezoelectric coupling coefficient.

From the BVD model and (2.3) to (2.6), the physical constants of the process can be obtained. However, the modified Butterworth-Van-Dyke (MBVD) model [29] gives a
more realistic representation of FBARs, because it accounts for dielectric and ohm losses in the piezoelectric material and the transmission line by using resistances $R_0$ and $R_s$ respectively, as shown in Fig. 2.3. The differences between the MBVD model and BVD model are in the parallel-plate capacitance arm, $R_0$ is serially connected to $C_0$, and the two components of resistance $R_s/2$ are added, which corresponds to the bottom and top electrode line losses respectively.

At $f_p$ and at $f_s$ the MBVD model can also be simplified into a model with a single series resistance, $R_{ss}$ and a single shunt resistance, $R_{pp}$, as shown in Fig. 2.4.

Fig. 2. 4 Simplified model used only at $f_s$ (a) and at $f_p$ (b)
With the MBVD model, the impedance characteristic of FBARs can be depicted in Fig. 2.5. Thus the Q-factor at the series resonance frequency \( (Q_s) \) and the Q-factor at the parallel resonance frequency \( (Q_p) \) can be computed as:

\[
Q_s \approx \frac{f_s}{\Delta f_s} \\
Q_p \approx \frac{f_p}{\Delta f_p}
\]

(2.7)

where \( \Delta f_s \) and \( \Delta f_p \) are the -3 dB frequency widths of the impedance magnitude of FBAR at \( f_s \) and \( f_p \) respectively. From experiment, it is known that the Q-factor of FBAR is always larger than 1000 [24-26].

Fig. 2.5 Magnitude and phase of FBAR impedance
2.3. Oscillator Fundamentals

In this subsection, it focuses on discussion of the oscillation condition and the phase noise model of oscillators.

2.3.1. Barkhausen Criteria and Negative Resistance Theory

In order to keep oscillator oscillate, it is necessary to satisfy the Barkhausen criteria [30]. The Barkhausen criteria are based on feedback systems. Fig. 2.6 shows an unity-gain negative feedback system, where $H(s)$ is called the feed-forward network.

Fig. 2. 6 Unity-gain negative feedback system

Then the closed-loop gain of the system in Fig. 2.6 is

$$\frac{V_{out}}{V_{in}} = \frac{H(j\omega)}{1 + H(j\omega)} \quad (2.8)$$

If for a frequency $\omega_0$, $H(j\omega) = -1$, then the closed-loop gain approaches infinity at $\omega_0$.

Under this condition, if a little noise is input in this system, it will be amplified indefinitely and infinite output will be generated continuously which is also called oscillation. Actually, for the oscillation to begin, the condition $H(j\omega) \leq -1$ is necessary. This condition is able to resolve to the magnitude part and the phase shift part as follow:
\[ H(j\omega) = -1 \] \tag{2.9} \]

\[ \angle H(j\omega) = 180^\circ \] \tag{2.10} \]

These two conditions are called “Barkhausen criteria”.

It is worth notice that the second Barkhausen criterion (2.10) presents a frequency-dependent phase shift not a total phase shift. In Fig. 2.6, the system already produces a DC phase shift of 180° because of the negative feedback. Thus, the total phase shift is 360° not 180°.

Fig. 2. 7 (a) Damped oscillation, (b) add a negative resistance provided by active circuit to cancel the loss of \( R_p \)
All analyses above are based on feedback systems, however, in practice another theory of “negative resistance,” [31] can provide an easier way to analysis and design an FBAR-VCO. Because at \( f_p \), FBAR also can be considered an equivalent inductor-capacitor in parallel, a simple parallel LC-tank is used to describe the negative resistance theory, as shown in Fig. 2.7. If a current impulse is input in this parallel LC-tank, the response is a damped oscillation because of the loss of \( R_p \), as shown in Fig. 2.7 (a). If the loss of \( R_p \) is absolutely compensated by a negative resistance \(-R\), which is usually composed of active circuit, satisfying \(-R//R_p = \infty\), as shown in Fig. 2.7 (b), the LC-tank can oscillate indefinitely.

![Fig. 2. 8 A NMOS cross-coupled pair based negative resistance generation circuit](image)

A NMOS cross-coupled pair based negative resistance generation circuit is shown in Fig. 2.8. It can be proved that the negative resistance of the circuit in Fig. 2.8 is equal to \(-2/g_m\), where \( g_m \) is the trans-conductive of transistors. If \( R_p - 2/g_m \geq 0 \), the AC power provided by the negative resistance generation circuit is larger than loss \( R_p \), the oscillation will start and the oscillation amplitude will be increasing. When the amplitude is large enough, the transistors will be cutoff in a part of each period, which makes the loss is equal.
to the AC power provided by the negative resistance generation circuit, and make the oscillation amplitude become stable.

### 2.3.2. Frequency Tuning Method of FBAR Oscillator

It has been known from (2.2) the parallel resonance frequency \( f_p \) is decided by \( L_m, C_m \) and \( C_0 \). Therefore, the only method of changing \( f_p \) is that connecting a tunable capacitor \( C_1 \) in parallel and changing the capacitance of it, as shown in Fig 2.9. In this situation, \( f_p \) is decided by:

\[
f_p = \frac{1}{2\pi \sqrt{L_m \left( \frac{C_m C_0}{C_m + C_0} \right) / C_1}}
\]

(2.11)

![Fig. 2. 9 FBAR with tunable capacitor in parallel](image)

Normally, two methods can be used to realize the tunable \( C_1 \). The first one uses digital control logic employing a capacitor bank in which each capacitor is controlled by an NMOS switch, as shown in Fig 2.10. The capacitance is binary weighting which makes the \( N \) bits capacitor bank provide \( 2^N \) discrete frequencies.
Although the capacitor bank can provide several discrete frequencies, in many VCOs, the oscillation frequency is the linear function of the control voltage,

\[
\omega_{out} = \omega_c + K_{VCO} V_{cont}
\]  \hspace{1cm} (2.12)

where, \( \omega_c \) is the oscillation frequency when the control voltage \( V_{cont}=0 \); \( K_{VCO} \) is the gain of VCO.
In this situation, CMOS varactors are needed to be used to realize tunable $C_t$. In standard CMOS process, varactors are realized by CMOS transistors. A CMOS varactor and its capacitance-voltage characteristic are shown in Fig. 2.11. When the drain and source of transistor is connected together, the capacitance between the gate and the drain and source is changing with the control voltage.

2.3.3. Phase Noise Model of FBAR oscillator

Based on the analyses above, because at $f_p$ FBAR can be considered an equivalent inductor-capacitor-loss resistor in parallel, the phase noise model of LC oscillators is able to be used in the FBAR oscillator analyses. Assume the negative resistance generator is noise-free, thus the loss resistor is the only noise source of the circuit. Considering the thermal noise of resistor and the definition of phase noise, the phase noise of an ideal oscillator is [32]

$$L(\Delta \omega) = 10 \log \left( \frac{2kT}{P_{sig}} \left( \frac{\omega_c}{2Q\Delta \omega} \right)^2 \right)$$  \hspace{1cm} (2.13)

where, $L(\Delta \omega)$ is the phase noise at frequency offset $\Delta \omega$; $k$ and $T$ are constants; $P_{sig}$ is the oscillation power. It is shown that the phase noise is inversely proportional to the second power of offset frequency, however actually the relationship between experiment phase noise and offset frequency is much different with the ideal model, because of other noise sources such as the noise of negative resistance generator and the $1/f$ noise of CMOS. Considering these factors, Leeson proposed a famous phase noise model [32], as shown in (2.14) and Fig.2.12. In Leeson phase noise model, phase noise is separated by three regions: the $1/(\Delta \omega)^3$ region in which the phase noise is proportional to $1/(\Delta \omega)^3$; the $1/(\Delta \omega)^2$
region in which the phase noise is proportional to $1/(\Delta \omega)^2$; and noise floor. An experiment factor $F$ is used to account for the increased noise in the $1/(\Delta \omega)^3$ region, and $\omega_{1/f^3}$ is the boundary between the $1/(\Delta \omega)^2$ region and the $1/(\Delta \omega)^2$ region.

$$L(\Delta \omega) = 10\log\left[\frac{2FkT}{P_{\text{sig}}} \left(1 + \frac{\omega_c}{2Q\Delta \omega}\right)^2\left(1 + \frac{\omega_{1/f^3}}{\Delta \omega}\right)\right]$$  (2.14)

From the Lesson model, it is known that increasing the Q-factor of resonators is an effective method to improve the phase noise of VCO. That is the reason that high Q-factor FBAR resonators are employed in our design to take place of LC-tanks.

![Phase noise curve of Lesson model](image)

Fig. 2. 12 Phase noise curve of Lesson model

2.4. Conclusion

In this chapter, firstly the review of FBAR resonators including the structure and the equivalent circuit is presented briefly. Then the oscillator fundamentals included
Barkhausen criteria, negative resistance theory, frequency tuning methods are introduced. Finally, the phase noise model is presented, which makes us know that good phase noise performance is able to obtain if using high Q-factor FBAR resonators.
Chapter III
Pierce and Inverter FBAR-DCO

3.1. Introduction

In this chapter, the design and analysis of two kinds of single ended FBAR-DCO is presented. The first one is called Pierce FBAR-DCO which employs Pierce three-point architecture [33] and the second one is inverter architecture base FBAR-DCO. These two kinds of architecture have the advantages of simplicity and low power consumption and low phase noise.

3.2. Pierce FBAR-DCO

3.2.1 Pierce FBAR-DCO Design and Analyses

In this design, the parameters of the adopted FBAR are shown in Fig. 3.1. The parallel resonance frequency is 2.49 GHz and the series resonance frequency is 2.44 GHz. The parameter values can be obtained from (2.3)-(2.6). The $Q_p$ and the $Q_s$ of the FBAR, calculated by (2.7), are about 3550 and 175, respectively.

Fig. 3.1 Parameters of the adopted FBAR
The proposed Pierce FBAR-DCO is shown in Fig. 3.2. The transistor \( M_2 \) is used to generate negative resistance, and a gate bias voltage \( V_{bias} \) keeps \( M_2 \) in saturation region through a large resistor \( R_{bias} \). The bias current of the whole circuit is provided by transistor \( M_3 \), and a 5 bits capacitor bank is used to provide wide tuning range. In addition, an LC-tank based buffer is used to keep large amplitude output and prevent phase noise deterioration.

Ignoring the effect of capacitor bank and LC-tank buffer and considering all transistors as ideal transistors, the equivalent circuit of the proposed Pierce FBAR-DCO is shown in Fig. 3.3.
From Fig. 3.3, the drain current of $M_2$ is

$$I_D = V_{XY} g_m = (-I_X/(j\omega C_1))g_m$$

And then the voltage between the node X and the node Y is

$$V_{XY} = \left( I_X - I_X\frac{g_m}{j\omega C_1} \right) \frac{1}{j\omega C_1} + \frac{I_X}{j\omega C_1}$$

Therefore, the input impedance between the node X and the node Y can be obtained by rewriting (3.2) as

$$Z_{XY} = -\frac{g_m}{C_1 C_2 \omega^2} + \frac{1}{j\omega C_2} + \frac{1}{j\omega C_1}$$
It is shown that the real part of $Z_{XY}$ is a negative resistance and the imaginary part is the series impedance of $C_1$ and $C_2$. Thus, the equivalent circuit can be simplified to Fig. 3.4, where $R_n$ is equal to $-\frac{g_m}{C_1 C_2 \omega^2}$ and $C_n$ is equal to $\frac{C_1 C_2}{C_1 + C_2}$.

![Simplified equivalent circuit](image)

**Fig. 3.4 Simplified equivalent circuit**

The total admittance of the circuit is

$$Y_{total} = \frac{1}{Z_{FBAR}} + \frac{1}{Z_{XY}}$$  \hspace{1cm} (3.4)

If at one frequency at which the imaginary part of $Y_{total} = 0$, also can be written as

$$\text{imag} \left( \frac{1}{Z_{FBAR}} \right) + \text{imag} \left( \frac{1}{Z_{XY}} \right) = 0$$  \hspace{1cm} (3.5),

the real part of $Y_{total}$ is

$$\text{real} \left( Y_{total} \right) = \text{real} \left( \frac{1}{Z_{FBAR}} \right) + \text{real} \left( \frac{1}{Z_{XY}} \right) = 0$$  \hspace{1cm} (3.6),

it means that the loss of FBAR is completely compensated by the negative resistance generated by transistors and the circuit starts oscillate.
As shown in Fig. 3.5, because at $f_{\text{osc}}$ the admittance of the proposed Pierce FBAR-DCO satisfies the conditions in (3.5) and (3.6), the oscillator can operate at $f_{\text{osc}}$. Oscillation judgment can also be done by the stability analysis simulation. Fig. 3.6 shows the small signal loop gain and phase shift of proposed Pierce FBAR-DCO. It is indicated that in the frequency about 2.45 GHz, the loop gain is larger than zero and the total phase shift of the circuit is zero, satisfying the Barkhausen criteria.

Fig. 3.5 Admittance of the proposed Pierce FBAR-DCO
3.2.2 Simulation Result

The proposed Pierce FBAR-DCO is designed in TSMC 0.18 µm CMOS technology. The frequency tuning curve is shown in Fig. 3.7. In the proposed design, frequency tuning is realized by a 5 bits capacitor bank. The 5 bits capacitor bank provide a tuning range about 10 MHz. Compared to LC-VCO, the tuning range of FBAR oscillator is always narrow, because FBAR shows inductance characteristic only between $f_s$ and $f_p$, and the frequency difference of $f_s$ and $f_p$ is very small.
Fig. 3. 7 Tuning curve of the proposed FBAR-DCO

The output waveform is shown in Fig. 3.8 and Fig. 3.9 is the phase noise performance. It is indicated that with 0.65 V voltage supply, the peak to peak voltage of the output reached 0.6 V, and the phase noise is about -148 dBc/Hz at 1 MHz offset frequency. Compared to LC-VCO, the phase noise has been improved about 20dB. The FOM is able to be calculated by [34]

$$FOM = L(Δf) - 20\log(\frac{f_0}{Δf}) + 10\log(\frac{P_{DC}}{1mW})$$  \hspace{1cm} (3.7)

where \(L(Δf)\) is the phase noise at the offset frequency from the oscillation frequency \(f_0=2.46\ \text{GHz}\), and \(P_{DC}\) is the DC power consumption. Thus, the FOM is about -210.36 dB.
Fig. 3. 8 Output waveform of the proposed Pierce FBAR-DCO

Fig. 3. 9 Phase noise comparison between the proposed FBAR-DCO and LC-VCO
3.2.3 Chip Fabrication

The proposed Pierce FBAR-DCO was fabricated in TSMC 0.18 µm CMOS technology. Chip photograph is shown in Fig. 3.10 (a), where the size including pads is 850 µm×550 µm. When integrating FBAR to the chip, we employed monolithic FBAR-CMOS integration method [35] instead of using bonding wire, directly integrating FBAR above CMOS substrate, to reduce the parasitic inductance between FBAR and CMOS pads and not increase the size of the final chip, as shown in Fig. 3.10 (b). However, the chip was failed because the measured $R_m$ of the FBAR is as high as 550 Ohm. In the condition of the high $R_m$, the FBAR doesn’t have a resonance around 2.4 GHz.
Fig. 3. 10 Photograph of Pierce FBAR-DCO (a) without FBAR,
(b) with FBAR integrated
3.3. Inverter based FBAR-DCO

3.3.1 Inverter based FBAR-DCO Design and Analyses

The proposed inverter based FBAR-DCO is shown in Fig.3.11. In the proposed FBAR-DCO, PMOS transistor $M_1$ and NMOS transistor $M_2$ constitutes an inverter and $M_8$ is kept in transistor region as a large resistor to provide gate bias voltage. Transistors ($M_2$-$M_7$) make up a 3 bits capacitor bank. In this architecture, both $M_1$ and $M_2$ are used to generate negative resistance and the current of the circuit is reused. The generated negative resistance can be described by modifying (3.3) to

$$-\frac{g_{pm} + g_{nm}}{C_1C_2\omega^2} + \frac{1}{j\omega C_2} + \frac{1}{j\omega C_1}$$

(3.8)
where \( g_{pm} \) and \( g_{nm} \) are the trans-conductance of PMOS transistors and NMOS transistors respectively. Therefore, the generated negative resistance is \( \frac{g_{pm} + g_{nm}}{C_1 C_2 \omega^2} \). Compared to the previous one in Fig.3.2, It is clear that the inverter based FBAR-DCO can generate larger negative resistance, with same bias current.

![Fig. 3.12 Curve of \( |V_{th}| - VFBB \)](image)

In order to reduce the power consumption, forward body bias (FBB) technique is employed in the proposed design. Unlike normal connection of transistors, in FBB technique, both the bodies of PMOS and NMOS transistors are connected to a low bias
voltage \( (V_{FBB}) \) to reduce the threshold voltage of transistors \( (V_{th}) \). It is usually used in the design of high-speed prescaler to reduce power consumption and increase the operation frequency [36]. The curve of \( V_{th}-V_{FBB} \) for 0.18 \( \mu \)m CMOS transistors is shown in Fig. 3.12. As can be seen, the threshold voltage declines as the forward body bias voltage increases. In the proposed circuit, the bodies of PMOS and NMOS transistors are connected to bias voltage respectively through large resistors. The purpose of large resistors between the bodies of transistors and bias voltage is to prevent from excessively high bias voltage to avoid large leakage current. With connecting the body bias voltage, the \( |V_{th}| \) of PMOS is decrease to 350 mv, and the \( V_{th} \) of NMOS is decrease to 400 mv. Finally, benefit from the FBB technique, the proposed circuit can work under 1 V voltage supply with 0.5 mA current consumption.

### 3.3.2 Simulation Result

The proposed inverter based FBAR-DCO is designed in TSMC 0.18 \( \mu \)m CMOS technology. The output waveform is shown in Fig. 3.13 and Fig. 3.14 is the phase noise performance. It is indicated that with 1.0 V voltage supply and 0.5 mA current consumption the proposed DCO operates at 2.48 GHz and the peak to peak voltage of the output reached 0.8 V; the phase noise is about -139.4 dBC/Hz at 1 MHz offset frequency and the FOM is about -210.50 dB.
Fig. 3. 13 Output waveform of the proposed inverter based FBAR-DCO

Fig. 3. 14 Phase noise of the proposed inverter based FBAR-DCO
3.3.3 Chip Fabrication

The proposed inverter based FBAR-DCO was fabricated in TSMC 0.18 µm CMOS technology. Chip photograph is shown in Fig. 3.15, where the size including pads is 850 µm×750 µm. The monolithic FBAR-CMOS integration method was also used in this fabrication. It is a pity that the chip was failed either because the parallel impedance of FBAR is decreased too much as the measured $R_m$ of the FBAR, which is about is 17 ohm, is too high for an FBAR resonator.

![Chip Photograph](image)

Fig. 3. 15 Photograph of inverter based FBAR-DCO

3.4 Conclusion

In this chapter, a Pierce FBAR-DCO and an inverter based FBAR-DCO are presented. The circuit design is described and the oscillation condition is analyzed in detail.
The post-layout simulation results show that both two FBAR-DCO have low power consumption and low phase noise. Table 3.1 shows the comparison between the two proposed FBAR-DCO and other publish VCO. It is clear that the proposed FBAR-DCOs have better FOMs.

Table 3.1 Comparison with other published oscillators

<table>
<thead>
<tr>
<th></th>
<th>Post-layout simulation result of proposed Pierce FBAR-DCO</th>
<th>Post-layout simulation result of proposed inverter FBAR-DCO</th>
<th>[24]</th>
<th>[25]</th>
<th>[26]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18µm CMOS</td>
<td>0.18µm CMOS</td>
<td>0.25µm BiCMOS</td>
<td>0.13µm CMOS</td>
<td>0.18µm CMOS</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>0.65</td>
<td>1.0</td>
<td>2.4</td>
<td>1.0</td>
<td>1.8</td>
</tr>
<tr>
<td>$f_0$ (MHz)</td>
<td>2460</td>
<td>2480</td>
<td>2100</td>
<td>1575</td>
<td>1500</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>3.25</td>
<td>0.5</td>
<td>58</td>
<td>0.5</td>
<td>3.78</td>
</tr>
<tr>
<td>Tuning range (MHz)</td>
<td>10</td>
<td>9</td>
<td>37</td>
<td>1.35</td>
<td>1</td>
</tr>
<tr>
<td>$L(Δf)$ @ 1MHz (dBc/Hz)</td>
<td>-147.7</td>
<td>-139.4</td>
<td>-144</td>
<td>-138</td>
<td>-142</td>
</tr>
<tr>
<td>FOM</td>
<td>-210</td>
<td>-210</td>
<td>-193</td>
<td>-204</td>
<td>-200</td>
</tr>
</tbody>
</table>

Fig. 3. 16 Parallel resonance impedance of FBAR when $R_0$ is kept at 0.5 ohm
Nevertheless, although the two proposed FBAR-DCO was fabricated in TSMC 0.18 µm CMOS technology and used monolithic FBAR-CMOS integration method in the fabrication, both of them cannot start oscillation. The most probable reason is the measured $R_m$ of the FBAR is too large. For the Pierce FBAR-DCO, the $R_m$ is as high as 500 ohm. For the inverter based FBAR-DCO, the $R_m$ is 17 ohm. Both of the two $R_m$ are far greater than the desired 0.5 ohm. Fig. 3.16 shows that when $R_0$ is kept at 0.5 ohm, the parallel resonance impedance is reduced shapely with the increasing of $R_m$. Thus, in order to make these two FBAR-DCOs oscillate successfully, the reduction of $R_m$ in fabrication is necessary.
Chapter IV
Cross-coupled and Multiband FBAR-VCO

4.1. Introduction

FBAR-VCOs are not only able to be used to in transceivers to replace LC-VCO. In the fields of frequency reference and high precision sensors which use frequency as the output variable, low phase noise miniature oscillator is greatly demanded [37-39]. Traditionally, quartz crystal oscillators are widely used because of the excellent phase noise performance [37, 38]. However, large physical size, incompatibility with CMOS technology and low frequency output has severely limited the applications of quartz crystal oscillators in GHz-range and in highly miniaturized sensors in the future.

In response to the growing demand for GHz-range frequency and miniaturization, FBAR resonators which have Q-factor around 1000 or even more, have been used to design low phase noise GHz-range oscillators [37-39] for frequency reference and highly reliable sensors to replace quartz crystal oscillators in recent years. Nevertheless, simple single-ended architecture is employed and the phase noise of these FBAR oscillators needs further optimization.

In this chapter, a 1.9 GHz cross-coupled FBAR-VCO and a 0.65 GHz, 0.98 GHz, 1.96GHz and 3.92 GHz multiband FBAR-VCO are presented. The low frequency instability problem is analyzed and the solution methods are proposed. An excellent phase noise and high loop gain are obtained by considering the effect of transistors’ size on the Q-factor and impedance of FBAR and Oscillation frequencies are extended by a divider and a multiplier.
4.2. 1.9 GHz cross-coupled FBAR-VCO

4.2.1 Circuit Design

In this design, the parameters and the impedance response of the adopted FBAR are shown in Fig. 4.1. The parallel resonance frequency \( f_p \) is 1.96 GHz and the series resonance frequency is \( f_s \) 1.92 GHz. The parameter values is also obtained from (2.3)-(2.6). The \( Q_p \) and the \( Q_s \) of the FBAR, calculated by (2.7), are about 1200 and 800, respectively.

![Circuit Diagram](image)

**Fig. 4.1** Parameters and impedance response of the adopted FBAR

Because cross-coupled FBAR-VCO suffers from low frequency instability problem, simple single ended architecture is employed in most of the published FBAR-VCO [36-38]. In [25], although a cross-coupled FBAR-VCO is proposed, the phase noise
performance is not good and the reason and solution of low frequency instability is not explained in theory. In our design of FBAR-VCO, both NMOS ($M_1$, $M_2$) and PMOS ($M_3$, $M_4$) transistors are used to constitute two cross-coupled pairs to reuse current and provide larger negative resistance. Instead of obtaining gate bias voltage from the drains of cross-coupled transistors, two voltages $V_1$ and $V_2$ are added to the gates, which keep the transistors working in saturation region. A tail feedback current source, composed of $M_5$ and $M_6$, is used to control the common-mode drain voltage of the cross-coupled pairs and reduce $1/f$ noise furthermore. $V_{tune}$ is used to control the oscillation frequency of the VCO.

Fig. 4. 2 Circuit of the proposed FBAR-VCO
Large resistors $R_1-R_8$ are used as bias resistors to provide FBB bias voltage to all transistors. Capacitor $C_a$ creates a high frequency path to eliminate the low frequency instability, which will be presented in detail in section 4.2.2. The sizes of all transistors are well optimized, which prevents large Q-degeneration of FBAR caused by parasitic capacitance and on-resistance to get a low phase noise and a high loop gain. The optimized method will be described in section 4.2.3.

Fig. 4. 3 Equivalent circuit of the proposed FBAR-VCO

4.2.2. Low Frequency Instability Analyses and Elimination

In the design of a cross-coupled FBAR-VCO, because FBAR resonators are very similar to LC resonators at the parallel resonance frequency, the cross-coupled architecture of LC-VCO can also be employed. But the major challenge is to solve the instability in low
frequency which causes parasitic oscillation. In this subsection, not only the reason of instability is analyzed in theory, but also the solution methods are proposed. The first method employs a capacitor and while the other one employs a series inductor-capacitor.

![Redrawn equivalent circuit of the proposed FBAR-VCO](image)

To describe the instability problem, the equivalent circuit of this FBAR-VCO is shown as Fig. 4.3, where \( Z_f \) is the impedance of FBAR, and \( Z_c \) is the impedance between two sources of cross-coupled pair. Because both two cross-coupled pairs are used to generate negative resistance, in order to calculate the loop gain, this equivalent circuit can be redrawn in Fig.4.4, where \( R_{Pon} \) and \( R_{Non} \) are the on-resistance of PMOS transistors and NMOS transistors respectively; the trans-conductance of \( M_x \) and \( M_y \) \( (g_m) \) is the sum of the trans-conductance of PMOS transistors \( g_{pm} \) and NMOS transistors \( g_{nm} \). In order to calculate loop gain, the cross-coupled pair is cut from the gate of \( M_x \) and the input and output are named as \( V_{in} \) and \( V_{out} \), respectively. Thus the small signal equivalent circuit of Fig 4.4 can
be drawn in Fig. 4.5, where $V_{gxx}$ and $V_{gsy}$ are the voltages between the gate and source of $M_x$ and $M_y$ respectively.

![Diagram of small signal equivalent circuit](image)

**Fig. 4.5** Small signal equivalent circuit of the circuit in Fig. 4.4

Based on the small signal equivalent circuit, the equations of $V_{out}$, $V_{in}$ and $V_{gsy}$ can be written as (4.1), (4.2) and (4.3) respectively.

$$V_{out} = V_{gsy} g_m \left( R_{Non} \parallel R_{Pon} \parallel \frac{Z_s}{2} \right)$$  \hspace{1cm} (4.1)

$$V_{in} = V_{gxx} + V_{gsx} g_m \frac{Z_s}{2}$$  \hspace{1cm} (4.2)

$$V_{gsy} = V_{gxx} g_m \left( R_{Non} \parallel R_{Pon} \parallel \frac{Z_s}{2} \right) - V_{gsx} g_m \frac{Z_s}{2}$$  \hspace{1cm} (4.3)

Then rearranging (4.3), the relationship between $V_{gxx}$ and $V_{gsy}$ can be gotten as (4.4).

$$\frac{V_{gsy}}{V_{gxx}} = \frac{g_m \left( R_{Non} \parallel R_{Pon} \parallel \frac{Z_s}{2} \right)}{1 + g_m \frac{Z_s}{2}}$$  \hspace{1cm} (4.4)

Using (4.1), (4.2) and (4.4), the loop gain can be calculated as (4.5), based on the definition of loop gain.
\[ \text{Gain} = \frac{V_{\text{out}}}{V_{\text{in}}} = \left( \frac{g_m (R_{\text{Non}} \parallel R_{\text{Pon}}) \frac{Z_f}{2}}{1 + g_m \frac{Z_s}{2}} \right)^2 \]  

(4.5)

From (4.5), it is clear that high loop gain occurs not only at the frequency \( f_p \), but also occurs in low frequency as FBAR also has high impedance in low frequency as shown in Fig. 4.1, and \( Z_s \) is always small in normal condition. For this reason, low frequency instability and parasitic oscillation will happen if loop gain exceeds 0 dB satisfying Barkhausen’s criterion which is illustrated in Fig. 4.6.

![Parasitic oscillation](image)

Fig. 4. 6 Parasitic oscillation of a cross-coupled FBAR-VCO

To prevent parasitic oscillation, the high loop gain in low frequency should be reduced by increasing \( Z_s \) in low frequency. The two methods to enhance \( Z_s \) are shown in Fig. 4.7. For the first one, the capacitor \( C_a \) is added between the sources of \( M_3, M_4 \). This capacitor which creates a high frequency path reduces the loop gain in low frequency. If the value of \( C_a \) is not large enough, it will cause an undesirable reduction of the loop gain at the frequency \( f_p \). If the value of \( C_a \) is too large, parasitic oscillation will not be eliminated.
Thus, in this letter, $C_a$ is set to 2 pF for the trade-off between low frequency stability and loop gain.

![Diagram](image)

**Fig. 4.** Two methods for enhancing $Z_s$ in low frequency

In the second one, a series inductor-capacitor (series-$L_a C_b$) which has resonance frequency at $f_p$ is used. In this letter, to get low series resonance impedance, the $L_a$ and the $C_b$ are set to 6 nH and 1.1 pF respectively. It provides lower impedance around $f_p$ and higher impedance in low frequency as shown in Fig. 4.8. In Fig. 4.9 (a), it can be seen that in low frequency, the loop gain for series- $L_a C_b$ is lower by 0.6 dB compared to that for $C_a$ only; and in (b), the loop gain for series- $L_a C_b$ is increased by 12 dB compared to that for $C_a$ only in high frequency.
Fig. 4. 8 Impedance comparison of $C_a$ and series-$L_aC_b$

Fig. 4. 9 Loop gain comparison by using the two methods for enhancing $Z_s$
The two methods of enhancing $Z_s$ can solve the parasitic oscillation in low frequency. In addition, other methods are also employed to further improve the gain margin in low frequency.

The first method is to reduce $Z_f$ in low frequency. In the proposed VCO, the resistor $R_p$ is connected to FBAR in parallel to decrease the infinite impedance of FBAR in low frequency. Since the parallel resistor also leads to the impedance reduction of FBAR at parallel frequency, 10K ohm resistor is selected to avoid the deterioration of Q-factor.

![Graph showing low frequency gain margin with the size changing of the NMOS transistors $M_3$ and $M_4(W_n)$](image)

**Fig. 4. 10 Low frequency gain margin with the size changing of the NMOS transistors $M_3$ and $M_4(W_n)$**

For the second one, the effect of the size of NMOS transistors on the gain margin in low frequency is considered. Fig. 4.10 shows that the gain margin in low frequency
decreases with the decrease in the size of NMOS transistors \( M_3 \) and \( M_4 \) \( (W_n) \). The reason is that the impedance of FBAR has a great growth with frequency decrease and the frequency in which phase margin is equal to zero, is decreasing with the decrease of \( W_n \). In this letter, \( W_n \) is set to 30 \( \mu \)m.

4.2.3. Optimization of Phase Noise and Loop Gain

In Leeson phase noise model, the relationship between \( Q \) and phase noise is given by:

\[
L(f_m) \propto \frac{kT}{P_{out}} \cdot \frac{1}{2Q^2} \cdot \frac{f_0^2}{f_m^2}
\]

where \( k \) and \( T \) are constants; \( L(f_m) \) is the phase noise at the offset frequency \( f_m \) from the oscillation frequency \( f_0 \) and \( P_{out} \) is the output power. It is known that phase noise improves as both the carrier power and \( Q \)-factor increase. Because the \( Q \)-factor of FBAR will be deteriorated by the on-resistance reduction of transistors, large size transistors should be avoided. Both the size reduction of PMOS transistors and that of NMOS transistors can raise the on-resistance, but based on the analysis in subsection 4.2.2, the size reduction of NMOS transistors will decrease the gain margin in low frequency. Therefore, only the size of PMOS transistors is adjusted to optimize the phase noise. In Fig. 4.11 (a), it is shown that when the size of PMOS transistor \( M_1 \) and \( M_2 \) \( (W_p) \) is decreasing from 110 \( \mu \)m to 50 \( \mu \)m, the \( Q \)-factor of FBAR is increasing and the phase noise is improving. Thus, this region is called \( Q \) limit region in this paper. When \( W_p \) is below 50 \( \mu \)m, although the \( Q \)-factor is still increasing, the phase noise is not improving because of the reduction of the oscillation amplitude, which is called peak to peak voltage \( (V_{pp}) \) limit region. For the loop gain, it can
be known from (4.5) that since the loop gain also increases with the increase in on-resistance of transistors, the optimal size which can get the best phase noise, can also obtain high loop gain, as shown in Fig. 4.11 (b).
Fig. 4. 11 Relationship among the size of PMOS transistor $M_1$ and $M_2 (W_p)$, Q-factor, phase noise (a) and loop gain (b)

4.2.4. Simulation Result

Using the proposed solutions of low frequency instability, the proposed 1.9 GHz FBAR-VCO is designed in 0.18 µm CMOS successfully. Fig. 4.12 is the layout and Fig. 4.13 is the differential output waveform. The simulation phase noise is shown in Fig. 4.14. It is shown that enhancing $Z_s$ by using series-$L_a C_b$ can achieve better phase noise, because series-$L_a C_b$ has lower loss at $f_p$. The phase noise is improved from $-151.5$ dBc/Hz to $-153.5$ dBc/Hz at 1 MHz offset frequency. The FOM is also improved from -215 dB to -217 dB.
Although enhancing $Z_s$ by using series-$L_aC_b$ can get a better performance, it takes larger chip size because of a 6nH inductor. And it can be known from Fig. 4.9 that enhancing $Z_s$ by only using $C_a$, the 7.9dB gain margin is enough to suppress the parasitic oscillation and the -151.5dBc/Hz phase noise is also enough for most application. Therefore, to save the cost of fabrication, only $C_a$ is adopted in the final design. The tuning range is narrow because the FBAR shows inductance characteristic only between $f_s$ and $f_p$, and the frequency difference of $f_s$ and $f_p$ is very small.
Fig. 4. 13 Output waveform of the proposed FBAR-VCO

Fig. 4. 14 Phase noise comparison of FBAR-VCO by using the two methods for enhancing $Z_s$
Table 4.1 shows the comparison between this work and other published works. Compared to other published FBAR-VCOs, the proposed FBAR-VCO has better phase noise and FOM.

<table>
<thead>
<tr>
<th></th>
<th>This work with $C_a$ (Post-layout)</th>
<th>This work with $L_a C_b$ (Post-layout)</th>
<th>[24]</th>
<th>[25]</th>
<th>[26]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.18µm CMOS</td>
<td>0.18µm CMOS</td>
<td>0.25µm BiCMOS</td>
<td>0.13µm CMOS</td>
<td>0.18µm CMOS</td>
</tr>
<tr>
<td>Vdd (V)</td>
<td>1.1</td>
<td>1.1</td>
<td>2.4</td>
<td>1.0</td>
<td>1.8</td>
</tr>
<tr>
<td>$f_0$ (MHz)</td>
<td>1962</td>
<td>1962</td>
<td>2100</td>
<td>1575</td>
<td>1500</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>1.7</td>
<td>1.7</td>
<td>58</td>
<td>0.5</td>
<td>3.78</td>
</tr>
<tr>
<td>Tuning range (MHz)</td>
<td>2</td>
<td>2</td>
<td>37</td>
<td>1.35</td>
<td>1</td>
</tr>
<tr>
<td>$L(\Delta f)$ @ 1MHz (dBc/Hz)</td>
<td>-151.5</td>
<td>-153.5</td>
<td>-144</td>
<td>-138</td>
<td>-142</td>
</tr>
<tr>
<td>FOM</td>
<td>-215</td>
<td>-217</td>
<td>-193</td>
<td>-204</td>
<td>-200</td>
</tr>
</tbody>
</table>

4.3. Multiband FBAR-VCO

4.3.1. Circuit Design

In this design, we employed the cross-coupled FBAR-VCO as a VCO core and to extend output frequencies, an extended true single phase clock logic (E-TSPC) based divide-by-2 or 3 divider is used to generate 0.65 GHz and 0.98 GHz output, and a current mode logic (CML) based multiply-by-2 multiplier is employed to generate 3.92 GHz frequency. The architecture of the proposed multiband FBAR-VCO is shown in Fig. 4.15.
In order to extend oscillation frequencies below 1 GHz without using CMOS switch, a high-speed frequency divide-by-2 or 3 divider is adopted in this work. Conventionally, current mode logic (CML), injection-locked logic and extended true single phase clock logic (E-TSPC) are the main solutions of high-speed frequency dividers. However, because all transistors of CML must be biased in saturation region, CML logic costs more current compared to E-TSPC logic in 1.9 GHz band. For injection-locked logic, on-chip inductors lead to large chip area and it is not easy to cover the divider ratio of both 1/2 and 1/3.
Based on the analyses above, the E-TSPC logic is utilized in this design, as shown in Fig. 4.16. \( CLK \) is the input port and \( V_0 \) is the output port. The divider is composed of two E-TSPC D-flip flops in which two \( AND \) gates are embedded. The divider ratio is simply controlled by the potential of \( MC \). When \( MC \) is low, node \( S_1 \) is set to logically high, and both \( S_2 \) and \( S_3 \) are disabled. Thus only one D-flip flop is activated and the divider is operated as divide-by-2. Conversely, when \( MC \) is high, the divider operates in the mode of divide-by-3.

In order to generate higher frequency, a frequency multiply-by-2 multiplier is included in our work. Traditionally, frequency multipliers are realized by the nonlinearity of CMOS transistors. However, harmonics suppression and large power consumption are their challenges.

In our work, a CML logic based high-speed frequency multiplier is employed, as shown in Fig. 4.17. If two signals with same frequency but out of phase by 90 degree are
input to an XOR gate, the frequency of output signal will be two times the input signal frequency. In this work, the differential output signals of VCO are input to a passive RC phase shift network to generate quadrature signals. And the quadrature signals are used to drive the CML logic based high-speed XOR gate. Because this multiplier is not realized by the nonlinearity of CMOS transistors, the harmonics suppression problem doesn’t occur and the power consumption is also decreased.

Fig. 4. 17 Schematic of multiply-by-2 multiplier
4.3.2. Simulation Result

The proposed multiband FBAR-VCO designed in 0.18 µm CMOS operates at 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz successfully. The layout is shown in Fig. 4.18 and the output waveform is shown in Fig. 4.19. Fig. 4.20 shows the post-layout simulation phase noise is. Table 4.2 is the comparison between this work and other published works. It is shown that below 1.96 GHz, the proposed multiband FBAR-VCO has very low phase noise below -150 dBc/Hz at 1 MHz offset and even in 3.9 GHz, the phase noise is still below -140 dBc/Hz. All the FOMs of four bands are below -200 dB and the minimum FOM is as low as -215 dB, much better than other published works.

Fig. 4.18 Layout of the proposed multiband FBAR-VCO
Fig. 4. 19 Output waveform of the proposed multiband FBAR-VCO

Fig. 4. 20 Phase noise of the proposed multiband FBAR-VCO
Table 4.2. Comparison with other published oscillators

<table>
<thead>
<tr>
<th>Process</th>
<th>Proposed multiband FBAR-VCO (Post-layout)</th>
<th>[25]</th>
<th>[26]</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd (V)</td>
<td>0.18 µm CMOS</td>
<td>1.1</td>
<td>1.0</td>
</tr>
<tr>
<td>$f_0$ (MHz)</td>
<td>650 980 1960 3920</td>
<td>1575</td>
<td>1500</td>
</tr>
<tr>
<td>Power (mW)</td>
<td>3.97 4 1.7 4.3</td>
<td>0.5</td>
<td>3.78</td>
</tr>
<tr>
<td>Tuning range (MHz)</td>
<td>0.67 1 2 4</td>
<td>1.35</td>
<td>1</td>
</tr>
<tr>
<td>$L(f)@1$MHz (dBc/Hz)</td>
<td>-154.6 -153.5 -151.5 -143.2</td>
<td>-138</td>
<td>-142</td>
</tr>
<tr>
<td>FOM</td>
<td>-205 -207 -215 -209</td>
<td>-204</td>
<td>-200</td>
</tr>
</tbody>
</table>

4.4. Conclusion

In this Chapter, a 1.9 GHz cross-coupled FBAR-VCO and a multiband FBAR-VCO operating at 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz for frequency reference or highly miniature sensors are presented. The reason and solutions of low frequency instability in cross-coupled FBAR-VCO is discussed and by novel optimization method, an excellent phase noise and FOM value is obtained.
Chapter V
FBAR-VCO based PLL

5.1. Introduction

In this Chapter, instead of LC-VCOs in the traditional PLL, the presented cross-coupled FBAR-VCO is employed to design an FBAR-VCO based PLL. It is composed of phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), FBAR-VCO and divider, as shown in Fig. 5.1. The novel charge pump design based on complementary logic switches is adopted to reduce the mismatch current and the current noise. The proposed PLL proves the possibility of FBAR-VCO based PLL and the simulation result shows the phase noise of FBAR-VCO is further improved.

![Diagram of FBAR-VCO based PLL](image)

Fig. 5.1 Structure of FBAR-VCO base PLL

The flow of design is shown as follow:

1. Set basic parameter such as reference frequency, tuning range of VCO, divide ratio, current of CP, loop-bandwidth and phase margin;
2. Design LPF and analyze stability;
3. Make behavior model and simulate locking process by Verilog-A;
4. Circuit design of each part;
5. Extract noise of each part by Spectre-RF and simulate the total phase noise of PLL;

5.2. Design of FBAR-VCO based PLL

5.2.1. Stability Analysis and LPF Design

Since PLL is a close loop feedback system, it is important to keep the stability of PLL. Fig. 5.2 shows the linear phase model of PLL [40].

\[ \Theta_{in}(j\omega) \rightarrow \frac{I_{cp}}{2\pi} \rightarrow H_f(j\omega) \rightarrow \frac{K_{vco}}{j\omega} \rightarrow \Theta_{out}(j\omega) \]

where, \( I_{cp} \) is the current of CP (A/rad); \( K_{vco} \) is the gain of VCO (rad/s/V); \( N \) is the divide ratio of divider; and \( H_f(j\omega) \) is the transform function of LPF. In our design, a third-order passive LPF is adopted as shown in Fig. 5.3.
Thus, the transform function of LPF is

\[
H_y(j\omega) = \frac{1}{j\omega} \cdot \frac{(1 + j\omega R_1 C_1)/(C_1 + C_2 + C_3)}{1 + j\omega R_1 (C_2 + C_3) + (j\omega)^2 R_1 R_2 C_2 C_3} + \frac{(j\omega)^2 R_1 R_2 C_2 C_3}{C_1 + C_2 + C_3}
\]  (5.1)

As \(C_1 \gg C_2, C_3\)

\[
H_y(j\omega) \approx \frac{1}{j\omega (C_1 + C_2 + C_3)} \cdot \frac{(1 + j\omega R_1 C_1)}{1 + j\omega R_1 (C_2 + C_3) + (j\omega)^2 R_1 R_2 C_2 C_3}
\]

\[
= \frac{1}{j\omega (C_1 + C_2 + C_3)} \cdot \frac{(1 + j\omega/\omega_z)}{(1 + j\omega/\omega_{p2}) (1 + j\omega/\omega_{p3})}
\]  (5.2)

Where,

\[
\omega_z = \frac{1}{R_1 C_1}
\]  (5.3)

\[
\omega_{p2} = \frac{1}{R_1 (C_2 + C_3)}
\]  (5.4)

\[
\omega_{p3} = \frac{1}{R_2 C_2 C_3 / (C_2 + C_3)}
\]  (5.5)

In order to calculate the component value of the LPF, first we need to set some basic parameter as Table 5.1:
Table 5.1 Basic parameter of PLL

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Locking time $T_{lock}$</td>
<td>400 µS</td>
</tr>
<tr>
<td>Maximum frequency of VCO $f_{max}$</td>
<td>1961 MHz</td>
</tr>
<tr>
<td>Minimum frequency of VCO $f_{min}$</td>
<td>1959 MHz</td>
</tr>
<tr>
<td>Maximum control voltage of VCO $V_{max}$</td>
<td>1.4 V</td>
</tr>
<tr>
<td>Minimum control voltage of VCO $V_{min}$</td>
<td>0.4 V</td>
</tr>
<tr>
<td>Current of CP $I_{cp}$</td>
<td>100 µA</td>
</tr>
<tr>
<td>Divide ratio $N$</td>
<td>40</td>
</tr>
<tr>
<td>Open loop phase margin $\phi_m$</td>
<td>53°</td>
</tr>
</tbody>
</table>

Since the open loop gain of PLL is

$$H_{ol}(j\omega) = \frac{I_{cp}K_{vco}H_{v}(j\omega)}{2\pi N j\omega}$$ (5.6)

Where,

$$K_{vco} = \frac{2\pi(f_{max} - f_{min})}{V_{max} - V_{min}}$$ (5.7)

The bandwidth of PLL is solved from $|H_{ol}(j\omega)|=1$:

$$\omega_c = K \frac{C_1}{C_1 + C_2 + C_3} \cdot \frac{\cos(\phi_{p2}) \cos(\phi_{p3})}{\sin(\phi_2)}$$ (5.8)

Where,

$$K = \frac{I_{cp}K_{vco}R_i}{2\pi N}$$ (5.9)

$$\phi_2 = \tan^{-1}(\frac{\omega_c}{\omega_z})$$ (5.10)
\[
\phi_{p2} = \tan^{-1}(\omega_c / \omega_{p2})
\]  
(5.11)

\[
\phi_{p3} = \tan^{-1}(\omega_c / \omega_{p3})
\]  
(5.12)

Thus, the open loop phase margin is

\[
\phi_m = \phi_z - \phi_{p2} - \phi_{p3} = \tan^{-1}(\omega_c / \omega_z) - \tan^{-1}(\omega_c / \omega_{p2}) - \tan^{-1}(\omega_c / \omega_{p3})
\approx \tan^{-1}(\omega_c / \omega_z) - \tan^{-1}(\omega_c / \omega_{p2})
\]  
(5.13)

To keep stability, when \(|H_{oi}(j\omega)| = 1\), maximum phase margin should be obtain,

\[
\omega_c = \sqrt{\omega_{p2}\omega_z} = \sqrt{d}\omega_z
\]  
(5.14)

Where,

\[
d = \frac{C_1}{C_2 + C_3}
\]  
(5.15)

Then,

\[
\phi_{m_{\text{max}}} = \tan^{-1}(\sqrt{\omega_{p2}/\omega_z}) - \tan^{-1}(\sqrt{\omega_z/\omega_{p2}}) = \tan^{-1}\frac{d - 1}{2\sqrt{d}}
\]  
(5.16)

Since \(\sin(\phi_z) = \cos(\phi_{p2}) \cos(\phi_{p3})\), (5.8) is simplified as

\[
\omega_c = K \frac{C_1}{C_1 + C_2 + C_3} = K \frac{1 + d}{d}
\]  
(5.17)

As \(\omega_c\) is also equal to

\[
\omega_c \approx 2\pi \frac{4}{T_{\text{lock}}}
\]  
(5.18)

From (5.14)-(5.18) and the basic parameter in Table 5.1, \(K, d, \omega_z, \omega_{p2}\) and \(\omega_c\) is able to be calculated, and then from (5.3)-(5.5), (5.7) and (5.9), \(R_1, R_2, C_1, C_2, C_3\) can be obtained. The calculated parameters are shown in Table 5.2.
Table 5.2 Parameters of LPF

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_1$</td>
<td>17.427 K Ohm</td>
</tr>
<tr>
<td>$R_2$</td>
<td>15.186 K Ohm</td>
</tr>
<tr>
<td>$C_1$</td>
<td>2513.2 pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>231.89 pF</td>
</tr>
<tr>
<td>$C_3$</td>
<td>100 pF</td>
</tr>
</tbody>
</table>

After the parameters of LPF are calculated, the stability analyses should be done by Simulink. The bode graph of the proposed PLL is shown in Fig. 5.4.

![Bode Diagram](image)

Fig. 5.4 Bode graph of the proposed PLL
It is known in Fig. 5.4 that the bandwidth of PLL is about 10 KHz and the phase margin is about 45°, which can keep the stability of the proposed PLL. In addition, because of $C_1$ cannot be integrated, an off-chip capacitor is used in our design.

After calculating the parameters of LPF, the behavior simulation result of locking process is shown in Fig. 5.5. It is know that the PLL is locked at about 400 µS.

![Fig. 5.5 Locking process of PLL](image)
5.2.2. Circuit Design

5.2.2.1. PFD and CP design

PFD detects the phase difference between the reference signal and the feedback signal from divider. A traditional tri-state PFD [31] is employed in our design, as shown in Fig 5.6. It is based on two D-flip flops and an AND gate, and both D-flip flop inputs are tied high. The reference and the output of the divider are each fed into a clock input of one of the D-flip flops.

![Fig. 5.6 Traditional tri-state PFD](image)

Fig. 5.6 Traditional tri-state PFD
One of the most significant part of the PLL is the charge pump. The current mismatch of CP must be reduced as lower as possible to reduce the current noise. The schematic of proposed CP is shown in Fig 5.7. Transistors $M_1-M_{12}$ are used to constitute a cascode current source to improve the output impedance and reduce the current mismatch of node $X$ and $Y$. Transistors $M_{13}-M_{20}$ make up four complementary logic switches to restrain clock feed-through, and an operation amplitude is used to keep the voltage of node A and B in equal to reduce charge sharing. The current mismatch characteristic of CP (a) and the current noise of PFD and CP (b) are shown in Fig. 5.8. It is shown that the current mismatch is below 0.1% and the current noise is also very low.

Fig. 5. 7 Schematic of CP
Fig. 5. 8 Current mismatch characteristic of CP (a) and current noise of PFD and CP (b)
5.2.2.2. Divider design

The proposed divider employs multi-modulus divider (MMD) architecture [41] which is based on divide-by 2/3 divider connected on series, as shown in Fig. 5.9.

![Divider based on MMD architecture](image)

Fig. 5.9 Dividers based on MMD architecture

For this type of divider, a division ratio that increases in unity integer steps from $2^n$ to $2^{n+1}-1$ is able to be achieved, and the division ratio is given by:

$$N = P_0 + 2^1 P_1 + \ldots + 2^{n-2} P_{n-2} + 2^{n-1} P_{n-1} + 2^n$$  \hspace{1cm} (5.19)

Thus, in our design, for $N=49$, five divider cell are used and the control word is 10001 ($P_4$ to $P_0$).

The proposed divide by 2/3 divider cell and the timing diagram is shown in Fig. 5.10. It is known that the divider cell is composed of two E-TSPC flip-flops and one inverter. The first flip-flop (DFF1) embeds a logic gate A&(B+C) and the second one (DFF2) embeds an AND gate. The proposed divider cell takes three input signals $CLK$, $MI$, and $P$, and produces two output signals $MO$ and $FO$. When $P=0$ or $MO=0$, the mode select signal $B$ is high resulting in the divide-by-2 mode. For the divide-by-3 mode, the signals $P=1$, $FO=1$, $MI=1$, and $FI=1$ before passing the line Ec. The falling edge of $CLK$ at dash line Ec causes that $MO$ is changed from 0 to 1 that causes $B$ is changed from 1 to 0.
Fig. 5. 10 Proposed 2/3 divider cell and timing diagram
The output waveform (a) and output noise (b) of MMD based divider are shown in Fig. 5.11.

Fig. 5.11 Output waveform (a) and output noise (b) of MMD based divider
5.2.3. Phase Noise Analysis

The linear phase model of PLL with noise generated by each building block is shown in Fig. 5.12[40].

Where, $\Theta_{in}(j\omega)$ is the phase noise from the reference signal; $I_{cp}(j\omega)$ is current noise associated with PFD and charge pump; $V_{if}(j\omega)$ is voltage noise generated by LPF; $\Theta_{vco}(j\omega)$ is VCO output phase noise; $\Theta_{div}(j\omega)$ is phase noise generated by the divider; $\Theta_{out}(j\omega)$ is total PLL output phase noise.

From the noise model of PLL, the phase noise transfer function of each noise source to the output phase noise is listed in Table 5.3.

<table>
<thead>
<tr>
<th>Noise source</th>
<th>Phase transfer function</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input noise</td>
<td>$H_{in,n}(j\omega) = \Theta_{out}(j\omega)/\Theta_{in}(j\omega)$</td>
</tr>
<tr>
<td>PFD/CP noise</td>
<td>$H_{cp,n}(j\omega) = \Theta_{out}(j\omega)/I_{cp}(j\omega)$</td>
</tr>
</tbody>
</table>

$$H_{in,n}(j\omega) = \frac{N \cdot \frac{H_{oi}(j\omega)}{1 + H_{ol}(j\omega)}}{1}$$

$$H_{cp,n}(j\omega) = \frac{2\pi N \cdot \frac{H_{oi}(j\omega)}{I_{cp}}}{1 + H_{ol}(j\omega)}$$
<table>
<thead>
<tr>
<th>Block</th>
<th>Noise Model</th>
<th>Equation</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPF noise</td>
<td>$H_{lf,n}(j\omega) = \Theta_{out}(j\omega)/V_{lf}(j\omega)$</td>
<td>$K_{\Theta} \frac{1}{j\omega + 1/H_{ol}(j\omega)}$</td>
</tr>
<tr>
<td>VCO noise</td>
<td>$H_{vco,n}(j\omega) = \Theta_{out}(j\omega)/\Theta_{vco}(j\omega)$</td>
<td>$1 + \frac{1}{1 + H_{ol}(j\omega)}$</td>
</tr>
<tr>
<td>Divider noise</td>
<td>$H_{div,n}(j\omega) = \Theta_{out}(j\omega)/\Theta_{div}(j\omega)$</td>
<td>$-\frac{N}{1 + H_{ol}(j\omega)}$</td>
</tr>
</tbody>
</table>

Since total output noise PSD is the contribution of noise PSD of each block, the total output noise PSD is:

$$S_{out}(\omega) = S_{in,n}(\omega)H_{in,n}(j\omega)^2 + S_{cp,n}(\omega)H_{cp,n}(j\omega)^2 + S_{lf,n}(\omega)H_{lf,n}(j\omega)^2 + S_{vco,n}(\omega)H_{vco,n}(j\omega)^2 + S_{div,n}(\omega)H_{div,n}(j\omega)^2$$  \hspace{1cm} (5.20)

Where, $S_{in,n}(\omega)$ is the phase noise PSD from the reference signal; $S_{cp,n}(\omega)$ is current noise PSD associated with PFD and charge pump; $S_{lf,n}(\omega)$ is voltage noise PSD generated by LPF; $S_{vco,n}(\omega)$ is VCO output phase noise PSD; $S_{div,n}(\omega)$ is phase noise PSD generated by the divider; $S_{out}(\omega)$ is total PLL output phase noise PSD.

For PFD/CP and LPF we can directly extract the voltage noise PSD by Spectre-RF; for VCO and divider, first we can extract the phase noise $L(\omega_m)$ by Spectre-RF, and convert to phase noise PSD $S_\phi(\omega_m)$ by [39]:

$$L(\omega_m) = 10\log\left[\frac{S_\phi(\omega_m)}{2}\right]$$  \hspace{1cm} (5.21)

For reference signal, the phase noise PSD can be found by [40]:

$$S_{in,n}(\Delta\omega) = 10^{-16\pi} \cdot \left[1 + \left(\frac{\omega_0}{2\Delta\omegaQ_L}\right)^2 \left(1 + \frac{\omega}{\Delta\omega}\right)\right]$$  \hspace{1cm} (5.22)
where $\omega_0$ is the reference frequency; $\omega_c$ is the corner frequency, which is normally in the range 1-10 KHz; $Q_z$ is the Q-factor of the resonator, which is in the order of $10^4$ to $10^6$; $\Delta \omega$ is offset frequency.

After obtaining total output noise PSD by (5.20), the total phase noise can be converted by (5.21). The output phase noise of each block (a) and the total phase noise of PLL (b) are shown in Fig. 5.13. The layout of proposed PLL is shown in Fig.5.14. In Fig. 5.13(b), it is demonstrated that the phase noise of the PLL is much better than the free running FBAR-VCO below 10 KHz offset frequency.
Fig. 5. 13 Output phase noise of each block (a) and the total phase noise of PLL (b)

Fig. 5. 14 Layout of proposed PLL
5.3. Conclusion

In this Chapter, we replaced the LC-VCO of the traditional PLL by the presented cross-coupled FBAR-VCO, to design an FBAR-VCO based PLL. The LPF design method and stability analysis is presented and the circuit design of phase PFD, charge pump, and MMD divider is introduced. Especially for the design of charge pump, the architecture based on complementary logic switches is adopted to reduce the mismatch current and the current noise. Finally, the phase noise of PLL is analyzed and simulated. The simulation phase noise proves the possibility of FBAR-VCO based PLL and shows that the FBAR-VCO based PLL further improved the phase noise of FBAR-VCO.
Chapter VI
Conclusion and Future Work

6.1. Conclusion

This thesis mainly focuses on the design of monolithic low phase noise FBAR oscillator. In the beginning of this thesis, the demand of low cost, high performance and high integration of RFIC and the poor phase noise and high power consumption of the normal Ring-oscillators and LC-oscillators are emphasized. In order to solve these problem of current oscillators, researcher are trying using high Q-factor FBAR resonators to design low phase noise oscillators. Then the structure and equivalent circuit model of FBAR and the oscillator theory including Barkhausen criteria, negative resistance and phase noise model which can be used in FBAR oscillators are presented to provide the theoretical foundation of FBAR oscillator design. In the realization of FBAR oscillators, at first the Pierce FBAR-DCO and the inverter based FBAR-DCO are designed because of the simplicity structure. The oscillation condition of these two FBAR-DCOs is analyzed and the simulation result demonstrates that the FBAR-DCO is able to obtain a phase noise which is 20 dB lower than the phase noise of normal LC-oscillators. Then the second kind of FBAR oscillator in this thesis employs cross-couple architecture. Two methods to mitigate low frequency instability are proposed, which the first method employs a capacitor and while the other one employs a series inductor-capacitor. By considering the effect of transistors’ size on the Q-factor and impedance of FBAR, excellent phase noise and high loop gain are obtained. Furthermore, based on the designed cross-coupled FBAR-VCO core, a multiband FBAR-VCO operating at 0.65 GHz, 0.98 GHz, 1.96 GHz and 3.92 GHz is presented. Although the traditional divider and multiplier are employed, the possibility
of a multiband VCO using FBAR-VCO as a core circuit has been demonstrated. Finally, we replaced the LC-VCO of the traditional PLL by the presented cross-coupled FBAR-VCO, to design an FBAR-VCO based PLL. For the design of charge pump, the architecture based on complementary logic switches is adopted to reduce the mismatch current and the current noise. The proposed PLL proves the possibility of FBAR-VCO based PLL and the simulation result shows the phase noise of FBAR-VCO is further improved.

6.2. Future work

This section will provide future research opportunities for the designed prototypes in this work.

1. In the design of the pierce FBAR-DCO and the inverter based FBAR-DCO, the final fabrication was failed because of the $R_m$ is too large to oscillate. It is significant to find the approach to reduce $R_m$, or design an FBAR oscillator which can still oscillate even if the $R_m$ is large.

2. FBAR oscillators have two main applications. The first one is used as frequency reference to replace the quartz crystal oscillators while the second one is used as local oscillator to replace the normal Ring-VCOs and LC-VCOs. For the first application, the demand of low phase noise is satisfied by our novel phase noise optimization method. While for the second application, both low phase noise and wide tuning range are needed. Thus, the tuning range of the proposed FBAR oscillator is necessary to be improved. Now the method of improving tuning range based on parallel inductor-FBAR has been under investigation and will reported in near future.
Reference


